Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

(Accredited 'A++' Grade by NAAC with a score of 3.6)

Hingna Road, Wanadongri, Nagpur - 441 110

Master of Technology

SoE & Syllabus 20**25**

(Department of Electronics & Telecommunication)

M.Tech in VLSI Design

Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B.TECH SCHEME OF EXAMINATION 2025

(Scheme of Examination w.e.f. 2025-26 onward)

(Department of Electronics & Telecommunication Engineering)

M. Tech. in VLSI Design

SoE No. 25VLSD101

SN	Sem	Type	BoS/ Deptt	Sub. Code	Subject	T/P	Contact Hours				Credits	% Weightage		ESE Duration Hours
							L	T	P	Hrs		TA**	ESE	
FIRST SEMESTER														
1	1	PC	ETC	25VLSD101	VLSI Technology	T	3	0	0	3	3	20	80	3
2	1	PC	ETC	25VLSD102	CMOS Digital Circuit Design	T	3	0	0	3	3	20	80	3
3	1	PC	ETC	25VLSD103	**Lab:** CMOS Digital Circuit Design	P	0	0	2	2	1		40	
4	1	PC	ETC	25VLSD104	Digital System Design	T	3	0	0	3	3	20	80	3
5	1	PC	ETC	25VLSD105	**Lab:** Digital System Design	P	0	0	2	2	1		40	
6	1	PC	ETC	25VLSD106	Embedded System and RTOS	T	3	0	0	3	3	20	80	3
7	1	PE	ETC		**Professional Elective- I**	**T**	3	0	0	3	3	20	80	3
8	1	PE	ETC		**Professional Elective- II**	**T**	3	0	0	3	3	20	80	3
					TOTAL		**18**	**0**	**4**	**22**	**20**			

List of Professional Electives-I

1	1	PE-I	ETC	25VLSD111	PE I : MEMS Design and Fabrication
2	1	PE-I	ETC	25VLSD112	PE I : Machine Learning for VLSI Design
3	1	PE-I	ETC	25VLSD113	PE I : Advanced Computer Architecture

List of Professional Electives-II

1	1	PE-II	ETC	25VLSD131	PE II : Verification & Testing of VLSI Circuits
2	1	PE-II	ETC	25VLSD132	PE II : Advanced Nanotechnology
3	1	PE-II	ETC	25VLSD133	PE II : Advanced Digital Signal Processing

SECOND SEMESTER														
1	2	PC	ETC	25VLSD201	Analog IC Design	T	3	0	0	3	3	20	80	3
2	2	PC	ETC	25VLSD202	**Lab:** Analog IC Design	P	0	0	2	2	1		40	
3	2	PC	ETC	25VLSD203	VLSI Signal Processing	T	3	0	0	3	3	20	80	3
4	2	PC	ETC	25VLSD204	RF Circuit design	T	3	0	0	3	3	20	80	3
5	2	PC	ETC	25VLSD205	**Lab:** RF Circuit design	P	0	0	2	2	1		40	
6	2	PC	ETC	25VLSD206	Synthesis & Optimization of VLSI Circuits	T	3	0	0	3	3	20	80	3
7	2	PE	ETC		**Professional Elective -III**	T	3	0	0	3	3	20	80	3
8	2	PE	ETC		**Professional Elective -IV**	T	3	0	0	3	3	20	80	3
					TOTAL		**18**	**0**	**4**	**22**	**20**			

List of Professional Electives-III

1	2	PE-III	ETC	25VLSD211	PE III : VLSI for Wireless Communication
2	2	PE-III	ETC	25VLSD212	PE III : ASIC Design
3	2	PE-III	ETC	25VLSD213	PE III : CMOS Subsystem Design

List of Professional Electives-IV

1	2	PE-IV	ETC	25VLSD231	PE IV : Mixed Signal VLSI Design
2	2	PE-IV	ETC	25VLSD232	PE IV : Advanced VLSI Design
3	2	PE-IV	ETC	25VLSD233	PE IV : Low Power VLSI Design

THIRD SEMESTER														
1	3	STR	ETC	25VLSD301	Project Phase-I	P	0	0	20	20	10	100		
					TOTAL		**0**	**0**	**20**	**20**	**10**			

FOURTH SEMESTER														
1	4	STR	ETC	25VLSD401	Project Phase-II	P	0	0	36	36	18	60	40	
					TOTAL		**0**	**0**	**36**	**36**	**18**			

					GRAND TOTAL		**36**	**0**	**64**	**100**	**68**			

		June, 2025	**1.00**
Chairperson	**Dean (Acad. Matters)**	**Date of Release**	**Version**

Applicable for AY 2025-26 Onwards

I Semester

25VLSD101 – VLSI Technology

Course Outcomes:

Upon successful completion of the course the students will be able to

1. Describe the sequential steps in semiconductor fabrication processes such as wafer preparation, oxidation, and photolithography.
2. Analyze various etching and thin-film deposition techniques used in VLSI technology to evaluate their impact on device performance.
3. Apply the principles of ion implantation and diffusion processes for doping in semiconductor devices.
4. Compare different packaging techniques and evaluate their suitability for specific VLSI applications.

Unit:1	**Crystal growth & wafer preparation**	**7 Hours**

Crystal growth & wafer preparation, Processing considerations: Chemical cleaning, gettering the thermal Stress factors.Epitaxy: Vapors phase Epitaxy, Basic Transport processes & reaction kinetics, doping & auto doping, equipments, safety considerations, buried layers, epitaxial defects, molecular beam epitaxy, equipment used, film characteristics, SOI structure.

Contemporary Issues related to Topic

Unit:2	**Oxidation**	**6 Hours**

Growth mechanism & kinetics, Silicon oxidation model, interface considerations, orientation dependence of oxidation rates, thin oxides, Oxides, Oxidation technique & systems dry & wet oxidation. Masking properties of SiO2.Diffusion: Diffusion from a chemical source in vapour form at high temperature, diffusion from doped oxide source, diffusion from an ion implanted layer.

Contemporary Issues related to Topic

Unit:3	**Optical Lithography**	**7 Hours**

Lithography: Optical Lithography: optical resists, contact & proximity printing, projection printing, electron lithography: resists, mask generation, Electron optics, roster scans & vector scans, variable beam shape.X-ray lithography: resists & printing, X ray sources & masks. Ion lithography. Etching: Reactive plasma etching, AC & DC plasma excitation, plasma properties, chemistry & surface interactions, feature size control & anisotropic etching, ion enhanced & induced etching, properties of etch processing. Reactive Ion Beam etching, Specific etches processes: poly/polycide. Trench etching,

Contemporary Issues related to Topic

Unit:4	**Deposition Process**	**6 Hours**

Dielectric &polysilicon film deposition: Deposition processes, Polysilicon, Silicon dioxide, silicon nitride. Diffusion: Models of diffusion in solids, Ficks one dimensional diffusion equations, atomic diffusion mechanisms, Diffusivities of B,P,As &Sb, Diffusion enhancement & retardations, **Contemporary Issues related to Topic**		
Unit:5	**Implantation**	**7 Hours**
Ion implantation, range theory, equipment, annealing, Metallization, Metallization Applications, Metallization Choices, Physical vapor Deposition, Patterning, Metallization problems. **Contemporary Issues related to Topic**		
Unit :6	**VLSI Process integration**	**6 Hours**
VLSI Process integration, Fundamental considerations for IC processing, nMOS IC technology, CMOS IC technology, MOS memory IC technology, Bipolar IC technology, Yield & reliability, mechanism of yield loss in VLSI, modelling of yield loss mechanisms, reliability requirements for VLSI. **Contemporary Issues related to Topic**		
Total Lecture Hours		**39 Hours**

Textbooks	
1	S.M. Sze, " Modern Semiconductor Device Physics", John Wiley & Sons, 2000.
2	Chen,"VLSI Technology" Wiley, March 2003
3	VLSI technology and Circuits, Kaustav Banerjee and Shuji Ikeda, Wiley, 2013
Reference Books	
1	B.G. Streetman, "Solid State Electronics Devices", Prentice Hall, 2002.
2	VLSI fabrication principles, S. K. Gandhi, "John Wiley, New York",1983
YCCE e- library book links [ACCESSIBLE FROM COLLEGE CAMPUS]	
1	
MOOCs Links and additional reading, learning, video material	
1	https://archive.nptel.ac.in/courses/117/106/117106093/

I Semester

25VLSD102 – CMOS Digital Circuit Design

Course Outcomes:

Upon successful completion of the course the students will be able to

1. Analyze the characteristics of CMOS inverter.
2. Analyze the static and dynamic characteristics of CMOS circuits.
3. Design combinational and sequential circuits.
4. Evaluate the performance of CMOS circuits.

Unit:1	**CMOS processing technology:**	**7Hours**

MOS transistors, CMOS logic, NAND gate, combinational logic, NOR gate, Compound gates, Pass transistor and transmission gates, tristates, multiplexers, latches and flip flops, inverter cross section, fabrication process, Layout design rules, CMOS processing technology, CMOS Process enhancements, stick diagram, VLSI design flow ,Euler path in a CMOS gate.

Contemporary Issues related to Topic

Unit:2	**MOS transistor theory:**	**7Hours**

MOS transistor theory, Working of nMOS enhancement transistor & PMOS enhancement transistor, Ideal Current voltage characteristics, threshold voltage , nonideal current voltage effects, velocity saturation, mobility degradation, channel length modulation, Body effect, sub-threshold conduction, Junction leakage, Tunnelling, Temperature dependence, Geometry dependence, Small signal AC characteristics, CMOS inverter DC transfer characteristics, Beta ratio effects, noise margin, Ratioed inverter transfer function

Contemporary Issues related to Topic.

Unit:3	**Circuit characterization and performance estimation:**	**7Hours**

switch level RC delay models, Delay estimation, RC delay models, linear delay model, logical effort, parasitic delay, Delay in a logic gate, delay in a multistage logic networks, interconnect, design margin, Reliability, Scaling.

Contemporary Issues related to Topic.

Unit:4	**Combinational circuit design:**	**6 Hours**

Circuit families, static CMOS, Ratioed circuits, Cascode voltage switch logic, dynamic circuits, pass transistor circuits, differential circuits, sense amplifier circuits, BiCMOS circuits, power dissipation.

Contemporary Issues related to Topic.

Unit:5	**Sequential Circuit design:**	**6Hours**

Sequencing static circuits, Sequencing methods, Max-delay constraints, Min-delay constraints, Time borrowing, clock skew, circuit design of latches and Flip flops, static sequencing element methodology, Two phase timing types, characterizing sequencing element delays, sequencing dynamic circuits, Synchronizers. **Contemporary Issues related to Topic.**		
Unit :6	**Array subsystems:**	**6 Hours**
Static Random access memory, Dynamic random access memory, serial access memories, Content addressable memory Programmable logic arrays. **Contemporary Issues related to Topic**		
Total Lecture Hours		**39 Hours**

Textbooks	
1	Neil H. E. Weste, David F. Harris, A.Banerjee, "CMOS VLSI design: A Circuits and Systems Perspective", 4th Edition, Addison Wesley Publication, 2008
Reference Books	
1	Sung-Mo Kang and Yusuf Leblebici , CMOS Digital Integrated circuits Analysis and Design, 3rdedition, 2008,Tata Mc-Graw Hill
2	Pucknell and K. Eshraghian, CMOS VLSI Design, 3rd edition, 2005, Prentice Hall
YCCE e- library book links [ACCESSIBLE FROM COLLEGE CAMPUS]	
1	http://103.152.199.179/YCCE/Suported%20file/Supprted%20file/ecopies%20of%20books/Electronics%20and%20Telecommunication/cmos_kang.pdf
2	http://103.152.199.179/YCCE/Suported%20file/Supprted%20file/ecopies%20of%20books/Electronics%20Engineering/30.CMOS%20Logic%20Circuit%20Design%20%20(John%20P%20Uyemera).PDF
MOOCs Links and additional reading, learning, video material	
1	https://onlinecourses.nptel.ac.in/noc21_ee09
2	https://onlinecourses.nptel.ac.in/noc20_ee05/

I Semester

25VLSD103 – Lab CMOS Digital Circuit Design

Course Outcomes:
Upon successful completion of the course the students will be able to 1. Analyze the characteristics of CMOS inverter. 2. Analyze the static and dynamic characteristics of CMOS circuits. 3. Design combinational and sequential circuits. 4. Evaluate the performance of CMOS circuits.

Sr. No.	Experiments based on
1	a) V-I characteristics of NMOS transistor. b) V-I characteristics of PMOS transistor.
2	Design and simulate CMOS inverter.
3	Transfer characteristics of pseudo-NMOS inverter.
4	Design and simulate two input CMOS NAND gate
5	Layout design
6	Design of sequential circuits.
7	Calculation of delay
8	Determination of power
9	Circuit design using dynamic logic
10	Circuit design using pass transistor logic.

I Semester

25VLSD104 – Digital System Design

Course Outcomes:
Upon successful completion of the course the students will be able to 1. Model and test the Digital Designs using HDL 2. Analyze the timing issues in Digital Designs 3. Optimize the Digital Designs for area, power and delay 4. Implement the Digital Designs on FPGA and CPLD platforms

Unit:1	**Introduction to Verilog and Gate level modelling**	**7Hours**
Verilog as HDL, Levels of Design Description, Concurrency, Simulation and Synthesis, Functional Verification, System Tasks, Programming Language Interface (PLI), Module, Simulation and Synthesis Tools, AND Gate Primitive, Module Structure, Other Gate Primitives, Illustrative Examples, Tri-State Gates, Array of Instances of Primitives, Gate Primitives, Delays, Strengths and Contention Resolution, Net Types, Design of Basic Circuits. **Contemporary Issues related to Topic**		
Unit:2	**DATA FLOW MODELING**	**6 Hours**
Introduction, Continuous Assignment Structures, Delays and Continuous. Assignments, Assignment to Vectors, Operators. **Contemporary Issues related to Topic**		
Unit:3	**BEHAVIORAL MODELING**	**7 Hours**
Introduction, Operations and Assignments, Functional Bifurcation, Initial, Construct, Always Construct, Examples, Assignments with Delays, Wait, construct, Multiple Always Blocks, Designs at Behavioral Level, Blocking, and Non-blocking Assignments, The case statement, Simulation Flow .i*f* and i*f*-else constructs, assign-deassign construct, repeat construct, for loop, the disable construct, while loop, forever loop, parallel blocks, force-release construct, Event Contemporary Issues related to Topic		
Unit:4	**SWITCH LEVEL MODELLING**	**6 Hours**
Introduction, Basic Transistor Switches, CMOS Switch, Bi-directional, Gates, Time Delays with Switch Primitives, Instantiations with Strengths, and Delays, Strength Contention with Tri-reg Nets **Contemporary Issues related to Topic**		

Unit:5	FUNCTIONS , TASK AND PRIMITIVES	7 Hours
Introduction, Function, Tasks, User- Defined Primitives (UDP), FSM, Design (Moore and Mealy Machines). Introduction, Parameters, Path Delays, Module Parameters, System Tasks, and Functions, File-Based Tasks and Functions, Compiler Directives, Hierarchical Access, General Observations. Static RAM Memory, A simplified 486 Bus Model, UART Design **Contemporary Issues related to Topic**		
Unit :6	**IMPLEMENTATION USING FPGA & CPLD**	**6 Hours**
Xilinx 3000 Series FPGAs, Designing with FPGAs, Using a One-Hot State Assignment, Altera Complex Programmable Logic Devices (CPLDs),Altera FLEX 10K Series CPLDs. **Contemporary Issues related to Topic**		
Total Lecture Hours		**39 Hours**

Textbooks

1	Verilog Digital System Design Zainalabedin Navabi Second Edition, Tata McGraw Hill, 2009
2	A Verilog HDL Primer"J. Bhaskar,2nd Edition, Star Galaxy Press,1997

Reference Books

1	Digital Design : Principles and Practices 4th Edition, John F Wakerly, Pearson,2008

YCCE e- library book links [ACCESSIBLE FROM COLLEGE CAMPUS]

1	https://ycce.knimbus.com/portal/v2/default/home
2	Verilog HDL : A Guide to Digital, Design and Synthesis Samir Palnitkar 2nd Edition , Prentice Hall India, 2003

MOOCs Links and additional reading, learning, video material

1	https://archive.nptel.ac.in/courses/106/105/106105165/
2	https://onlinecourses.nptel.ac.in/noc24_cs61/

I Semester

25VLSD105 – Lab: Digital System Design

Course Outcomes:
Upon successful completion of the course the students will be able to
1. Design, develop, analyze and Implement combinational circuits using CAD tools 2. Design, develop , analyze and Implement sequential circuits using CAD tools

SN	Experiments based on
1	Modeling different types of gates: (a) 2-input NAND (b) 2-input OR gate (c) 2-input NOR gate (d) NOT gate (e) 2-input XOR gate (f) 2-input XNOR gate
2	Modeling (a) Half-adder (b) Full-adder
3	Modeling (a) 2-to-1 Multiplex (b) 2-to-4 Decoder (c) Tri-State Buffer.
4	Modeling a 4-bit PARALLEL ADDER
5	Modeling a 4-bit adder-subtractor circuit
6	Modeling Latch and Flip Flop
7	Modeling BCD counter
8	Modeling FSM
9	Modeling FIFO RAM.
10	Mini Project

I Semester

25VLSD106 – Embedded System and RTOS

Course Outcomes:
Upon successful completion of the course the students will be able to 1. Explore different technologies related to embedded systems 2. Effectively utilise the knowledge gained about RISC processor architecture and its instruction set for programming. 3. Explore the various real time systems with reference model. 4. Explore redundancy and various resource sharing mechanism.

Unit:1	**Overview of embedded systems**	**6 Hours**
Embedded Systems, Introduction, Design Metrics, Processor Technology, IC Technology, Design Technology, Design Productivity Gap, Custom Single purpose Processor Design, RT level design. **Contemporary Issues related to Topic**		
Unit:2	**Architectural Features Of RISC PROCESSORS**	**7 Hours**
The ARM processor - Register organization, Processor modes Exceptions and their handling, Memory-mapped I/Os, ARM and THUMB instruction sets, Addressing modes, programming examples. **Contemporary Issues related to Topic**		
Unit:3	**ARM7/9 Core**	**7 Hours**
H/W architecture, Timing diagrams for Memory access, Co-processor interface, Debug support, Scan chains, Embedded Real Time In Circuit Emulation (ICE), Hardware and software breakpoints. Buses: AMBA, Development tool like Compilers, Debuggers, IDE **Contemporary Issues related to Topic**		
Unit:4	**Introduction to RTOS**	**6 Hours**
Digital Controller, Air traffic flight control, Real time command and Controls, Low and High level Control, Signal Processing and Radar System, Hard Vs Soft Real Time Systems, Threads and Kernel, Real Time Application. **Contemporary Issues related to Topic**		
Unit:5	**Scheduling Algorithms :**	**7 Hours**
Clock Driven, Weighted Round Robin, Priority Driven, FIFO, Dynamic Vs State Systems, Effective Release Times		

and Dead Lines, Offline Vs Online Scheduling. **Contemporary Issues related to Topic**		
Unit :6	**Faults and Redundancy**	**6 Hours**
Fault Causes, Types, Detection of Fault. Redundancy: Hardware, Software, Time, Semaphore and Mutex , Message Queues, Interrupt Service Routines (ISR). **Contemporary Issues related to Topic**		
Total Lecture Hours		**39 Hours**

Textbooks	
1	Embedded System Design ,Frank Vahid and Tony Givargis, , 2002, 1st Edition, Wiley Publication
2	ARM System-on-Chip Architecture, Steve Furber 2nd Edition,2002, Pearson Education
3	Real Time Systems, 2013, Jane W.S. Liu , Pearson
Reference Books	
1	ARM System Developer's Guide: Designing and Optimizing, Sloss Andrew N, Symes Dominic, Wright Chris , Morgan Kaufman Publication
2	Real Time Systems, C.M.Krishna, Kang G. Shin, McGraw.Hill
3	Embedded System Design , Raj Kamal , 2003, Tata McGraw Hill
4	Embedded Real time systems: Concepts, Design & Programming, Black Book, Dr. K V K K Prasad, Dreamtech Press
YCCE e- library book links [ACCESSIBLE FROM COLLEGE CAMPUS]	
1	
2	
MOOCs Links and additional reading, learning, video material	
1	https://swayam.gov.in/explorer?searchText=embedded
2	Technical references and user manuals on www.arm.com

I Semester

– PE-I : Micro Electro Mechanical Systems

Course Outcomes:

Upon successful completion of the course the students will be able to

1. Design parallel and pipelining processing systems for speed, power and area optimization.
2. Implement the pipelined and parallel architectures using folding and unfolding techniques.
3. Apply algorithmic strength reduction techniques such as Fast Convolution algorithms and FDCT algorithms for increasing the speed of computation.
4. Design DSP algorithms with reduced numerical strength by sub expression sharing techniques.

Unit:1	Intrinsic Characteristic of MEMS	7 Hours

Energy Domains & Transducers. Sensors & Actuators. Introduction to Micro fabrication- silicon based MEMS processes. New Materials- Review of Electrical and Mechanical concepts in MEMS. Semiconductor devices- Stress & Strain analysis- Flexural beam bending, Torsional deflection

Contemporary Issues related to Topic

Unit:2	Electrostatic sensors	7 Hours

Parallel Plate capacitors, Applications, Interdigital Finger capacitor,Com drive devices, Thermal sensing and Actuation, Thermal Expansion, Thermal couples, Thermal resistors, Applications, Magnetic Actuators, Micro magnetic Components, Case studies of MEMS in magnetic actuators

Contemporary Issues related to Topic

Unit:3	Piezoelectric sensors and actuators	6 Hours

Piezo resistive sensors, Piezo resistive sensor materials, Stress analysis of mechanical elements, Applications to Inertia, Pressure, Acoustic, Tactile and Flow sensors, Piezoelectric sensors and actuators, Piezoelectric effects, Piezoelectric materials

Contemporary Issues related to Topic

Unit:4	Silicon Anisotropic Etching	7 Hours

Silicon Anisotropic Wet Etching, Dry Etching of Silicon, Plasma Etching, Deep reaction Ion Etching (DRIE), Isotropic Wet Etching, Gas phase Etchants-Case studies, Basic surface micromachining processes, Structural and sacrificial materials, Acceleration of sacrificial Etch, Striction and Anistriction methods, Assembly of 3D MEMS,Foundry process

Contemporary Issues related to Topic

Unit:5	**Polymer MEMS**	**6 Hours**
Polymers in MEMS ,Polimide, SU-8, Liquid Crystal Polymer(LCP), PDMS, PMMA, Parylene, Flurocarbon, Application to acceleration, Pressure, Flow and Tactile sensors **Contemporary Issues related to Topic**		
Unit :6	**Optical MEMS**	**6 Hours**
Optical MEMS, Lensens and Mirrors, Actuators for Active Optical MEMS. **Contemporary Issues related to Topic**		
Total Lecture Hours		**39 Hours**

Textbooks

1	Foundations of MEMS, Chang Liu, Pearson Education Inc, 2006.

Reference Books

1	An introduction to micro electro mechanical system design, NadimMaluf, Artech House,2000
2	The MEMS Handbook Mohames Gad-el-Hak, CRDC press , 2000

YCCE e- library book links [ACCESSIBLE FROM COLLEGE CAMPUS]

1	

MOOCs Links and additional reading, learning, video material

1	https://nptel.ac.in/courses/117105082

I Semester
25VLSD112 – PE I : Machine Learning for VLSI Design

Course Outcomes:

Upon successful completion of the course the students will be able to

1. Apply and analyze models using regression
2. Apply supervised and unsupervised learning for problem solving
3. Apply Machine learning algorithms for IC Manufacturing Yield Enhancement
4. Apply Machine Learning algorithm for VLSI Chip Testing

Unit:1	**Regression**	**7 Hours**

Supervised and Unsupervised Learning, Regression, Model and Cost Function, Gradient Descent, Multivariate Linear Regression, Feature Scaling, Gradient Descent for multivariable

Contemporary Issues related to Topic

Unit:2	**Classification**	**6 Hours**

Classification, Hypothesis Representation, Decision Boundary, Cost function and Gradient Descent, Multi-classification, Regularization, Model Evaluation

Contemporary Issues related to Topic

Unit:3	**Supervised Learning**	**7 Hours**

KNN, SVM, Decision tree, Naive Bayes Classifiers, Random Forest

Contemporary Issues related to Topic

Unit:4	**Unsupervised Learning**	**6 Hours**

K-means clustering, Hierarchical Clustering, DBSCAN Clustering, PCA, Anomaly Detection, Recommender System

Contemporary Issues related to Topic

Unit:5	**Machine Learning Approaches for IC Manufacturing Yield Enhancement**	**7 Hours**

Challenges: Imbalance classification and channel drift, Background of the Manufacturing Process, Mathematical formulations, Learning models such as Imbalanced Classification and Batch RUSBoost Learning, Online RUSBoost Learning, Incremental Learning for Concept Drift and Class Imbalance

Contemporary Issues related to Topic

Unit :6	**Machine Learning for VLSI Chip Testing**	**6 Hours**

Machine Learning for Chip Testing and Yield Optimization, Robust Spatial Correlation Extraction, Problem Formulations, Extraction Algorithms, Statistical Chip Testing and Yield Optimization, Statistical Test Margin Computation

Contemporary Issues related to Topic	
Total Lecture Hours	**39 Hours**

Textbooks	
1	Understanding Machine Learning. Shai Shalev-Shwartz and Shai Ben-David. Cambridge University Press.
2	The Elements of Statistical Learning. Trevor Hastie, Robert Tibshirani and Jerome Friedman, Second Edition
Reference Books	
1	Machine Learning: A Probabilistic Perspective, Kevin P. Murphy MIT Press
2	Machine learning An Algorithmic Perspective Second Edition Stephen Marsland, Chapman & Hall/CRC
YCCE e- library book links [ACCESSIBLE FROM COLLEGE CAMPUS]	
1	
MOOCs Links and additional reading, learning, video material	
1	https://onlinecourses.nptel.ac.in/noc23_cs18/preview
2	**https://onlinecourses.nptel.ac.in/noc24_ee146/preview**

I Semester

25VLSD113 – PEI: Advanced Computer Architecture

Course Outcomes:

Upon successful completion of the course the students will be able to

1. Demonstrate concepts of parallelism in hardware/software.
2. Discuss memory organization and mapping techniques.
3. Interpret performance of different pipelined processors.
4. Development of software to solve computationally intensive problems

Unit:1	Parallel Computer Models	7 Hours

Evolution of Computer architecture, system attributes to performance, Multi processors and multi computers, Multi-vector and SIMD computers, PRAM and VLSI models-Parallelism in Programming, conditions for Parallelism-Program Partitioning and Scheduling-program flow Mechanisms-Speed up performance laws-Amdahl's law, Gustafson's law-Memory bounded speedup Model.

Contemporary Issues related to Topic

Unit:2	Memory Systems and Buses	6 Hours

Memory hierarchy-cache and shared memory concepts-Cache memory organization-cache addressing models, Aliasing problem in cache, cache memory mapping techniques-Shared memory organization-Interleaved memory organization, Lower order interleaving, Higher order interleaving. Backplane bus systems-Bus addressing, arbitration and transaction.

Contemporary Issues related to Topic

Unit:3	Advanced Processors	7 Hours

Instruction set architectures-CISC and RISC scalar processors-Super scalar processors-VLIW architecture-Multivector and SIMD computers-Vector processing principles-Cray Y-MP 816 system-Inter processor communication

Contemporary Issues related to Topic

Unit:4	Multi Processor and Multi Computers	7 Hours

Modern multiprocessor systems use interconnects like crossbar switches and multiport memory, though they face the hot spot problem due to memory access contention. Message passing mechanisms enable communication between processors, while pipelined processor designs—including linear and non-linear pipelines—optimize performance through instruction and arithmetic pipelining, enhancing parallelism and throughput.

Contemporary Issues related to Topic

Unit:5	Data Flow Computers	6 Hours

Modern dataflow computer architectures include static and dynamic models enabling parallel, token-triggered execution widely used in AI and ML accelerators. VLSI computing structures like systolic arrays

support efficient matrix operations with rhythmic data movement **Contemporary Issues related to Topic**		
Unit :6	**VLSI Computations**	**6 Hours**
Fine-grain and coarse-grain reconfigurable arrays, energy-efficient VLSI arithmetic designs using approximate computing, bit-level and word-level parallelism in modern arithmetic units, on-chip and near-memory compute partitioning for large matrix handling, deep pipelining and dataflow execution in VLSI matrix engine **Contemporary Issues related to Topic**		
Total Lecture Hours		**39 Hours**

Textbooks	
1	Kai Hwang, Advanced Computer architecture Parallelism ,scalablity ,Programmablity , Mc Graw Hill,N.Y, 2003
2	Kai Hwang and F.A.Briggs, Computer architecture and parallel processor ' Mc Graw Hill, N.Y, 1999
Reference Books	
1	David A. Patterson and John L. Hennessey, ―Computer organization and design Elsevier, Fifth edition, 2014
2	www.sci.tamucc.edu/~sking/Courses/COSC5351/syllabus.php
YCCE e- library book links [ACCESSIBLE FROM COLLEGE CAMPUS]	
1	
2	
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1	https://archive.nptel.ac.in/content/syllabus_pdf/106103206.pdf

I Semester

25VLSD131 – PE II: Verification & Testing of VLSI Circuits

Course Outcomes:
Upon successful completion of the course the students will be able to 1. Analyze and explain the principles and significance of VLSI testing with respect to design verification, fault models, test pattern generation, fault coverage, and testing economics. 2. Interpret and utilize various design representations such as graphical models, binary decision diagrams, and net lists, and understand the VLSI design flow, including the use of CAD tools and design methodologies. 3. Perform logic and fault simulations, and apply automatic test pattern generation algorithms. 4. Assess and implement advanced testing methods.

Unit:1	**Overview Of Testing**	**7 Hours**
Design Process, Verification, Faults & Their Detection, Test Pattern Generation, Fault Coverage, Types Of Tests, Test Application, Testing Economics. Defects, Failures, and Faults: Physical Defects, Failures Modes, Faults, Fault Equivalence and Dominance, Fault Collapsing **Contemporary Issues related to Topic**		
Unit:2	**Design Representation**	**6 Hours**
Graphical representation, Graphs, Binary Decision diagrams, Netlists, VLSI Design Flow: CAD tools, Design Methodologies, Semicustom Design **Contemporary Issues related to Topic**		
Unit:3	**Simulation**	**7 Hours**
Logic Simulation, Approaches to Simulation, Fault Simulation & Their Results. Automatic Test Pattern Generation: D-Algorithm, Critical Path Extensions to D-Algorithm PODEM, FAN **Contemporary Issues related to Topic**		
Unit:4	**Ad Hoc Techniques**	**6 Hours**
Ad Hoc Techniques, Scan–Path Design, Test pattern generation, Test Pattern Application, Scan architectures, multiple scan chains, Partial Scan Testing **Contemporary Issues related to Topic**		
Unit:5	**Boundary-Scan Testing**	**7 Hours**
Boundary Scans Architecture, Test Access Port, Registers, Tap Controller, Modes of Operation. Built In Self Test: Pseudorandom Test Pattern Generation, Response Compaction, BIST Architectures **Contemporary Issues related to Topic**		

Unit :6	Memory Testing	6 Hours
Types of Memory Testing, Functional Testing Schemes, Testing FPGAs and Microprocessors: Testability Of FPGAs, Testing RAM- Based FPGAs, Testing Microprocessors, Synthesis For Testability. **Contemporary Issues related to Topic**		
Total Lecture Hours		**39 Hours**

	Textbooks
1	"Essentials of Electronic Testing for Digital, Memory, and Mixed-Signal VLSI Circuits",Michael L. Bushnell and Vishwani D. Agrawal, B.S.Publications, 2000
2	"Principles of Testing Electronic Systems", 2nd edition Samiha Mourad, Yervant Zorian
3	"Digital Systems Testing and Testable Design" ,Miron Abramovici, Melvin Breuer and Arthur Friedman, IEEE press
	Reference Books
1	"A Guide to VHDL" by Stanley Mazor,2nd Edition, Kluwer Academic Press, 2007
2	"HDL Chip Design" by Douglas Smith, 3rd Edition, Doone Publications, 2008 6. "Rapid Prototyping of Digital Systems", by J. O. Hamblen and M. Furman, Kluwer Academic Publishers.2001
	YCCE e- library book links [ACCESSIBLE FROM COLLEGE CAMPUS]
1	http://103.152.199.179/YCCE/Suported%20file/Supprted%20file/e-copies%20of%20books/Electronics%20Engineering/
2	http://103.152.199.179/YCCE/NPTEL%20VIDEOS%20PHASE%20I%20%20-%20PART3/Electronics%20and%20Communication%20Engineering/VLSI%20Design/
	MOOCs Links and additional reading, learning, video material
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I Semester

25VLSD132 - PE II: Advanced Nanotechnology

Course Outcomes:
Upon successful completion of the course the students will be able to 1. Analyze nanoelectronic concepts and evaluate how CMOS scaling influences device characteristics and performance.Analyze MOSFET I-V characteristics and evaluate the advantages of Silicon-On-Insulator (SOI) technology. 2. Assess the role of nanomaterials in enhancing the electrical and structural properties of electronic devices. 3. Apply the foundational principles of quantum mechanics to nanoscale systems and predict their influence on device behavior. 4. Compare Chemical Vapor Deposition (CVD) and Atomic Layer Deposition (ALD) techniques, and demonstrate their applications in fabricating thin films and nanostructures.

Unit:1	**Nanoscale Transistor Fundamentals and Design Challenges**	**7 Hours**
Introduction to Nanoelectronics, CMOS Technology scaling issues, Short channel effects, sub-threshold conduction, Drain Induced Barrier Lowering, Design techniques for nanoscale transistor. **Contemporary Issues related to Topic**		
Unit:2	**Electrical Characterization and Non-Classical MOSFETs**	**6 Hours**
MOS Electrical Characterization, Ideal MOS I-V Characteristics, Effects on non-idealities on I-V, MOS Parameter extraction, Overview of Non Classical MOSFETs and carrier transport in Nano MOSFETs, Ballistic Transport. **Contemporary Issues related to Topic**		
Unit:3	**SOI MOSFETs and Advanced Device Structures**	**7 Hours**
Silicon on Insulator (SOI) MOSFET, SOI technology comparison with bulk silicon CMOS Technology, Partially Depleted (PD) and Fully Depleted (FD) SOI-MOSFETs, Metal Semiconductor contacts and Metal-Source / Drain Junction MOSFETs. **Contemporary Issues related to Topic**		
Unit:4	**Alternative Channel Materials and Compound Semiconductor Devices**	**6 Hours**
Germanium and Compound semiconductor Nano MOSFETs, Germanium as alternative to silicon , Compound semiconductors, GaAs MESFETs types, Introduction to Nanomaterials. **Contemporary Issues related to Topic**		
Unit:5	**Quantum Mechanics and Nanomaterial Fabrication**	**7 Hours**
Quantum Mechanics and Quantum Statistics for considering nanomaterials, Basic principles of quantum mechanics , Energy bands in crystalline solids, Synthesis / Fabrication of Nanomaterials / structures, nanowires. **Contemporary Issues related to Topic**		

Unit :6	Nanostructures, Deposition Techniques, and Characterization	6 Hours
Chemical vapor deposition (CVD) and atomic layer deposition (ALD) , Carbon nanostrucutes, Characterization of Nanomaterials and Nanostructures **Contemporary Issues related to Topic**		
Total Lecture Hours		**39 Hours**

Textbooks	
1	Fundamentals of Modern VLSI Devices, Y. Taur and T. Ning, Cambridge University Press.
2	Nanotechnology (strategies, industry trends and applications, Jurgen Schulte,Willey,1 Edition, England 2005.
Reference Books	
1	
YCCE e- library book links [ACCESSIBLE FROM COLLEGE CAMPUS]	
1	http://link.springer.com/openurl?genre=book&isbn=978-1-4613-6193-0
MOOCs Links and additional reading, learning, video material	
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I Semester

25VLSD133 – PE II : Advanced Digital Signal Processing

Course Outcomes:

Upon successful completion of the course the students will be able to

1. Analyse discrete time signals.
2. Describe the multirate digital signal processing algorithms and applications.
3. Describe different linear predictive, optimum linear filters and adaptive filters.
4. Analyze the various nonparametric and parametric methods for power spectrum estimation.

Unit:1	Introduction to Digital Signal Processing	7 Hours

Review of Discrete time signals and systems and frequency analysis of discrete time linear time invariant systems, implementation of discrete time systems, correlation of discrete time systems Sampling, decimation by a factor 'D', Interpolation by a factor 'I', sampling rate conversion by a factor 'I/D', Implementation of sampling rate conversion, Multistage implementation of sampling rate conversion.

Contemporary Issues related to Topic

Unit:2	Multirate Digital Signal Processing	6 Hours

Multirate signal processing and its applications, Design of Digital filters, Design of FIR filters, Design of IIR filters, frequency transformations, Digital filter banks, two channel quadrature mirror filter banks, Mchannel QMF bank

Contemporary Issues related to Topic

Unit:3	Linear prediction and Optimum Linear Filters	7 Hours

Random signals, Correlation Functions and Power Spectra, Innovations Representation of a Stationary Random Process. Forward and Backward Linear Prediction. Solution of the Normal Equations. The Levinson-Durbin Algorithm. Properties of the Linear Prediction-Error Filters.

Contemporary Issues related to Topic

Unit:4	Applications of Adaptive Filters	6 Hours

Adaptive Channel Equalization, Adaptive noise cancellation, Linear Predictive coding of Speech Signals, Adaptive direct form FIR filters-The LMS algorithm, Properties of LMS algorithm. Adaptive direct form filters- RLS algorithm.

Contemporary Issues related to Topic

Unit:5	Non-Parametric Methods of Power Spectral Estimation	6 Hours
Estimation of spectra from finite duration observation of signals, Non-parametric Methods: Bartlett, Welch & Blackman - Tukey methods, Comparison of all Non-Parametric methods **Contemporary Issues related to Topic**		
Unit :6	**Parametric Methods of Power Spectrum Estimation**	**7 Hours**
Autocorrelation & Its Properties, Relation between auto correlation & model parameters, AR Models - Yule-Walker & Burg Methods, MA & ARMA models for power spectrum estimation, Finite word length effect in IIR digital Filters - Finite word-length effects in FFT algorithms. **Contemporary Issues related to Topic**		
Total Lecture Hours		**39 Hours**

Textbooks	
1	J.G.Proakis & D. G. Manolakis - Digital Signal Processing: Principles, Algorithms & Applications, 4th Ed., Pearson Education Publication.
2	Alan V Oppenheim & R. W Schaffer - Discrete Time Signal Processing, PHI
Reference Books	
1	Theory and Application of Digital Signal Processing by Lawrence R. Rabiner and Bernard Gold.
2	Mitra, Sanjit Kumar, and Yonghong Kuo. Digital signal processing: a computer-based approach. Volume 2. New York: McGraw-Hill Higher Education,
YCCE e- library book links [ACCESSIBLE FROM COLLEGE CAMPUS]	
1	
MOOCs Links and additional reading, learning, video material	
1	https://dss-kiel.de/index.php/teaching/lectures/lecture-advanced-digital-signal-processing
2	https://dss-kiel.de/index.php/teaching/lectures/lecture-advanced-digital-signal-processing

II Semester

25VLSD201 – Analog IC Design

Course Outcomes:
Upon successful completion of the course the students will be able to 1. Describe the basic concepts of MOS devices, amplifiers and converters. 2. Analyze MOS transistor and single stage amplifiers. 3. Analyze differential amplifiers and operational amplifiers 4. Analyze DAC, ADC and sigma delta converters.

Unit:1	**Basic MOS Device Physics**	**7 Hours**
Introduction to Analog IC Design, Threshold voltage, Derivation of I/V characteristics, second order effects, MOS device capacitance, MOS small signal models, MOS SPICE models **Contemporary Issues related to Topic**		
Unit:2	**Single stage amplifiers**	**6 Hours**
Basic concept, common source, common source stage with resistive load, common source with diode-connected , load CS stage with source degeneration, source follower, common gate Stage., Cascade Stage. **Contemporary Issues related to Topic**		
Unit:3	**Differential amplifiers**	**7 Hours**
Single ended & differential operation, Basic differential pair, qualitative and quantitative analysis, Common mode response **Contemporary Issues related to Topic**		
Unit:4	**Operational amplifiers**	**6 Hours**
General Considerations, Theory and Design, Performance Parameters, Single-Stage Op Amps, Two-Stage Op Amps, Design of 2-stage MOS Operational Amplifier, Gain Boosting, Comparison of various topologies, slew rate, Offset effects, PSRR. **Contemporary Issues related to Topic**		
Unit:5	**ADC converter and DAC converter**	**7 Hours**
Converting Analog Signals to Digital Signals, Sample and-Hold (S/H) Characteristics, Digital to Analog Converter (DAC) Specifications Analog -to-Digital Converter (ADC) Specifications **Contemporary Issues related to Topic**		
Unit :6	**Sigma Delta Converter**	**6 Hours**

The Oversampling ADC, The First-Order Sigma Delta Modulator, The Higher Order Sigma Delta modulator. **Contemporary Issues related to Topic**	
Total Lecture Hours	**39 Hours**

Textbooks	
1	Design of Analog CMOS Integrated Circuits, Nineteenth reprint2010, Behzad Razavi, Mc-Graw-Hill
2	CMOS circuit design, layout, and Simulation', Second edition, reprint 2009, Jacob Baker,WSE
Reference Books	
1	CMOS Analog Circuit Design, second edition, 2010, P.E. Allen, D.R.Holdberg, Oxford univ. press
2	Analysis and Design of Analog Integrated Circuits, fifth edition, reprint 2010, Paul B Gray , Hurst , Lewis, Meyer, John Wiley & sons
YCCE e- library book links [ACCESSIBLE FROM COLLEGE CAMPUS]	
1	http://103.152.199.179/YCCE/Suported%20file/Supprted%20file/e-copies%20of%20books/Electronics%20Engineering/14.Analog%20Design%20for%20CMOS%20VLSI%20Systems%20-%20(Franco%20Maloberti).pdf
MOOCs Links and additional reading, learning, video material	
1	https://archive.nptel.ac.in/courses/117/101/117101105/
2	https://archive.nptel.ac.in/courses/117/108/117108038/

II Semester

25VLSD202 –Lab Analog IC Design Lab

Course Outcomes:
Upon successful completion of the course the students will be able to 1. Analyze small signal model of MOS transistor &Perform analysis of single stage amplifiers with or without load. 2. Analyze small signal parameters of Differ Amplifier. 3. Analyze Performance parameters of CMOS op amp. 4. Analyze Performance parameters of converters

SN	Experiments based on
1	NMOS characteristic :- Vds Vs ID for various values of Vgs.
2	PMOS characteristic :- Vds Vs ID for various values of Vgs.
3	Common Source amplifier:- AC analysis Transient analysis
4	Common Drain amplifier:- AC analysis Transient analysis
5	Differential Amplifier :- AC analysis Transfer curve (Vin Vs Vout, DC condition)
6	Op-Amp Design: AC analysis Transient analysis DC analysis
7	SPICE simulation of basic Analog circuits, Analog Circuit simulation Verification of layouts.
8	Basic CMOS Comparator Design
9	Source Coupled Pair Differential Amplifier
10	Analysis of ADC, DAC , Sigma delta Convertor .
11	Mini Project

II Semester
25VLSD203 - VLSI Signal Processing

Course Outcomes:

Upon successful completion of the course the students will be able to

1. Analyze DSP algorithms and iteration bounds.
2. Apply pipelining, parallel processing, retiming, unfolding, and folding transformations to optimize DSP architectures for performance and power efficiency.
3. Design and optimize signal processing structures using algorithmic transformations such as Cook-Toom, Winograd, and cyclic convolution techniques.
4. Implement strength reduction techniques to improve the computational efficiency of digital filters and transforms in VLSI systems.

Unit:1	Introduction to DSP systems and Iteration Bound	7 Hours

Introduction to DSP systems – Typical DSP algorithms, Data flow and Dependence graphs - critical path, Loop bound, iteration bound, Algorithms for computing iteration bound

Contemporary Issues related to Topic

Unit:2	Pipelining , Parallel processing and Retiming	6 Hours

Pipelining and Parallel processing of FIR filters, Pipelining and Parallel processing for low power, Retiming – definitions and properties, solving systems of inequalities, retiming techniques.

Contemporary Issues related to Topic

Unit:3	Unfolding and Folding	7 Hours

Unfolding – an algorithm for unfolding, properties of unfolding, sample period reduction and parallel processing application, Folding transformation, Register minimization techniques

Contemporary Issues related to Topic

Unit:4	Fast convolution	6 Hours

Cook-Toom algorithm, modified Cook-Toom algorithm, winograd algorithm, iterated convolution, cyclic convolution

Contemporary Issues related to Topic

Unit:5	Algorithmic strength reduction in filters and transforms	6 Hours

2-parallel FIR filter, 2-parallel fast FIR filter, Two parallel fast FIR filter, Three parallel fast FIR filter, Parallel filter by transposition, DCT architecture, Inverse DCT architecture

Contemporary Issues related to Topic

Unit :6	Numerical strength reduction	7 Hours

Sub expression elimination, CSD representation, multiple constant multiplication, iterative matching, sub-expression sharing in digital filters, additive and multiplicative number splitting

Contemporary Issues related to Topic		
Total Lecture Hours		**39 Hours**
Textbooks		
1	VLSI Digital Signal Processing Systems: Design and Implementation, Keshab K. Parhi, John Wiley and Sons, 2007 1st Edition.	
Reference Books		
1	Digital Signal Processing with Field Programmable Gate Arrays, U. Meyer- Bease, 2nd edition 2004, Springer	
YCCE e- library book links [ACCESSIBLE FROM COLLEGE CAMPUS]		
1		
MOOCs Links and additional reading, learning, video material		
1	https://nptel.ac.in/courses/108105157	

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II Semester

25VLSD204 - RF Circuit Design

Course Outcomes:
Upon successful completion of the course the students will be able to 1. Analyze various Planar transmission lines and its characteristics. 2. Analyze various RF passive components, Power Devider, Directional Coupler and MIC filters. 3. Design RF Transistor Amplifier, power gain, Amplifier Stability and for Specified Gain 4. Design power amplifier. Perform measurements on mixer, Oscillator

Unit:1	**Planar Transmission Lines**	**7 Hours**
Introduction, Importance of Radio frequency Design, RF Behaviour of Passive Components, Chip Components, Transmission Line Analysis, Equivalent Circuit Representation, Transmission Line.Stripline, microstrip line, Suspended strip line and coplanar line; Parallel coupled lines in Stripline and microstrip – Analysis, Design and characteristics of Stripline and microstrip. **Contemporary Issues related to Topic**		
Unit:2	**RF Passive Devices**	**6 Hours**
Scattering Parameters Matching networks Single- and double-stub matching, Quarter wave transformer. The Smith Chart, From Reflection Coefficient to Load Impedance, Impedance Transformation, Admittance, Analysis and design of Stripline /microstrip components- Types of Branch line couplers, Power divider, Hybrid ring. **Contemporary Issues related to Topic**		
Unit:3	**MIC Filters**	**7 Hours**
An Overview of RF Filter Design, Basic Resonator and Filter Configurations. Lumped element filter design at RF. Impedance and Low pass scaling, Frequency transformation, High impedance/Low impedance low pass filter, Parallel coupled band pass filter, High pass filter, band stop filter. **Contemporary Issues related to Topic**		
Unit:4	**RF Active Circuits**	**6 Hours**
RF Transistor Amplifier Designs: Characteristics of Amplifiers, Amplifier Power Relations, Stability Considerations, Constant Gain, Noise Figure Circles, Constant VSWR Circles. **Contemporary Issues related to Topic**		
Unit:5	**RF Power Amplifier and Phase Detectors**	**7 Hours**
Introductions to RF Power Amplifiers, Classification of Power Amplifiers, Modulation of Power Amplifiers, Introduction to Phase lock loops, Linearized PLL Model, Phase Detector, Sequential Phase Detector. **Contemporary Issues related to Topic**		
Unit :6	**Oscillators & Mixers**	**6 Hours**
Oscillators, Basic Oscillator Model, High-Frequency Oscillator, Configuration, Colpitt"s oscillators Resonators, Tuned Oscillators, Negative resistance oscillators, Basic Characteristics of Mixers, Quadratic mixers, Multiplier based mixers, Single balanced and double balanced mixers, sub sampling mixers. **Contemporary Issues related to Topic**		

Total Lecture Hours		**39 Hours**
Textbooks		
1	B. Bhat & S.K. Koul, Stripline-like Transmission Line for Microwave Integrated Circuits, New Age Intl. (P)Ltd.	
2	RF Circuit Design – Theory and Applications", Reinhold Luduig and Pavel Bretchko, 2nd Edition, Pearson Education, 2000.	
3	D. M. Pozar, Microwave Engineering, John Wiley,1998.	
4	B.Razavi, "RF Microelectronics", Pearson Education, 1997	
5	Thomas H. Lee , The Design of CMOS Radio-Frequency Integrated Circuits, Second Edition, , CAMBRIDGE,1998	
Reference Books		
1	B.Razavi, "Design of Analog CMOS Integrated Circuits", McGraw Hill, 2001	
2	RF Circuit Design Theory and Applications, 2nd Edition, R. Ludwig & P. Bretchko, Pearson Publication.	
3	G. Gonzalez, Microwave Transistor Amplifiers Analysis and Design, Prentice Hall, 1997	
4	Renhold Ludwig and Pavel, Bretchko , RF Circuits Design, Prentice Hall	
YCCE e- library book links [ACCESSIBLE FROM COLLEGE CAMPUS]		
1	http://103.152.199.179/YCCE/yccelibrary.html	
2	http://103.152.199.179/YCCE/Suported%20file/Supprted%20file/e-copies%20of%20books/Electronics%20Engineering/81.microwave-devices-and-circuits-samuel-liao.pdf	
3	http://103.152.199.179/YCCE/yccelibrary.html	
MOOCs Links and additional reading, learning, video material		
1	https://youtu.be/KUDGGsyh1Hs	
2	https://youtu.be/ZZEZUysFPDY	
3	https://www.digimat.in/nptel/courses/video/117102012/L01.html	
4	NPTEL Course on CMOS RF Integrated Circuits by Dr. S. Chatterjee, IIT Delhi,	

II Semester

25VLSD205 – Lab RF Circuit Design

Course Outcomes:
Upon successful completion of the course the students will be able to 1. Apply Smith Chart techniques for RF circuit development. *(Apply – Level 3) 2. Analyze impedance matching networks and passive RF filters. (Analyze – Level 4) 3. Design high-frequency and RF power amplifiers for RF applications. (Create – Level 6) 4. Utilize CAD tools for RF circuit simulation and design.

SN	Experiments based on
1	To design Low Pass, Band Stop Filters
2	To design Band Pass Filters
3	To design Band Stop Filters
4	To design Branch line Coupler
5	To design Power Divider
6	To design Hybrid ring Coupler
7	To design differential Amplifier.
8	To design the series RLC circuit. and To design parallel RLC circuit.
9	To design L-C Filter (Low Pass Filter by using lumped element).
10	To design of power BJT amplifier.

II Semester

25VLSD206 - Synthesis & Optimization of VLSI Circuits

Course Outcomes:

Upon successful completion of the course the students will be able to

1. Describe Boolean functions, representations, and CAD-based synthesis and optimization issues.
2. Analyze and solve algorithms for behavioral synthesis including scheduling, allocation, and binding.
3. Evaluate high-level synthesis techniques and optimize logic at two-level, multilevel, and sequential stages.
4. Apply the concept of satisfiability (SAT) in synthesis and optimization contexts.

Unit:1	Graph-Theoretic Foundations	7 Hours

Microelectronics, Semiconductor technologies and circuit taxonomy, Microelectronic design styles, Computer aided synthesis and optimization. Graphs Notation, Undirected graphs, Directed graphs, Combinatorial optimization, Algorithms, Tractable and intractable problems Graph optimization problems and algorithms, Boolean algebra and Applications.

Contemporary Issues related to Topic

Unit:2	Hardware Modeling	6 Hours

Hardware Modeling Languages, Distinctive features, Structural hardware language, Behavioral hardware language, HDLs used in synthesis, Abstract models, Structures logic networks, State diagrams, Data flow and sequencing graphs, Compilation and optimization techniques.

Contemporary Issues related to Topic

Unit:3	Logic Optimization and Boolean Minimization	7 Hours

Logic optimization, principles, Operation on two level logic covers, Algorithms for logic minimization, Symbolic minimization and encoding property, Minimization of Boolean relations. Multiple level combinational optimizations, Models and transformations

Contemporary Issues related to Topic

Unit:4	Combinational and Sequential Circuit optimization	6 Hours

Combinational networks, Algebraic model, Synthesis of testable network, Algorithm for delay evaluation and optimization, Rule based system for logic optimization. Sequential circuit optimization, Sequential circuit optimization using state based models, Sequential circuit optimization using network models.

Contemporary Issues related to Topic

Unit:5	Scheduling and Library Binding	7 Hours

A model for scheduling problems, Scheduling with resource and without resource constraints, Scheduling algorithms for extended sequencing models, Scheduling Pipe lined circuits. Cell library binding, Problem formulation and

analysis, Algorithms for library binding, Specific problems and algorithms for library binding (lookup table F.P.G.As and Antifuse based F.P.G.As), Rule based library binding. **Contemporary Issues related to Topic**		
Unit :6	**Advanced Trends and Future Directions**	**6 Hours**
Ongoing work in logic Synthesis, Speedup Algorithms Design Reuse, Domain Specific Synthesis, Testability, Future role of Logic Synthesis **Contemporary Issues related to Topic**		
Total Lecture Hours		**39 Hours**

Textbooks	
1	"Synthesis and Optimization of Digital Circuits" ,Giovanni De Micheli, 1st Edition, Tata McGraw-Hill, 2003.
Reference Books	
1	"Logic Synthesis" SrinivasDevadas, AbhijitGhosh, and Kurt Keutzer,1st Edition, McGraw-Hill, USA, 1994.
2	VHDL for Programmable Logic," Kevin Skahill, 1st Edition, Pearson Education, 2000.
YCCE e- library book links [ACCESSIBLE FROM COLLEGE CAMPUS]	
1	http://103.152.199.179/YCCE/yccelibrary.html
MOOCs Links and additional reading, learning, video material	
1	https://nptel.ac.in/courses/108103108
2	https://archive.nptel.ac.in/noc/courses/noc18/SEM1/noc18-ec06/
3	https://archive.nptel.ac.in/courses/108/103/108103108/
4	https://onlinecourses.nptel.ac.in/noc22_cs109/preview

II Semester

25VLSD211 - PEIII VLSI for Wireless Communication

Course Outcomes:

Upon successful completion of the course the students will be able to

1. Learn new related technologies in the fields of telecommunication and wireless networks along with the concepts of that require advanced knowledge within the field.
2. Analyze the function and design principles of receiver front-end components, including low-noise amplifiers (LNAs).
3. Designing and optimizing mixers, particularly the Gilbert cell mixer.
4. Learn Analog to Digital Converters and PLL.

Unit:1	Communication Concept	7 Hours
Generation of wireless networks, Wireless systems, Standards, Access methods, Modulation schemes, Classical channel, Wireless Channel Description, Path Loss, Multipath Fading, Channel Model and Envelope Fading, Frequency Selective and Fast Fading **Contemporary Issues related to Topic**		
Unit:2	**Transmitter/Receiver Architecture**	**6 Hours**
Transmitter backend, Quadrature LO generator, Receiver Front End: Filter Design ,Receiver frond end, Filter design, non idealities and design parameters, deviation of Noise Figures. **Contemporary Issues related to Topic**		
Unit:3	**Low Noise Amplifiers (LNA)**	**7 Hours**
Matching networks, Wideband LNA Design: DC Bias,Gain and Frequency Response,Noise Figure, Narrowband LNA Design: Impedance matching, Narrowband LNA, Narrowband LNA Core Amplifiers: Noise figure, Power Dissipation,Trade off Between Noise figure and power. **Contemporary Issues related to Topic**		
Unit:4	**Active & Passive Mixers**	**6 Hours**
Balancing: unbalanced mixer,single balanced mixer,Double balanced mixer, Qualitative description of Gilbert Mixer, Conversion gain , noise, Passive mixer :switching mixer, noise, , Distortions in unbalanced switching Mixers and conversion gain. **Contemporary Issues related to Topic**		
Unit:5	**Analog to Digital Converters**	**7 Hours**

Demodulators, A/D converters Used in a Receiver, Low-Pass Sigma-Delta Modulators, Implementation of Low-Pass Sigma-Delta Modulators, Bandpass Sigma-Delta Modulators, Implementation of Bandpass Sigma-Delta Modulators. **Contemporary Issues related to Topic**		
Unit :6	**Frequency Synthesizers**	**6 Hours**
PLL Based Frequency Synthesizer, Phase detector and charge pump, VCO, Dividers, Ring oscillators, Loop filter, General description, Design approaches **Contemporary Issues related to Topic**		
Total Lecture Hours		**39 Hours**

Textbooks	
1	Bosco Leung, "VLSI for Wireless Communication, Second Edition, Springer,2011
2	Wen-Chih Kan,"VLSI Architecture for High-capacity Wireless Communications", University of Minnesota, 2007
Reference Books	
1	Emad N Farag, M.I Elmasry, "Mixed Signal VLSI Wireless Design Circuits and Systems", Kluwer Publications, 2013.
2	David Tsee, Pramod Viswanath," Fundamentals of Wireless Communication", Cambridge Univ Press, 2005.
YCCE e- library book links [ACCESSIBLE FROM COLLEGE CAMPUS]	
1	
MOOCs Links and additional reading, learning, video material	
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II Semester

25VLSD212 - PEIII ASIC Design

Course Outcomes:
Upon successful completion of the course the students will be able to 1. Apply ASIC design methodologies and use programmable logic cells to implement digital functions. 2. Analyze the back-end physical design flow including partitioning, floor-planning, placement, and routing. 3. Demonstrate theoretical understanding sufficient for performing FPGA and ASIC design tasks.

Unit:1	Introduction to ASIC and Data Path Design	7 Hours
Introduction to ASICs: Full custom, Semi-custom and Programmable ASICs, ASIC Design flow, ASIC cell libraries. CMOS Logic: Data path Logic Cells: Data Path Elements, Adders: Carry skip, Carry bypass, Carry save, Carryselect, Conditional sum, Multiplier (Booth encoding), Data path Operators, I/O cells, Cell Compilers **Contemporary Issues related to Topic**		
Unit:2	**ASIC Libraries and Programmable Logic Architectures**	**7 Hours**
ASIC Library Design: Logical effort: Predicting Delay, Logical area and logical efficiency, Logical paths, Multi stage cells, Optimum delay and number of stages, library cell design. Programmable ASIC Logic Cells: MUX as Boolean function generators, Acted ACT: ACT 1, ACT 2 and ACT 3 Logic Modules, Xilinx LCA:XC3000 CLB, Altera FLEX and MAX, Programmable ASIC I/O Cells: Xilinx and Altera I/O Block. **Contemporary Issues related to Topic**		
Unit:3	**Low-Level ASIC Design Entry and Netlist Representation**	**6 Hours**
Low-level design entry: Schematic entry: Hierarchical design, The cell library, Names, Schematic Icons & Symbols, Nets, Schematic Entry for ASICs, Connections, vectored instances & buses, Edit in place, attributes, Netlist screener. **Contemporary Issues related to Topic**		
Unit:4	**ASIC Physical Design and Partitioning Algorithms**	**6 Hours**
ASIC Construction: Physical Design, CAD Tools System partitioning, Estimating ASIC size. Partitioning: Goals and objectives, Constructive Partitioning, Iterative Partitioning Improvement, KL, FM and Look Ahead algorithms. **Contemporary Issues related to Topic**		
Unit:5	**Mixed-Signal ASIC Blocks: Sigma-Delta Modulators**	**7 Hours**

Demodulators, A/D converters Used in a Receiver, Low-Pass Sigma-Delta Modulators, Implementation of Low-Pass Sigma-Delta Modulators, Bandpass Sigma-Delta Modulators, Implementation of Bandpass Sigma-Delta Modulators. **Contemporary Issues related to Topic**		
Unit :6	**ASIC Routing and Design Rule Verification**	**6 Hours**
Routing: Global Routing: Goals and objectives, Global Routing Methods, Global routing between blocks, Back-annotation. Detailed Routing: Goals and objectives, Measurement of Channel Density, Left-Edge Algorithm, Area-Routing Algorithms, Multilevel routing, Timing –Driven detailed routing, Final routing steps, Special Routing, Circuit extraction and DRC. **Contemporary Issues related to Topic**		
Total Lecture Hours		

Textbooks	
1	Michael John Sebastian Smith, "Application - Specific Integrated Circuits", Addison- Wesley Professional, 2005
2	Neil H.E. Weste, David Harris, and Ayan Banerjee, "CMOS VLSI Design: A Circuits and Systems Perspective", Addison Wesley/ Pearson education 3rdedition, 2011
Reference Books	
1	Vikram Arkalgud Chandrasetty, "VLSI Design: A Practical Guide for FPGA and ASIC Implementations" Springer, ISBN: 978-1-4614-1119-2. 2011
2	Rakesh Chadha, Bhasker J, "An ASIC Low Power Primer", Springer, ISBN: 978-14614-4270-7.
3	Peter J. Ashenden Digital Design (Verilog): An Embedded Systems Approach Using Verilog,1st Edition, Kindle Edition
YCCE e- library book links [ACCESSIBLE FROM COLLEGE CAMPUS]	
1	
MOOCs Links and additional reading, learning, video material	
1	https://www.youtube.com/watch?v=oZSv68esbgI
2	https://www.youtube.com/watch?v=4cPkr1VHu7Q

II Semester

25VLSD213 - PEIII CMOS Subsystem Design

Course Outcomes:
Upon successful completion of the course the students will be able to 1. Describe MOSFET fundamentals, fabrication process, and layout design rules. 2. Analyze performance issues and trade-offs in CMOS subsystem design. 3. Identify relationships among process parameters, device structure, circuit performance, and system-level design. 4. Use analog design tools and software for CMOS circuit simulation. 5. Design CMOS-based VLSI subsystems.

Unit:1	**MOS Devices and Electrical Modeling**	**7 Hours**
Material Model Electrical Properties, Junction Diode. MOS transistor Operation Modes Threshold Voltage: Metal and Polysilicon Trapped Charge Implants Strong Inversion: Charge Modeling Constant Vtmodel: NMOS/PMOS transistors. I/V characteristics, Sign Conventions parasitic Bipolar Transistors CMOS Latch-up Analysis (D.C. and transient), **Contemporary Issues related to Topic**		
Unit:2	**Capacitance, Charge Storage, and Fabrication Processes**	**6 Hours**
Device capacitance and Charge Storage in MOS NMOS/CMOS circuit analysis, Small signal amplifier model Miller Effect. Layout /Fabrication, Diffusion / Implants / Wires, NMOS / CMOS Processes **Contemporary Issues related to Topic**		
Unit:3	**SCMOS Design Rules and Layout Techniques**	**6 Hours**
SCMOS Design Rules – special derivation self-aligned processes Resistor / Capacitor Layout, Logic Level Design, Cube Decomposition, Realization of Duals for CMOS Euler path layout, Topological Considerations. Don't Cares and Redundancy, layout Parasitic Reduction **Contemporary Issues related to Topic**		
Unit:4	**MOS Logic Families and Performance Optimization**	**7 Hours**
MOS Logic Families: Propagation Delay for CMOS/NMOS/PNMOS, Layout Capacitance / Resistance. Estimation; Gain effects; MOS Performance Estimation, Buffers/Capacitive Loading, Power Dissipation: Transient Optimization, Sidewall/2-d and 3-d effects: Cross-talk Fringing, Ball-park numbers for process Estimation Scaling CMOS Design Optimization: High- Speed Logic Strategies **Contemporary Issues related to Topic**		

Unit:5	**Interconnects, Clocking, and Advanced Logic Styles**	**7 Hours**
Interconnection. Distributed R/C cross/talk, Noise, Clocking Strategies, Sub-System Design and Partitioning Dynamic Logic, Dynamic Circuits, Stored Charge and timing. Domino Logic, Switched Capacitor and Charge Flow circuits, pass-Transistor logic (CPL). **Contemporary Issues related to Topic**		
Unit :6	**Data-Path and Memory Circuit Design**	**6 Hours**
Data-Path and Memory Circuits: Static/Dynamic memories, Ancillary memory Analog Circuits. Advance topics on VLSI Design **Contemporary Issues related to Topic**		
Total Lecture Hours		**39 Hours**

Textbooks	
1	Weste, "Principles of CMOS VLSI Design (2ndedition)"
2	Dougles A. Pucknell and kamran Eshraghian, "Basic VLSI Systems and Circuits, Prentice Hall of India Pvt. Ltd.1993.
3	Wayne Wolf, "Modern VLSI Design, 2nd Edition". Prentice Hall 1998.
Reference Books	
1	
YCCE e- library book links [ACCESSIBLE FROM COLLEGE CAMPUS]	
1	
MOOCs Links and additional reading, learning, video material	
1	

II Semester

25VLSD231 - PEIV Mixed Signal VLSI Design

Course Outcomes:

Upon successful completion of the course the students will be able to

1. Interpret the operation of MOSFETs and analyze the relationship between process technology and modeling in analog integrated circuit design.
2. Apply Mixed signal VLSI concepts to design MOS circuits.
3. Analyze CMOS digital circuits and provide exposure to the complex, non-digital behavior of the devices and circuits

Unit:1	Introduction to Mixed Signal	7 Hours

Introduction to Mixed Signal VLSI System, Signal and Filters, digital comb filter, the z-plane, simple digital filters, Sampling and Aliasing

Contemporary Issues related to Topic

Unit:2	Data Converter	6 Hours

Data Converter SNR: Effective number of bits ,Clock jitter, Interpolating filters for DACs, Band pass and High pass Sync filters, Using feedback to improve SNR.

Contemporary Issues related to Topic

Unit:3	Sub-Micron CMOS circuit design	7 Hours

Sub-Micron CMOS circuit design : Process flow, capacitors and resistors, MOSFET Switch, Delay and Adder elements

Contemporary Issues related to Topic

Unit:4	Implementing Data converters	6 Hours

Current mode and voltage mode R-2R DAC, Using Op-Amps in data converters, Implementing ADCs, Cyclic ADC, Cyclic ADC, pipeline ADC

Contemporary Issues related to Topic

Unit:5	Integrator Based CMOS Filters:	7 Hours

Integrator Building Blocks, Low pass and Active R-C filters, MOSFET-C integrators, gm-C Integrators, Discrete time integrator

Contemporary Issues related to Topic

Unit :6	Bilinear and Bi-quadratic transfer functions	6 Hours
Active R-C Trans conductor-C and Switched Capacitor implementations both transfer functions, Canonic form of a digital filter. **Contemporary Issues related to Topic**		
Total Lecture Hours		**39 Hours**

Textbooks	
1	"CMOS – Mixed signal circuit design, layout and simulation", R. Jacob Baker, "2nd Edition a. IEEE Press and Wiley Interscience, 2002.
2	"CMOS Circuit Design, Layout, and Simulation", Third Edition, R. Jacob Baker
Reference Books	
1	"Design of Analog CMOS Integrated circuits", B. Razavi, 1st Edition, McGraw Hill, 2001
2	"CMOS Analog Circuit Design", P.E. Allen and D.R. Holberg, 2nd Edition, Oxford University Press, 2002.
YCCE e- library book links [ACCESSIBLE FROM COLLEGE CAMPUS]	
1	http://103.152.199.179/YCCE/Suported%20file/Supprted%20file/e-copies%20of%20books/Electronics%20Engineering/29.CMOS%20Circuit%20Design%20Layout%20and%20Simulation_2nd_Baker.pdf
MOOCs Links and additional reading, learning, video material	
1	

II Semester

25VLSD232 - PEIV Advanced VLSI Design

Course Outcomes:

Upon successful completion of the course the students will be able to

1. Analyze the design and performance aspects of fast CMOS circuits.
2. Describe arithmetic circuit implementations and apply low-power design techniques.
3. Analyze the impact of scaling, buffer insertion, inductive peaking, and capacitive coupling on CMOS circuit performance.
4. Describe the architecture and design principles of MMIPS and finite state machines (FSMs).
5. Design and test CMOS-based digital circuits using modern tools

Unit:1	**Emerging Trends and High-Speed CMOS Design**	**7 Hours**
Future trends in VLSI circuit and system design, A way of designing fast CMOS circuits. **Contemporary Issues related to Topic**		
Unit:2	**Low-Power CMOS Design and Arithmetic Implementation**	**6 Hours**
Power Estimation and control in CMOS circuit, Low power design techniques, Arithmetic implementation of CMOS circuits. **Contemporary Issues related to Topic**		
Unit:3	**Interconnect Design and Scaling Challenges**	**7 Hours**
Impact of scaling, buffer insertion, inductive peaking, capacitive coupled interconnects **Contemporary Issues related to Topic**		
Unit:4	**Processor Architectures and System Partitioning**	**6 Hours**
FSM and datapath, Single cycle MMIPS, Multicycle MMIPS, Netlist and system partitioning **Contemporary Issues related to Topic**		
Unit:5	**VLSI Testing and Built-In Self-Test for Mixed-Signal Circuits**	**7 Hours**
Introduction to VLSI Testing, Design for test, Built in self-test for analog and mixed signal blocks **Contemporary Issues related to Topic**		
Unit :6	**Design Verification and Model Checking in High-Level Synthesis**	**6 Hours**
Introduction to Design Verification, Equivalence /model checking for HLS Design. **Contemporary Issues related to Topic**		
Total Lecture Hours		**39 Hours**
Textbooks		

1	Advanced VLSI Design and Testability Issues Edited By Suman Lata Tripathi, Sobhit Saxena, Sushanta Kumar Mohapatra
2	CMOS VLSI Design : A circuits and systems perspective 5th edition 2023
Reference Books	
1	Advanced VLSI Technology Technical Questions with Solutions by Cherry Bhargava, Lovely Professional University, India Gaurav Mani Khanal, University of Rome Tor Vergata, Italy
YCCE e- library book links [ACCESSIBLE FROM COLLEGE CAMPUS]	
1	
MOOCs Links and additional reading, learning, video material	
1	https://archive.nptel.ac.in/courses/117/101/117101004/

II Semester

25VLSD233 – PEIV Low Power VLSI Design

Course Outcomes:

Upon successful completion of the course the students will be able to

1. Describe power reduction strategies and evaluate existing low-power VLSI design approaches.
2. Apply the different components of power consumption and their estimation method to MOS circuits
3. Analysis of Low-Power Circuits, low power circuit synthesis and extending the low power design to different Applications.
4. Analyse advanced issues in VLSI systems, specific to the deep-submicron silicon technologies, such as Short-Channel-Effect, leakage problem

Unit:1	**Low Power CMOS VLSI Design**	**7 Hours**

Need for low power VLSI chips, Sources of power dissipation: Short circuit dissipation, dynamic dissipation, designing Techniques for low power. Physics of power dissipation in MOSFET devices, MOS Capacitance analysis, low power figure of merits, brief overview of low power VLSI design limits

Contemporary Issues related to Topic

Unit:2	**Power Estimation**	**6 Hours**

Probabilistic power analysis: random logic signals, probability and frequency, probabilistic power analysis techniques, signal entropy, Low power circuits: transistor and gate sizing, equivalent pin ordering, network reconstruction and reorganization, Glitching Power, special latches and flip-flops.

Contemporary Issues related to Topic

Unit:3	**Sequential Circuit Design**	**7 Hours**

Behavioural, Logic and circuit level approaches. Algorithm level transforms. Circuit activity driven architectural transformations, voltage scaling, operation reduction and substitution, pre-computation, Logic: gate reorganization, signal gating, logic encoding, state machine encoding.

Contemporary Issues related to Topic

Unit:4	**Deep Submicron Transistor Design**	**6 Hours**

Design style, Leakage current in Deep sub-micron transistors, device design issues, minimizing short channel effect. Low voltage design techniques using reverse Vgs. Steep sub threshold swing and multiple threshold voltages. Multiple threshold CMOS based on path critically, multiple supply voltages.

Contemporary Issues related to Topic

Unit:5	**Energy computing**	**7 Hours**

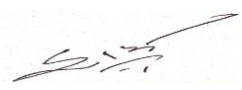
Low energy computing, Energy dissipation in transistor channel. Energy recovery circuit design, designs with reversible and partially reversible logic, energy recovery in adiabatic logic and SRAM core, Design of peripheral circuits – address decoder, level shifter and IO Buffer, supply clock generation **Contemporary Issues related to Topic**		
Unit :6	**Software Power Optimization**	**6 Hours**
Introduction, sources of software power dissipation, power estimation and optimization. Co-design for low power. **Contemporary Issues related to Topic**		
Total Lecture Hours		**39 Hours**

Textbooks	
1	K.Roy and S.C. Prasad, LOW POWER CMOS VLSI circuit design, Wiley, 2000
Reference Books	
1	Dimitrios Soudris, Chirstian Pignet, Costas Goutis, DESIGNING CMOS CIRCUITS FOR LOW POWER, Kluwer, 2002.
2	Low-Power CMOS Circuits-Technology, Logic Design and CAD Tools" Christian Piguet, 2006 by Taylor & Francis Group, LLC
YCCE e- library book links [ACCESSIBLE FROM COLLEGE CAMPUS]	
1	http://103.152.199.179/YCCE/yccelibrary.html
MOOCs Links and additional reading, learning, video material	
1	https://archive.nptel.ac.in/courses/106/105/106105034/
2	https://archive.nptel.ac.in/courses/106/105/106105034/
3	https://nptel.ac.in/courses/106105034

III Semester

25VLSD301

Project Phase-I

		June, 2025	1.00	Applicable for AY 2025-26 Onwards
Chairperson	Dean (Acad. Matters)	Date of Release	Version	

IV Semester

25VLSD401

Project Phase-II