Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

(Accredited 'A++' Grade by NAAC with a score of 3.6)

Hingna Road, Wanadongri, Nagpur - 441 110

Bachelor of Technology

SoE & Syllabus 2025

(Department of Electronics Engineering)

B.Tech Honors in VLSI Design & Embedded System

Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B.Tech SCHEME OF EXAMINATION 2025-26

(Department of Electronics Engineering)

SoE No. 25EE-VLSI-101

B.Tech Honors in VLSI Design & Embedded System

SN	Sem	Type	Sub. Code	Subject	T/P	Contact Hours				Credits	% Weightage			ESE Duration Hours
						L	T	P	Hrs		MSEs*	TA**	ESE	
1	V	PC	25EEH501	CMOS VLSI Design	T	3	0	0	3	3	30	20	50	3
2	V	PC	25EEH502	Embedded System	T	3	0	0	3	3	30	20	50	3
3	V	PC	25EEH503	Embedded & CMOS Lab	P	0	0	2	2	1		60	40	
4	VI	PC	25EEH601	Introduction to FinFET	T	3	0	0	3	3	30	20	50	3
5	VI	PC	25EEH602	VLSI Scripting Language	T	3	0	0	3	3	30	20	50	3
6	VI	PC	25EEH603	**Lab :** VLSI Scripting Language	P	0	0	2	2	1		60	40	
7	VII	PC	25EEH701	RTL to GDSII	T	3	0	0	3	3	30	20	50	3
8	VII	PC	25EEH702	Project Lab :RTL to GDSII	P	0	0	2	2	1		60	40	
				TOTAL		**15**	**0**	**6**	**21**	**18**				

		Jun-25	**1.00**	**Applicable for AY 2025-26 Onwards**
Chairperson	**Dean (Acad. Matters)**	**Date of Release**	**Version**	

V SEMESTER
25EEH501: CMOS VLSI Design

Course Outcomes:

Upon successful completion of the course the students will be able to

1. Describe and interpret the basic concepts of MOS transistors.
2. Construct digital CMOS circuits as per specifications.
3. Analyze inverter design, characteristics, and Performance parameters of CMOS Circuits.
4. Design and implement combinational and sequential circuits using different CMOS styles

Unit:1	Introduction of CMOS	**7 Hours**
Introduction of MOSFETs: CMOS Fabrication Process steps, NMOS Enhancement Transistor, MOS Transistor Operations, PMOS Enhancement Transistor, Regions of Operations, Threshold Voltage, MOS Device Equations.		
Unit:2	Logic Design With CMOS	**7 Hours**
Logic Design with MOSFETs: Ideal Switches and Boolean Operations, MOSFETs as Switches, Basic Logic Gates in CMOS, Compound Gates in CMOS, Transmission Gate Circuits (TG), Pass Transistor.		
Unit:3	CMOS inverter	**7 Hours**
MOS inverter Characteristics: Resistive load inverter, Inverters with n type MOSFET load, CMOS inverter, Principle of operation, DC characteristics, Tristate Inverter, Noise Margin, Introduction to BiCMOS Inverter		
Unit:4	Combinational circuit design	**6 Hours**
Static CMOS, Ratioed Logic circuits, Analysis of CMOS Logic Gates: MOS Device Capacitance, Switching Characteristics, Rise Time, Fall Time, Propagation Delay, Power Dissipation in CMOS, Fanin, Fan-out, Complex Logic Structures, Complementary Static CMOS, Pseudo NMOS Logic, Dynamic CMOS Logic, CMOS Domino Logic, CMOS Pass Transistor Logic		
Unit:5	Sequential Circuit Design	**7 Hours**
Sequential Circuit Design, Latches and Flip Flops: D-latch, S-R latch and flip flop, J-K latch and flip flop.		
Unit :6	Data path VLSI System Component	**7 Hours**

Data path VLSI System Components: Half and full adder, half and full subtractor, Comparators, barrel shifters, Multiplexers, Demultiplexer, Binary Decoders, Equality Detectors, Priority Encoders	
Total Lecture Hours	**41 Hours**

Text books	
1	Neil H. E. Weste Harris, Principle of CMOS VLSI Design, 4th Edition, Addison Wesley VLSI Series.
Reference Books	
1	John P. Uyemura, Introduction to VLSI Circuits and Systems, Students Edition, Wiley Publication.
2	Sung-Mo Kang, Yusuf leblebici, CMOS VLSI Design, Third edition, 2008, Tata McGraw Hill.
YCCE e- library book links [ACCESSIBLE FROM COLLEGE CAMPUS]	
1	http://103.152.199.179/YCCE/yccelibrary.html
MOOCs Links and additional reading, learning, video material	
1	https://nptel.ac.in/courses/108107129
2	https://nptel.ac.in/courses/106103116
3	https://nptel.ac.in/courses/117106092

V SEMESTER
25EEH502: Embedded System

Course Outcomes:		
Upon successful completion of the course the students will be able to 1. Describe the ARM microprocessor architectures, its features and instructions. 2. Write program for specific task. 3. Analyze and Interface the peripherals to ARM based microcontroller. 4. Develop embedded system application using ARM based microcontroller.		
Unit:1	Introduction to ARM, Advantages of architectural features of ARM Processor, Processor modes, Register organization, Exceptions and its handling, 3/5- stage pipeline ARM organization	**7 Hours**
Unit:2	ARM and THUMB instruction sets, ARM programmer's model, addressing modes, Instruction set in detail and programming, data processing instruction, data transfer instruction, Control flow instructions, simple assembly language programs.	**7 Hours**
Unit:3	ARM assembly language programs and C language programs. Code conversion programs.	**7 Hours**
Unit:4	LPC 2148 architecture block diagrams, pins and signals. GPIO, I / O Interfaces like LED and Switch and their Programs.	**6 Hours**
Unit:5	Display interfacing with LPC 2148. 7segment display interfacing. LCD interfacing and programs.	**7 Hours**
Unit :6	LPC 2148 TIMER and PWM Applications. Embedded ARM applications	**7 Hours**
	Total Lecture Hours	**41 Hours**

Text books	
1	ARM System on-chip Architecture, 2nd edition, 2000, Steve Furber, Pearson Education Asia
2	Embedded Linux, Hardware, Software and interfacing, 2002. Craig Hallabaugh, Addison Wesley Professional
3	ARM System Developer's Guide: Designing and Optimizing, 2005 Sloss Andrew N, Symes Dominic, Wright Chris Morgan Kaufman Publication
Reference Books	
1	Technical references on www.arm.com
YCCE e- library book links [ACCESSIBLE FROM COLLEGE CAMPUS]	
1	http://172.16.1.9/LocalGuru/listLectures.php?cid=29086f3420285fdf&bid=927d7542627865a3
MOOCs Links and additional reading, learning, video material	
1	https://nptel.ac.in/courses/106105159
2	https://nptel.ac.in/courses/106105193

V SEMESTER
25EEH503: Embedded & CMOS Lab

Course Outcomes:
Upon successful completion of the course the students will be able to 1. Design and implement basic digital logic gates and combinational circuits using CMOS technology. 2. Develop and test assembly language programs to perform arithmetic, logical operations on ARM-based microcontrollers. 3. Interface and control basic peripherals like LEDs and LCDs using LPC2148 microcontroller. 4. Integrate hardware and software knowledge to simulate and debug digital and embedded systems.

Sr. No.	Experiments based on
1	To implement NAND and NOR gate using CMOS
2	To implement different Functions using CMOS
3	To implement Function MUX and DMUX using CMOS
4	To implement NAND and NOR gate S-R flip-flop using CMOS logic.
5	To implement Full adder using CMOS
6	Write a program in assembly language to perform arithmetic and logical operations on two 16 bits numbers.
7	Compare two strings of 3 ASCII characters, One string starts at 0x40000000 and other at 0x40000010. If both the string match store 11H in memory location 0x40000030 otherwise store 22H in memory location 0x40000030.
8	Draw Interfacing of LED with LPC2148 and write program to blink LED connected to port pin P0.7 of LPC2148
9	Draw interfacing of LCD 16x2 with LPC2148 and write program to display your FIRST NAME in first line.
10	Draw Interfacing of LED with LPC2148 and Write program to blink 8 LEDs alternately connected to port pins P1.16 to P1.23 of LPC2148

VI Semester
25EEH601: Introduction to FinFET

Course Outcomes:		
Upon successful completion of the course the students will be able to 1. Understand the fundamental principles of Metal-Oxide-Semiconductor (MOS) 2. Analyze the operation of MOSFETs 3. Interpret MOSFET SPICE models to simulate the behavior of MOS transistors and diodes in circuit design. 4. Analyze the device operation of FinFETs, including drain current formulation.		
Unit:1	MOS Capacitors	**7 Hours**
Introduction of Metal-Oxide-Semiconductor, Energy Band Diagram of MOS Capacitors, Second Order Effects in MOS Capacitors, C–V of MOS capacitor		
Unit:2	MOSFET and Application	**7 Hours**
Introduction of MOSFET, I-V and C-V Characteristics of MOSFETs, Capacitance Modeling for HF & LF, High and Low Frequency Modeling in Bulk MOSFET, MOSFET as Switch and Amplifier		
Unit:3	MOSFET SPICE Models	**7 Hours**
Introduction to MOSFET SPICE Models, - Discuss Various SPICE Models equations, SPICE Models for the MOS Transistor, The SPICE Diode Models		
Unit:4	Semiconductor Heterostructures	**6 Hours**
Introduction, Carriers and Transport, Band Diagram of Heterostructure, PN Heterojunction Diode, Properties and Application		
Unit:5	FinFET	**7 Hours**
Introduction to FinFET, FinFET Manufacturing Technology, Bulk-FinFET Fabrication, SOI FinFET Process Flow, Long Channel FinFETs, Basic Features of FinFET Devices		
Unit :6	FinFET Device Technology:	**7 Hours**
FinFET Device Operation, Drain Current Formulation, Small Geometry FinFETs: Physical Effects on Device Performance, Short-channel Effects on Threshold Voltage, Quantum Mechanical Effects, Surface Mobility, High Field Effects		
	Total Lecture Hours	**41 Hours**

Text books	
1	Physics of Semiconductor Devices: S. M. Sze, Wiley Eastern, (1981).
Reference Books	
1	CMOS Circuit Design, Layout and simulation: J. Baker, D.E. Boyce., IEEE press

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2	Semiconductor physics and Devices, Donald Neamen, McGraw-Hill, 3rd edition
3	Modern Semiconductor Devices for Integrated Circuits, Chenming Hu, Prentice Hall, 2010.
YCCE e- library book links [ACCESSIBLE FROM COLLEGE CAMPUS]	
1	http://103.152.199.179/YCCE/yccelibrary.html
MOOCs Links and additional reading, learning, video material	
1	https://www.chu.berkeley.edu/modern-semiconductor-devices-for-integrated-circuits-chenming-calvin-hu-2010/
2	https://www.youtube.com/watch?v=LdPcJIIvVfY
3	https://www.youtube.com/watch?app=desktop&v=YssB6YR0fTg&t=917s

VI Semester
25EEH602:VLSI Scripting Language

Course Outcomes:		
Upon successful completion of the course the students will be able to **1**.Understand the basic syntax and structure of TCL scripting language. 2.Apply control structures and procedures in TCL for writing modular code. 3.Analyze and process file data using TCL for automation tasks in EDA tools. 4. Design and develop TCL scripts to automate workflows in VLSI tools.		
Unit:1	**Introduction to TCL Language**	**7 Hours**
History and features of TCL,Structure of TCL script,Running TCL scripts in different environments Variables and data types, Basic syntax: puts, gets, expr		
Unit:2	**Control Statements and Loops**	**7 Hours**
Conditional constructs: if, elseif, else, Loop constructs: while, for, foreach, switch statements,Script writing using control structures		
Unit:3	**Procedures and File Handling**	**7 Hours**
Defining and invoking procedures (proc), Arguments and return values,File operations: open, read, write, close,Error handling and file parsing,parsing netlist files		
Unit:4	**TCL Lists, Arrays, and Strings**	**6 Hours**
List creation and manipulation, Array declarations and operations, String manipulation commands Practical examples in design automation script		
Unit:5	**TCL in EDA Tool Automation (VLSI Focus)**	**7 Hours**
TCL in EDA tools, Automating tool flows (e.g., synthesis, simulation, layout),Writing constraint and configuration scripts,TCL with shell commands and tool APIs		
Unit :6	**Project and Case Studies**	**7 Hours**
Mini project: Automating a synthesis/EDA task using TCL,Case study: Using TCL in Xilinx Vivado or Synopsys,Best practices in TCL scripting,Debugging and optimization of scripts.		
	Total Lecture Hours	**41 Hours**

Text books	
1	Programming and GUI Fundamentals: TCL-TK for Electronic Design Automation (EDA), Suman Lata Tripathi , Abhishek Kumar, Jyotirmoy Pathak
Reference Books	

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1	**TCL Scripting for Electronic Design Automation (EDA) – Xilinx & Cadence tool guides**
2	Practical Programming in Tcl and Tk – Brent B. Welch, Ken Jones
3	Tool Command Language (TCL): Scripting for EDA Tools – Synopsys Documentation/User Manuals
YCCE e- library book links [ACCESSIBLE FROM COLLEGE CAMPUS]	
1	http://103.152.199.179/YCCE/yccelibrary.html
MOOCs Links and additional reading, learning, video material	
1	https://www.youtube.com/playlist?list=PL1h5a0eaDD3rsGDFnVki_fFEtDWQfXjca

VI Semester
25EEH603:Lab : VLSI Scripting Language

Course Outcomes:
Upon successful completion of the course the students will be able to 1. Understand the fundamental syntax, structure, and features of Tcl scripting language. 2. Apply Tcl control structures, procedures, and data handling techniques to develop modular scripts. 3. Analyze file input/output operations and implement Tcl scripts for parsing and processing data. 4. Design and develop Tcl scripts to automate VLSI design flows using industry-standard EDA tools.

Sr. No.	Experiments based on
1	Write a basic Tcl script using variables, expressions, and print statements
2	Implement conditional statements (if, else) and loops (for, while) in Tcl
3	Develop a Tcl procedure to perform arithmetic operations and call it with arguments
4	Create and manipulate lists and arrays using Tcl commands
5	Write a Tcl script to read data from a text file and perform basic parsing (e.g., count lines)
6	Generate and write output to a file using Tcl scripting
7	Automate synthesis flow in **Xilinx Vivado** using Tcl script (project creation, add files)
8	Write a Tcl script to generate a constraint file (e.g., clock constraints) for a VLSI design
9	Automate simulation setup using Tcl (e.g., ModelSim or Vivado simulation launch)
10	**Mini Project**: Develop an end-to-end Tcl script to automate synthesis, simulation, and report generation in an EDA tool

VII Semester
25EEH701: RTL to GDSII

Course Outcomes:

Upon successful completion of the course the students will be able to

1: Describe the structure, fabrication steps, types, and design methodologies of Integrated Circuits, and explain the complete VLSI design flow from system specification to GDSII.

2: **Model** digital systems using Verilog HDL and **analyze** simulation results using testbenches, functional coverage, and waveform inspection techniques.

3: **Apply** RTL synthesis and logic optimization techniques, and **evaluate** the correctness of the design using formal verification and static timing analysis.

4: **Implement** power-aware and testable digital designs, and **analyze** physical design steps including placement, routing, and sign-off checks such as DRC, LVS, and STA.

Unit:1	Basic Concepts of Integrated Circuit: Structure, Fabrication, Types, Design Styles, Designing vs. Fabrication, Economics, Figures of Merit. Overview of VLSI Design Flow: Design Flows and Abstraction; Pre-RTL Methodologies: Hardware-software Partitioning, SoC Design, Intellectual Property (IP) Assembly, Behavioral Synthesis. Overview of VLSI Design Flow: RTL to GDS Implementation: Logic Synthesis, Physical Design; Verification and Testing; Post-GDS Processes	**7 Hours**
Unit:2	Hardware Modelling: Introduction to Verilog Functional verification using simulation: testbench, coverage, mechanism of simulation in Verilog. RTL Synthesis: Verilog Constructs to Hardware Logic Optimization: Definitions, Two-level logic optimization: Multi-level logic optimization, FSM Optimization Formal	**7 Hours**
Unit:3	Verification: Introduction, Formal Engines: BDD, SAT Solver. Formal Verification: Model Checking, Combinational Equivalence Checking Technology Library: Delay models of Combinational and Sequential Cells.	**7 Hours**
Unit:4	Static Timing Analysis: Synchronous Behaviour, Timing Requirements, Timing Graph, Mechanism, Delay Calculation, Graph-based Analysis, Path-based Analysis, Accounting for Variations. Constraints: Clock, I/O, Timing Exceptions Technology Mapping Timing-driven Optimizations	**6 Hours**
Unit:5	Power Analysis, Power-driven Optimizations Design for Test: Basics and Fault Models, Scan Design Methodology. Design for Test: ATPG, BIST Basic Concepts	**7 Hours**

	for Physical Design: IC Fabrication, FEOL, BEOL, Interconnects and Parasitics, Signal Integrity, Antenna Effect, LEF files	
Unit :6	Chip Planning: Partitioning, Floorplanning, Power Planning Placement: Global Placement, Wirelength Estimates, Legalization, Detailed Placement, Timing-driven Placement, Scan Cell Reordering, Spare Cell Placement. Clock Tree Synthesis: Terminologies, Clock Distribution Networks, Clock Network Architectures, Useful Skews Routing: Global and Detailed, Optimizations Physical Verification: Extraction, LVS, ERC, DRC, ECO and Sign-off.	**7 Hours**
	Total Lecture Hours	**41 Hours**

Text books	
1	Sneh Saurabh, "Introduction to VLSI Design Flow", Cambridge University Press, 2023 https://www.cambridge.org/highereducation/books/introduction-to-vlsi-design-flow/93E6832E63FE6B795181D6D67B552333#overview
Reference Books	
1	M.J.S. Smith, "Application-specific integrated circuits", Addison-Wesley, 1997
2	L. Lavagno, I. L. Markov, G. Martin, and L. K. Scheffer (Editors), "Electronic Design Automation for IC Implementation, Circuit Design, and Process Technology", CRC Press, 2016
3	S. Palnitkar, "Verilog HDL: a guide to digital design and synthesis", Pearson Education India, 2003
4	M. Bushnell and V. Agrawal, "Essentials of electronic testing for digital, memory and mixed-signal VLSI circuits", Springer Science & Business Media, 2004
MOOCs Links and additional reading, learning, video material	
1	https://onlinecourses.nptel.ac.in/noc25_ee106

VII Semester
25EEH702: Project Lab :RTL to GDSII

Course Outcomes:
Upon successful completion of the course the students will be able to 1. Design, simulate, and verify a digital circuit using Verilog. 2. Apply timing and power analysis 3. Apply optimization techniques to meet design specifications. 4. Implement a design for test (DFT) methodology for a given digital circuit.

Sr. No.	Experiments based on
1	FPGA Tools & Simulation: Setup, basic HDL simulation.
2	Design and Implementation of High Speed Adders
3	Design and Implementation of Multiplers
4	Design and Implementation of Comparators
5	Design and Implementation of Code Converters
6	Design and Implementation of Parity Checkers
7	Design and Implementation of Flip Flops
8	Design and Implementation of Counters
9	Design and Implementation of Shift Register