

Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

(Accredited 'A++' Grade by NAAC with a score of 3.6)

Hingna Road, Wanadongri, Nagpur - 441 110



Bachelor of Technology

SoE & Syllabus 2023

1st to 6th Semester

(Department of Electronics Engineering)

B. Tech in VLSI



Nagar Yuwak Shikshan Sanstha's
Yeshwantrao Chavan College of Engineering
 (An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)
B.TECH SCHEME OF EXAMINATION 2023
 (Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)
B. Tech in V.L.S.I.

SoE No.
23VLSI-101

S N	Sem	Type	BoS/ Deptt	Sub. Code	Subject	T/P	Contact Hours				Credits	% Weightage			ESE Duration Hours
							L	T	P	Hrs		MSEs*	TA**	ESE	
FIRST SEMESTER (GROUP-B)															
1	1	BS	GE	23GE1102	Differential Equations, Matrices and Statistics	T	3	0	0	3	3	30	20	50	3
2	1	BS	GE	23GE1108	Engineering Physics	T	3	0	0	3	3	30	20	50	3
3	1	BS	GE	23GE1109	Lab: Engineering Physics	P	0	0	2	2	1		60	40	
4	1	BES	EE	23EE1101	Basic Electronics	T	3	0	0	3	3	30	20	50	3
5	1	BES	EE	23EE1102	Lab : Basic Electronics	P	0	0	2	2	1		60	40	
6	1	BES	EL	23EL1102	Basic Electrical Engineering	T	3	0	0	3	3	30	20	50	3
7	1	PC	EE	23EE1103	Digital Logic Design	T	3	0	0	3	3	30	20	50	3
8	1	PC	EE	23EE1104	Lab : Digital Logic Design	P	0	0	2	2	1		60	40	
9	1	VSEC	GE	23GE1117	Get Set Go	2		60	40	
10	1	CC2	GE		Liberal Learning Course (LLC2)	2		60	40	
TOTAL FIRST SEM								0	6	21	22				
MANDATORY LEARNING COURSES															
1	1	HS		GE2131	Universal Human Values (UHV)	A	2	0	0	2	0				
SECOND SEMESTER (GROUP-B)															
1	2	BS	GE	23GE1201	Calculus and Vector	T	3	0	0	3	3	30	20	50	3
2	2	BS	GE	23GE1204	Applied Chemistry	T	3	0	0	3	3	30	20	50	3
3	2	BS	GE	23GE1205	Lab: Applied Chemistry	P	0	0	2	2	1		60	40	
4	2	HS/AEC1	GE	23GE1212	Professional Communication	T	2	0	0	2	2	30	20	50	2
5	2	HS/IKS	GE	23GE1215	Indian Knowledge System	T	2	0	0	2	2	30	20	50	2
6	2	BES	EE	23EE1205	Electronics Device and Circuit	T	3	0	0	3	3	30	20	50	3
7	2	BES	EE	23EE1206	Lab: Electronics Device and Circuit	P	0	0	2	2	1		60	40	
8	2	BES	IT	23IT1203	Programming for Problem Solving	T	2	0	0	2	2	30	20	50	2
9	2	BES	IT	23IT1204	Lab: Programming for Problem Solving	P	0	0	2	2	1		60	40	
10	2	VSEC	GE	23GE1218	Functional English	2		60	40	
11	2	CC1	GE		Liberal Learning Course (LLC1)	2		60	40	
TOTAL SECOND SEM							15	0	6	21	22				

Liberal Learning Course

S N	Sem	Type	BoS/ Deptt	Sub. Code	Subject
1	2	CC2	GE	23LLC1201	Music (Vocal)
2	2	CC2	GE	23LLC1202	Music (Instrumental)
3	2	CC2	GE	23LLC1203	Indian Classical Dance
4	2	CC2	GE	23LLC1204	Other forms of Dances
5	2	CC2	GE	23LLC1205	Painting
6	2	CC2	GE	23LLC1206	Theatre and acting
7	2	CC2	GE	23LLC1207	Photography
8	2	CC2	GE	23LLC1208	Yoga
9	2	CC2	GE	23LLC1209	Chess
10	2	CC2	GE	23LLC1210	Athletics
11	2	CC2	GE	23LLC1211	Basket Ball
12	2	CC2	GE	23LLC1212	Judo
13	2	CC2	GE	23LLC1213	Elements of Japanese Language
14	2	CC2	GE	23LLC1214	Elements of German Language
15	2	CC2	GE	23LLC1215	Elements of French Language
16	2	CC2	GE	23LLC1216	Elements of Spanish Language
17	2	CC2	GE	23LLC1217	Basics of Vedic Maths
18	2	CC2	GE	23LLC1218	Skilling in Microsoft Visio and Inkscape



Nagar Yuwak Shikshan Sanstha's
Yeshwantrao Chavan College of Engineering
 (An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)
B.TECH SCHEME OF EXAMINATION 2023
 (Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)
B. Tech in V.L.S.I.

SoE No.
23VLSI-101

S N	Sem	Type	BoS/ Deptt	Sub. Code	Subject	T/P	Contact Hours				Credits	% Weightage			ESE Duration Hours
							L	T	P	Hrs		MSEs*	TA**	ESE	

Liberal Learning Course

S N	Sem	Type	BoS/ Deptt	Sub. Code	Subject
1	1	CC1	GE	23LLC1101	Music (Vocal)
2	1	CC1	GE	23LLC1102	Music (Instrumental)
3	1	CC1	GE	23LLC1103	Indian Classical Dance
4	1	CC1	GE	23LLC1104	Other forms of Dances
5	1	CC1	GE	23LLC1105	Painting
6	1	CC1	GE	23LLC1106	Theatre and acting
7	1	CC1	GE	23LLC1107	Photography
8	1	CC1	GE	23LLC1108	Yoga
9	1	CC1	GE	23LLC1109	Chess
10	1	CC1	GE	23LLC1110	Athletics
11	1	CC1	GE	23LLC1111	Basket Ball
12	1	CC1	GE	23LLC1112	Judo
13	1	CC1	GE	23LLC1113	Elements of Japanese Language
14	1	CC1	GE	23LLC1114	Elements of German Language
15	1	CC1	GE	23LLC1115	Elements of French Language
16	1	CC1	GE	23LLC1116	Elements of Spanish Language
17	1	CC1	GE	23LLC1117	Basics of Vedic Maths
18	1	CC1	GE	23LLC1118	Skilling in Microsoft Visio and Inkscape

MSEs* = Two MSEs of 15 Marks each will conducted and marks of these 2 MSEs will be considered for Continuous Assessment

TA ** = for Theory : TA1-5 marks on Proctored Online Exam, TA2-12 marks on activities decided by course teacher, TA3 - 3 marks on class attendance

TA = for Practical : MSPA will be 15 marks each**

		July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's
Yeshwantrao Chavan College of Engineering
 (An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)
B.TECH SCHEME OF EXAMINATION 2023
 (Scheme of Examination w.e.f. 2023-24 onward)
 (Department of Electronics Engineering)
B. Tech Electronics Engineering(VLSI Design and Technology)

SoE No.
23VLSI-101

SN	Sem	Type	BoS/ Deptt	Sub. Code	Subject	T/P	Contact Hours				Credits	% Weightage			ESE Duration Hours
							L	T	P	Hrs		MSEs*	TA**	ESE	
THIRD SEMESTER															
1	3	HSSM-1	GE	23GE1301	Fundamentals of Management & Economics	T	2	0	0	2	2	30	20	50	3
2	3	PC	EE	23VLS1301	Analog Circuits	T	3	0	0	3	3	30	20	50	3
3	3	PC	EE	23VLS1302	Lab : Analog Circuits	P	0	0	2	2	1		60	40	
4	3	PC	EE	23VLS1303	Network Analysis	T	3	0	0	3	3	30	20	50	3
5	3	PC	EE	23VLS1304	Lab : Network Analysis	P	0	0	2	2	1		60	40	
6	3	PC	EE	23VLS1305	Signal and Systems	T	3	0	0	3	3	30	20	50	3
7	3	VEC-2	EE	23VLS1306	Basics of Python Programming	T	2	0	0	2	2	30	20	50	3
8	3	CEP	EE	23VLS1307	Community Engagement Project	P	0	0	2	4	2		60	40	
9	3	OE-1	OE		Open Elective-I	T	2	0	0	2	2	30	20	50	3
10	3	MDM	MDM		MD Minor Course-I	T	2	0	0	2	2	30	20	50	3
TOTAL							17	0	6	25	21				

List of Mandatory Learning Course (MLC)

1	3	HS	T&P	MLC2123	YCAP3 : YCCE Communication Aptitude Preparation	A	3	0	0	3	0				
---	---	----	-----	---------	---	---	---	---	---	---	---	--	--	--	--

Open Elective - I

SN	Sem	Type	BoS / Deptt	Sub. Code	Subject
1	3	OE1	GE	23OE1301	OE-I : Combinatorics
2	3	OE1	GE	23OE1302	OE-I : Fuzzy Set Theory, Arithmetic And Logic
3	3	OE1	GE	23OE1303	OE-I : Green Chemistry & Sustainability
4	3	OE1	GE	23OE1304	OE-I : Hydrogen Fuel
5	3	OE1	GE	23OE1305	OE-I : Electronic Materials And Applications
6	3	OE1	GE	23OE1306	OE-I : Laser Technology And Applications
7	3	OE1	MGT	23OE1307	OE-I : Finance And Cost Management
8	3	OE1	MGT	23OE1308	OE-I : Operation Research Techniques
9	3	OE1	MGT	23OE1309	OE-I : Project Evaluation & Management
10	3	OE1	MGT	23OE1310	OE-I : Total Quality Management
11	3	OE1	MGT	23OE1311	OE-I : Value Engineering
12	3	OE1	MGT	23OE1312	OE-I : Maintenance Management
13	3	OE1	MGT	23OE1313	OE-I : Industrial Safety
14	3	OE1	MGT	23OE1314	OE-I : Industry 4.0
15	3	OE1	MGT	23OE1315	OE-I : Operation Management
16	3	OE1	MGT	23OE1316	OE-I : Material Management
17	3	OE1	MGT	23OE1317	OE-I : Hospitality Management
18	3	OE1	MGT	23OE1318	OE-I : Human Resource Management & Organizational Behaviour
19	3	OE1	MGT	23OE1319	OE-I : Agri-Business Management
20	3	OE1	MGT	23OE1320	OE-I : Rural Marketing
21	3	OE1	MGT	23OE1321	OE-I : Marketing Management
22	3	OE1	MGT	23OE1322	OE-I : Health Care Management
23	3	OE1	MGT	23OE1323	OE-I : Designated approved online NPTEL/KKSU Course
24	3	OE1	MGT	23OE1324	OE-I : Indian Archeology
25	3	OE1	MGT	23OE1325	OE-I : Social & Positive Psychology
26	3	OE1	MGT	23OE1326	OE-I : Seismology & Earthquake

		July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's
Yeshwantrao Chavan College of Engineering
 (An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)
B.TECH SCHEME OF EXAMINATION 2023
 (Scheme of Examination w.e.f. 2023-24 onward)
 (Department of Electronics Engineering)
B. Tech Electronics Engineering(VLSI Design and Technology)

SoE No.
23VLSI-101

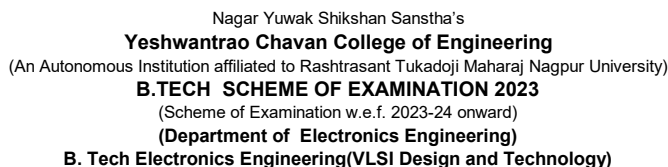
SN	Sem	Type	BoS/ Deptt	Sub. Code	Subject	T/P	Contact Hours				Credits	% Weightage			ESE Duration Hours
							L	T	P	Hrs		MSEs*	TA**	ESE	
FOURTH SEMESTER															
1	4	BS	GE	23GE1404	Probability Theory and Sampling Theory	T	3	0	0	3	3	30	20	50	3
2	4	HSSM-2	GE	23GE1401	Entrepreneurship Development	T	2	0	0	2	2	30	20	50	3
3	4	AEC-2	GE	23GE1405 23GE1406	Marathi Language / Hindi Language	T	2	0	0	2	2	30	20	50	3
4	4	VEC-1	CV	23CV1411	Environmental Sustainability, Pollution and Management	T	2	0	0	2	2	30	20	50	3
5	4	PC	EE	23VLS1401	Microcontrollers and Computer Architecture	T	3	0	0	3	3	30	20	50	3
6	4	PC	EE	23VLS1402	Lab : Microcontrollers and Computer Architecture	P	0	0	2	2	1		60	40	
7	4	PC	EE	23VLS1403	Lab : Workshop Lab	P	0	0	2	2	1		60	40	
8	5	PC	EE	23VLS1404	Control System Engineering	T	3	0	0	3	3	30	20	50	3
9	4	VSEC-3	EE	23VLS1405	Lab : PCB design or CAD	P	0	0	2	4	2		60	40	
10	4	OE-2	OE		Open Elective-II	T	2	0	0	2	2	30	20	50	3
11	4	MDM	EE		MD Minor Course-II	T	2	0	0	2	2	30	20	50	3
TOTAL							19	0	6	27	23				

List of Mandatory Learning Course (MLC)															
1	4	HS	T&P	MLC2124	YCAP4 : YCCE Communication Aptitude Preparation	A	3	0	0	3	0				

Open Elective - II

SN	Sem	Type	BoS/ Deptt	Sub. Code	Subject
1	4	OE2	GE	23OE2401	OE-II : Combinatorics
2	4	OE2	GE	23OE2402	OE-II : Fuzzy Set Theory, Arithmetic And Logic
3	4	OE2	GE	23OE2403	OE-II : Green Chem. & Sustainability
4	4	OE2	GE	23OE2404	OE-II : Hydrogen Fuel
5	4	OE2	GE	23OE2405	OE-II : Electronic Materials And Applications
6	4	OE2	GE	23OE2406	OE-II : Laser Technology And Applications
7	4	OE2	MGT	23OE2407	OE-II : Finance And Cost Management
8	4	OE2	MGT	23OE2408	OE-II : Operation Research Techniques
9	4	OE2	MGT	23OE2409	OE-II : Project Evaluation & Management
10	4	OE2	MGT	23OE2410	OE-II : Total Quality Management
11	4	OE2	MGT	23OE2411	OE-II : Value Engineering
12	4	OE2	MGT	23OE2412	OE-II : Maintenance Management
13	4	OE2	MGT	23OE2413	OE-II : Industrial Safety
14	4	OE2	MGT	23OE2414	OE-II : Industry 4.0
15	4	OE2	MGT	23OE2415	OE-II : Operation Management
16	4	OE2	MGT	23OE2416	OE-II : Material Management
17	4	OE2	MGT	23OE2417	OE-II : Hospitality Management
18	4	OE2	MGT	23OE2418	OE-II : Human Resource Management & Organizational Behaviour
19	4	OE2	MGT	23OE2419	OE-II : Agri-Business Management
20	4	OE2	MGT	23OE2420	OE-II : Rural Marketing
21	4	OE2	MGT	23OE2421	OE-II : Marketing Management
22	4	OE2	MGT	23OE2422	OE-II : Health Care Management
23	4	OE2	MGT	23OE2423	OE-II : Designated approved online NPTEL/KKSU Course
24	4	OE2	MGT	23OE2424	OE-II : Indian Archeology
25	4	OE2	MGT	23OE2425	OE-II : Social & Positive Psychology
26	4	OE2	MGT	23OE2426	OE-II : Seismology & Earthquake

		July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Date of Release	Version	



SN	Sem	Type	BoS/Deptt	Sub. Code	Subject	T/P	Contact Hours				Credits	% Weightage			ESE
							L	T	P	Hrs		MSEs*	TA**	ESE	Duration Hours
FIFTH SEMESTER															
1	5	PC	EE	23VLS1501	Embedded System	T	3	0	0	3	3	30	20	50	3
2	5	PC	EE	23VLS1502	Lab : Embedded System	P	0	0	2	2	1		60	40	
3	5	PC	EE	23VLS1503	CMOS VLSI Design	T	3	0	0	3	3	30	20	50	3
4	5	PC	EE	23VLS1504	Lab : CMOS VLSI Design	P	0	0	2	2	1		60	40	
5	5	PC	EE	23VLS1505	Digital System Modelling	T	3	0	0	3	3	30	20	50	3
6	5	PC	EE	23VLS1506	Lab : Digital System Modelling	P	0	0	2	2	1		60	40	
7	6	PC	EE	23VLS1507	Object Oriented Programming	T	2	0	0	2	2	30	20	50	3
8	6	PC	EE	23VLS1508	Lab : Object Oriented Programming	P	0	0	2	2	1		60	40	
9	5	PE	EE		Professional Elective-I	T	3	0	0	3	3	30	20	50	3
10	5	OE-3	OE		Open Elective-III	T	3	0	0	3	3	30	20	50	3
11	5	MDM	EE		MD Minor Course-III	T	3	0	0	3	3	30	20	50	3
12	5	STR	EE	23VLS1509	Internship and Indsutrial Visit	P	0	0	2	2	1		60	40	
TOTAL							20	0	10	30	25				

1	5	HS	T&P	MLC2125	YC&P5 : YCCE Communication Aptitude Preparation	A	3	0	0	3	0				
---	---	----	-----	---------	--	----------	---	---	---	---	----------	--	--	--	--

Professional Electives I					
1	5	PE-I	EE	23VLS1521	PE-I : CAD for VLSI
2	5	PE-I	EE	23VLS1522	PE-I : Algorithm and Data Structure
3	5	PE-I	EE	23VLS1523	PE-I : Semiconductor Device Modeling

Open Elective - III					Subject	FACULTY
SN	Sem	Type	BoS/Deptt	Sub. Code		
1	5	OE3	CSE	23OE3501	OE-III : Social Reformers in Modern Maharashtra	ARTS
2	5	OE3	CSE	23OE3502	OE-III : Independent India 1948-2010	ARTS
3	5	OE3	CT	23OE3503	OE-III : Introduction To Cognitive Psychology	ARTS
4	5	OE3	CT	23OE3504	OE-III : Introduction To Engineering Psychology	ARTS
5	5	OE3	CT	23OE3505	OE-III : Introduction To Behavioural Psychology	ARTS
6	5	OE3	CT	23OE3506	OE-III : Introduction To Emotional Psychology	ARTS
7	5	OE3	EL	23OE3507	OE-III : Elements of Public Administration	ARTS
8	5	OE3	ETC	23OE3508	OE-III : Ancient Indian History	ARTS
9	5	OE3	IT	23OE3509	OE-III : Consciousness Studies	ARTS
10	5	OE3	IT	23OE3510	OE-III : Psychology for Professionals	ARTS
11	5	OE3	IT	23OE3511	OE-III : Introduction to Sociology and Human Behavior	ARTS
12	5	OE3	GE	23OE3512	OE-III : Economics of Money and Banking	ARTS
13	5	OE3	GE	23OE3513	OE-III : Economics of Capital Market	ARTS
14	5	OE3	GE	23OE3514	OE-III : Digital Humanities	ARTS
15	5	OE3	GE	23OE3515	OE-III : Introduction to Political Science	ARTS
16	5	OE3	CT	23OE3516	OE-III : Bhagwat Geeta - An Engineer's Interpretation	ARTS - IKS
17	5	OE3	CT	23OE3517	OE-III : Artha shastra by Kautiliya	ARTS - IKS
18	5	OE3	CSD	23OE3518	OE-III : Glimpses of Ancient science and Technology	ARTS - IKS
19	5	OE3	CV	23OE3519	OE-III : Indian taxation system	COMMERCE
20	5	OE3	CV	23OE3520	OE-III : Elements of share trading	COMMERCE
21	5	OE3	EE	23OE3521	OE-III : Introduction to Fintech	COMMERCE
22	5	OE3	EE	23OE3522	OE-III : Financial Analytics	COMMERCE
23	5	OE3	ETC	23OE3523	OE-III : Fundamentals of Investments	COMMERCE
24	5	OE3	EE	23OE3524	OE-III : Lifestyle Diseases	HEALTHCARE & MEDICINE
25	5	OE3	EE	23OE3525	OE-III : Holistic Nutrition	HOME SCIENCE
26	5	OE3	EL	23OE3526	OE-III : Community Organization & Development	HOME SCIENCE
27	5	OE3	CSE	23OE3527	OE-III : Human Rights & International Laws	LAW
28	5	OE3	CSE	23OE3528	OE-III : Cyber Crime Administration	LAW
29	5	OE3	MATHS	23OE3529	OE-III : Finite Differences & Numerical Methods	SCIENCE
30	5	OE3	MATHS	23OE3530	OE-III : Business Statistics	SCIENCE
31	5	OE3	PHY	23OE3531	OE-III : Crystalline Solids: Properties and Applications.	SCIENCE
32	5	OE3	PHY	23OE3532	OE-III : Nanotechnology: Fundamental to Applications	SCIENCE
33	5	OE3	CHE	23OE3533	OE-III : Chemistry in daily life	SCIENCE
34	5	OE3	CHE	23OE3534	OE-III : Battery Systems and Management	SCIENCE
35	5	OE3	NPTFEL	23OE3535	OE-III : Designated approved online NPTEL Course	NPTFEL

July, 2023

1.00

Applicable for
AY 2023-24 Onwards

Chairperson

Dean (Acad. Matters)

Date of Release

Version



Nagar Yuwak Shikshan Sanstha's
Yeshwantrao Chavan College of Engineering
 (An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)
B.TECH SCHEME OF EXAMINATION 2023
 (Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)
B. Tech Electronics Engineering(VLSI Design and Technology)

SoE No.
23VLSI-101

SN	Sem	Type	BoS/Deptt	Sub. Code	Subject	T/P	Contact Hours				Credits	% Weightage			ESE Duration Hours
							L	T	P	Hrs		MSEs*	TA**	ESE	
SIXTH SEMESTER															
1	6	PC	EE	23VLS1601	Digital Signal Processing	T	3	0	0	3	3	30	20	50	3
2	6	PC	EE	23VLS1602	Lab: Digital Signal Processing	P	0	0	2	2	1		60	40	
3	6	PC	EE	23VLS1603	VLSI Verification and Testing	T	3	0	0	3	3	30	20	50	3
4	6	PC	EE	23VLS1604	Design Thinking and Research Methodology	T	2	0	0	2	2	30	20	50	3
5	6	PE	EE		Professional Elective-II	T	3	0	0	3	3	30	20	50	
6	6	PE	EE		Lab : Professional Elective-II	P	0	0	2	2	1		60	40	3
7	6	PE	EE		Professional Elective-III	T	3	0	0	3	3	30	20	50	3
8	6	PE	EE		Lab : Professional Elective-III	P	0	0	2	2	1		60	40	
9	6	MDM	EE		MD Minor Course-IV	T	3	0	0	3	3	30	20	50	3
10	5	VSEC-4	EE	23VLS1605	Lab : Electronics Design Automation	P	0	0	2	4	2		60	40	
11	6	STR	EE	23VLS1606	Project Phase-I	P	0	0	4	4	2		60	40	
TOTAL							17	0	12	31	24				

List of Mandatory Learning Course (MLC)

1	6	HS		MLC126	YCAP6 :	A	3	0	0	3	0				
---	---	----	--	--------	---------	---	---	---	---	---	---	--	--	--	--

Professional Electives - II

1	6	PE-II	EE	23VLS1621	PE-II : CMOS Subsystem Design
2	6	PE-II	EE	23VLS1622	PE-II : Lab : CMOS Subsystem Design
3	6	PE-II	EE	23VLS1623	PE-II : Synthesis & Optimisation of VLSI Circuits
4	6	PE-II	EE	23VLS1624	PE-II : Lab : Synthesis & Optimisation of VLSI Circuits
5	6	PE-II	EE	23VLS1625	PE-II : Quantum Computing
6	6	PE-II	EE	23VLS1626	PE-II : Lab : Quantum Computing

Professional Electives - III

1	6	PE-III	EE	23VLS1641	PE-III : Analog VLSI Design
2	6	PE-III	EE	23VLS1642	PE-III : Lab : Analog VLSI Design
3	6	PE-III	EE	23VLS1643	PE-III : FPGA-Based System Design
4	6	PE-III	EE	23VLS1644	PE-III : Lab : FPGA-Based System Design
5	6	PE-III	EE	23VLS1645	PE-III : System C
6	6	PE-III	EE	23VLS1646	PE-III : Lab : System C

		July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Date of Release	Version	

Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

(Accredited 'A++' Grade by NAAC with a score of 3.6)

Hingna Road, Wanadongri, Nagpur - 441 110



Bachelor of Technology

SoE & Syllabus 2023

1st Semester

(Department of Electronics Engineering)

B. Tech in VLSI



Nagar Yuwak Shikshan Sanstha's
Yeshwantrao Chavan College of Engineering
 (An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)
B.TECH SCHEME OF EXAMINATION 2023
 (Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)
B. Tech in V.L.S.I.

SoE No.
23VLSI-101

S N	Sem	Type	BoS/ Deptt	Sub. Code	Subject	T/P	Contact Hours				Credits	% Weightage			ESE Duration Hours
							L	T	P	Hrs		MSEs*	TA**	ESE	
FIRST SEMESTER (GROUP-B)															
1	1	BS	GE	23GE1102	Differential Equations, Matrices and Statistics	T	3	0	0	3	3	30	20	50	3
2	1	BS	GE	23GE1108	Engineering Physics	T	3	0	0	3	3	30	20	50	3
3	1	BS	GE	23GE1109	Lab: Engineering Physics	P	0	0	2	2	1		60	40	
4	1	BES	EE	23EE1101	Basic Electronics	T	3	0	0	3	3	30	20	50	3
5	1	BES	EE	23EE1102	Lab : Basic Electronics	P	0	0	2	2	1		60	40	
6	1	BES	EL	23EL1102	Basic Electrical Engineering	T	3	0	0	3	3	30	20	50	3
7	1	PC	EE	23EE1103	Digital Logic Design	T	3	0	0	3	3	30	20	50	3
8	1	PC	EE	23EE1104	Lab : Digital Logic Design	P	0	0	2	2	1		60	40	
9	1	VSEC	GE	23GE1117	Get Set Go	2		60	40	
10	1	CC2	GE		Liberal Learning Course (LLC2)	2		60	40	
TOTAL FIRST SEM								0	6	21	22				
MANDATORY LEARNING COURSES															
1	1	HS		GE2131	Universal Human Values (UHV)	A	2	0	0	2	0				
SECOND SEMESTER (GROUP-B)															
1	2	BS	GE	23GE1201	Calculus and Vector	T	3	0	0	3	3	30	20	50	3
2	2	BS	GE	23GE1204	Applied Chemistry	T	3	0	0	3	3	30	20	50	3
3	2	BS	GE	23GE1205	Lab: Applied Chemistry	P	0	0	2	2	1		60	40	
4	2	HS/AEC1	GE	23GE1212	Professional Communication	T	2	0	0	2	2	30	20	50	2
5	2	HS/IKS	GE	23GE1215	Indian Knowledge System	T	2	0	0	2	2	30	20	50	2
6	2	BES	EE	23EE1205	Electronics Device and Circuit	T	3	0	0	3	3	30	20	50	3
7	2	BES	EE	23EE1206	Lab: Electronics Device and Circuit	P	0	0	2	2	1		60	40	
8	2	BES	IT	23IT1203	Programming for Problem Solving	T	2	0	0	2	2	30	20	50	2
9	2	BES	IT	23IT1204	Lab: Programming for Problem Solving	P	0	0	2	2	1		60	40	
10	2	VSEC	GE	23GE1218	Functional English	2		60	40	
11	2	CC1	GE		Liberal Learning Course (LLC1)	2		60	40	
TOTAL SECOND SEM							15	0	6	21	22				

Liberal Learning Course

S N	Sem	Type	BoS/ Deptt	Sub. Code	Subject
1	2	CC2	GE	23LLC1201	Music (Vocal)
2	2	CC2	GE	23LLC1202	Music (Instrumental)
3	2	CC2	GE	23LLC1203	Indian Classical Dance
4	2	CC2	GE	23LLC1204	Other forms of Dances
5	2	CC2	GE	23LLC1205	Painting
6	2	CC2	GE	23LLC1206	Theatre and acting
7	2	CC2	GE	23LLC1207	Photography
8	2	CC2	GE	23LLC1208	Yoga
9	2	CC2	GE	23LLC1209	Chess
10	2	CC2	GE	23LLC1210	Athletics
11	2	CC2	GE	23LLC1211	Basket Ball
12	2	CC2	GE	23LLC1212	Judo
13	2	CC2	GE	23LLC1213	Elements of Japanese Language
14	2	CC2	GE	23LLC1214	Elements of German Language
15	2	CC2	GE	23LLC1215	Elements of French Language
16	2	CC2	GE	23LLC1216	Elements of Spanish Language
17	2	CC2	GE	23LLC1217	Basics of Vedic Maths
18	2	CC2	GE	23LLC1218	Skilling in Microsoft Visio and Inkscape



Nagar Yuwak Shikshan Sanstha's
Yeshwantrao Chavan College of Engineering
 (An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)
B.TECH SCHEME OF EXAMINATION 2023
 (Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)
B. Tech in V.L.S.I.

SoE No.
23VLSI-101

S N	Sem	Type	BoS/ Deptt	Sub. Code	Subject	T/P	Contact Hours				Credits	% Weightage			ESE Duration Hours
							L	T	P	Hrs		MSEs*	TA**	ESE	

Liberal Learning Course

S N	Sem	Type	BoS/ Deptt	Sub. Code	Subject
1	1	CC1	GE	23LLC1101	Music (Vocal)
2	1	CC1	GE	23LLC1102	Music (Instrumental)
3	1	CC1	GE	23LLC1103	Indian Classical Dance
4	1	CC1	GE	23LLC1104	Other forms of Dances
5	1	CC1	GE	23LLC1105	Painting
6	1	CC1	GE	23LLC1106	Theatre and acting
7	1	CC1	GE	23LLC1107	Photography
8	1	CC1	GE	23LLC1108	Yoga
9	1	CC1	GE	23LLC1109	Chess
10	1	CC1	GE	23LLC1110	Athletics
11	1	CC1	GE	23LLC1111	Basket Ball
12	1	CC1	GE	23LLC1112	Judo
13	1	CC1	GE	23LLC1113	Elements of Japanese Language
14	1	CC1	GE	23LLC1114	Elements of German Language
15	1	CC1	GE	23LLC1115	Elements of French Language
16	1	CC1	GE	23LLC1116	Elements of Spanish Language
17	1	CC1	GE	23LLC1117	Basics of Vedic Maths
18	1	CC1	GE	23LLC1118	Skilling in Microsoft Visio and Inkscape

MSEs* = Two MSEs of 15 Marks each will conducted and marks of these 2 MSEs will be considered for Continuous Assessment

TA ** = for Theory : TA1-5 marks on Proctored Online Exam, TA2-12 marks on activities decided by course teacher, TA3 - 3 marks on class attendance

TA = for Practical : MSPA will be 15 marks each**

		July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Date of Release	Version	



Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Mathematics & Humanities)

SoE No.
23FY-101

B.Tech First Year

I SEMESTER

23GE1102 : Differential Equations, Matrices and Statistics

Course Outcomes	
The students will be able to <ol style="list-style-type: none"> 1. Use appropriate Methods to solve first order and higher order differential equations and apply it to find solution of engineering problems. 2. Use Matrix method to solve linear system of equations, evaluate eigen values - eigen vectors and its applications. 3. Make use of probability distributions to solve real life problems. 4. Inspect scientific data, use proper curve fitting and find correlation, regression of variables. 	
Unit I: Differential Equations I	(7 Hrs.)
Linear differential equations of first order and first degree, Differential equation reducible to linear form, Exact differential equations (excluding the case of integrating factor) and their applications to various fields. (Contemporary Issues related to Topic)	
Unit II: Differential Equations II	(7 Hrs.)
Higher order linear differential equations with constant coefficients, Complementary functions and Particular Integral for different cases, Method of variation of parameters, Examples on application to various fields. (Contemporary Issues related to Topic)	
Unit III: Differential Equations III	(6 Hrs.)
Cauchy's homogeneous linear differential equations, Legendre's linear differential equation, Applications of differential equations to various fields (only up to second order). (Contemporary Issues related to Topic)	
Unit IV: Partial Differential Equations	(6 Hrs.)
Partial Differential Equations of first order, first degree i.e. Lagrange's form, linear homogeneous equations of higher order with constant coefficient. Application of variable separable method to solve first and second order partial differential equations. (Contemporary Issues related to Topic)	
Unit IV: Matrices	(7 Hrs.)
Rank of a matrix, Consistency of system of equations using rank, Characteristics equations, Eigen values and Eigen vectors, Cayley Hamilton Theorem (without proof) statement and verification, Sylvester's theorem-statement and its application. (Contemporary Issues related to Topic)	
Unit VI: Statistics	(6 Hrs.)
Fitting of straight line, $y = a + bx$, a parabola $y = a + bx + cx^2$, exponential curves and power curves by method of least squares; Lines of regression and correlation; Rank correlation. (Contemporary Issues related to Topic)	
Total Lecture	39 Hours

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Mathematics & Humanities)

SoE No.
23FY-101

B.Tech First Year

Textbooks:

- | | |
|----|--|
| 1. | Erwin Kreyzig, Advance Engineering Mathematics, 6 th Edition, John Wiley and Sons, INC. |
| 2. | H.K. Dass, Engineering Mathematics, 11 th revised edition, S. Chand, Delhi. |
| 3. | H.K. Dass, Advanced Engineering Mathematics, 8 th revised edition, S. Chand, Delhi. |
| 4. | Dr. B.S. Grewal, Higher Engineering Mathematics, 42 th edition, Khanna Publishers. |
| 5. | P.N.Wartikar and J.N.Wartikar, Applied Mathematics, 4 th Edition, Vidyarthi GrihaPrakashan. |

Reference Books:


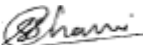
- | | |
|----|--|
| 1. | G B Thomas and R L Finney, Calculus and Analytical Geometry, 9th edition, Addison-Wesley, 1999. |
| 2. | N.P. Bali and Manish Goyal, A text book of Engineering Mathematics, 10 th edition, Laxmi Prakashan. |

YCCE e- library book links [ACCESSIBLE FROM COLLEGE CAMPUS]

- | | |
|---|---|
| 1 | http://103.152.199.179/YCCE/Supported%20file/Supported%20file/e-copies%20of%20books/Applied%20Sciences%20&%20Humanities/Mathematics%20and%20Humanities/ |
|---|---|

MOOCs Links and additional reading, learning, video material

- | | |
|----|---|
| 1. | https://nptel.ac.in/courses/111103070 |
| 2. | https://onlinecourses.nptel.ac.in/noc19_ma28/preview |
| 3. | https://nptel.ac.in/courses/111/106/111106100/ |

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)

(Department of Physics)

B.Tech First Year

SoE No.
23FY-101

I SEMESTER

23GE1108 : Engineering Physics

Course Outcomes :

Upon successful completion of the course the students will be able to

1. Correlate fundamentals of quantum mechanics to solve problems dealing with quantum particles.
2. Assess the characteristics of semiconductor materials in terms of crystal structures, charge carriers and Energy bands.
3. Examine the intensity variation of light due to interference, diffraction, laser and its applications.
4. Analyze the motion of charged particles in electric and magnetic field and its applications to electron optic devices.
5. Illustrate the nature and characterization of magnetic materials and superconductors for engineering applications.

Unit I: Quantum Physics

(7 Hrs.)

Wave-particle duality, de-Broglie's hypothesis, Wave packet, Heisenberg's uncertainty principle: significance and applications, Wave function and its probability interpretation, Schrodinger Equation, Particle in infinite potential well. (Contemporary Issues related to Topic)

Unit II: Semiconductor Physics

(7 Hrs.)

Formation of energy bands in solids; Classification of solids, Energy band diagram of Si and Ge, Intrinsic and extrinsic semiconductors, Conductivity, Law of mass action, Fermi function, Fermi level in intrinsic and extrinsic semiconductors, Dependence of Fermi level on impurity concentration and temperature, Hall effect. (Contemporary Issues related to Topic)

Unit III: Geometrical Optics

(7 Hrs.)

Interference: Interference in thin films, Wedge shaped film, Newton's rings, Applications of interference
Diffraction: Fraunhofer diffraction from a single slit. (Contemporary Issues related to Topic)

Unit IV: Laser

(6 Hrs.)

Coherence and its types, Interaction of radiation with matter, Population Inversion, Pumping: methods and schemes, Optical resonant cavity, Ruby laser, Semiconductor diode laser, Properties and engineering applications of laser. (Contemporary Issues related to Topic)

Unit V: Electron Ballistics

(7 Hrs.)



Motion of a charged particle in uniform electric and magnetic field, Cross field configuration; Electron refraction, Electron lens. Cathode ray oscilloscope and its application. (Contemporary Issues related to Topic)

Unit VI: Magnetic Materials & Superconductors

(6 Hrs.)

Introduction to magnetic materials, Interpretation of Hysteresis curves, Superconductors: Type-I and Type-II, Meissner effect, Applications. (Contemporary Issues related to Topic)

Total Lecture 40 Hours

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Physics)

**SoE No.
23FY-101**

B.Tech First Year

Textbooks

1	M. N. Avadhanulu, P.G.Kshirsagar, A Textbook of Engg. Physics, S.Chand and Company.
2	Hitendra K Malik , A K Singh , Engineering Physics, 2nd Edition, Tata McGraw Hill Education Private Limited,

Reference Books

1	David Halliday, Robert Resnick and Jerle Walker, John-Wiley India, Fundamentals of Physics, 10 th John Wiley & Sons Inc.
2	Brijlal and Subramanyam, Text Book of Optics, Revised edition, S. Chand and Company.
3	M.N. Avadhanulu, 2 nd Edition, Laser, S.Chand and Company.
4	A.Beiser, Concept of Modern Physics, 6 th Edition, Laser, Tata McGraw-Hill.
5	Thyagarajan K. and Ghatak A.K, LASERS: Theory and Applications, 2 nd Edition, Macmillan Publication
6	S.O.Pillai, Solid State Physics, 9 th Edition, New Edge International Publishers.
7	Palanisamy, Solid State Physics, 8 th Edition, New Edge International Publishers.
8	C. Kittel, Solid State Physics, 8 th Edition, Willey Publication.
9	B. K. Pandey, S. Chaturvedi, Engineering Physics, 1 st Edition, Cengage Learning.
10	John Allision, Electronic Engineering Materials and Devices, TMH edition, 10 th reprint, Tata McGraw Hill.

YCCE e- library book links [ACCESSIBLE FROM COLLEGE CAMPUS]

1	http://103.152.199.179/YCCE/Suported%20file/Supprted%20file/e-copies%20of%20books/Applied%20Sciences%20&%20Humanities/Physics/Eisberg%20&%20Resnick%20-%20Quantum%20Physics.pdf
2	http://103.152.199.179/YCCE/Suported%20file/Supprted%20file/e-copies%20of%20books/Applied%20Sciences%20&%20Humanities/Physics/2016_Book_ThePhysicsOfSemiconductors.pdf
3	http://103.152.199.179/YCCE/Suported%20file/Supprted%20file/e-copies%20of%20books/Applied%20Sciences%20&%20Humanities/Physics/Dekker%20-%20Solid%20State%20Physics.pdf

MOOCs Links and additional reading, learning, video material

1	https://nptel.ac.in/courses/115106066 - Quantum Physics
2	https://archive.nptel.ac.in/courses/115/105/115105121/ -CRO
3	www.digimat.in/nptel/courses/video/115102124/L36.html - Laser

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)

(Department of Physics)

B.Tech First Year

SoE No.
23FY-101

I SEMESTER

23GE1109 : Lab. Engineering Physics

Course Outcomes:

Upon successful completion of the course the students will be able to

1. Correlate fundamentals of quantum mechanics to solve problems dealing with quantum particles.
2. Assess the characteristics of semiconductor materials in terms of crystal structures, charge carriers and Energy bands.
3. Examine the intensity variation of light due to interference, diffraction, laser and its applications.
4. Analyze the motion in electric field and magnetic field and its applications to electron optic devices.
5. Illustrate the nature and characterization of magnetic materials and superconductors for engineering Applications.

List of Experiments :

Sr. No.	Experiments based on
1	Determination of Planck's constant.
2	Study of Tunnel Diode.
3	Determination of Hall coefficient and density of charge carriers using Hall effect.
4	Dependence of Hall coefficient on temperature.
5	Determination of Band gap in a semiconductor by four probe method.
6	Determination of Band gap in a semiconductor using reverse biased p-n junction diode.
7	Determination of radius of curvature of Plano convex lens using Newton's rings.
8	Determination of thickness of thin paper using air wedge.
9	Determination of wavelength of sodium light using diffraction grating.
10	Determination of wavelength of laser using diffraction grating.
11	Determination of divergence of laser beam.
12	Determination of amplitude and frequency of sinusoidal signal using CRO.
13	To measure the phase shift introduced by a phase shift network using Dual beam CRO.
14	Determination of the velocity of Ultrasonic waves in a non -electrolytic liquid by ultrasonic interferometer.

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023

(Scheme of Examination w.e.f. 2023-24 onward)

(Department of Electronics Engineering)

B.Tech in Electronics Engineering

**SoE No.
23EE-101**

I SEMESTER

23EE1101 : Basic Electronics

Course Outcomes:

Upon successful completion of the course the students will be able to

1. Understand, define and explain the fundamental concepts of Analog Electronic Circuits
2. Apply the concepts of Electronic Circuits to obtain the desired parameter
3. Analyze Electronic Circuits to arrive at suitable Conclusions.
4. Design simple circuits using fundamentals of Electronic circuit for given application

Unit:1	Diode and its Applications	7 Hours
Characteristics of materials based on Energy band theory, Intrinsic and extrinsic semiconductors, P-N junction diodes, Biasing & Characteristics of diodes. Diode Circuits - Half wave rectifier, full wave rectifier, bridge rectifier		
Unit:2	Bipolar Junction Transistor	7 Hours
Introduction to BJT- NPN and PNP, biasing, Modes of operation, Configuration and its Characteristics		
Unit:3	BJT Applications	7 Hours
Amplifiers: Various classes of operation (Class A, B, AB, C etc.), Oscillators: Review of the basic concept, Barkhausen criterion, RC & LC oscillators		
Unit:4	OPAMP & its Applications	6 Hours
Introduction to Op-Amp, Inverting and Non-Inverting Amplifier, Linear Applications of OP-AMP, Comparator.		
Unit:5	Measurement Systems	7 Hours
Introduction to Measurement System, Generalized block diagram of Measurement System, Static & dynamic characteristics of measurement system, Types of errors & their sources, Statistical analysis		
Unit :6	DAC & ADC	7 Hours
Digital-to-Analog converters: Weighted resistor, R-2R ladder, etc. Analog-to-Digital converters: Single slope, dual slope, etc		
Total Lecture Hours		41 Hours

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023

(Scheme of Examination w.e.f. 2023-24 onward)

(Department of Electronics Engineering)

B.Tech in Electronics Engineering

SoE No.
23EE-101

Text books

- | | |
|---|---|
| 1 | Electronics Devices and circuits, Millman Jacob, McGraw Hill Education, Fourth Edition (2015) |
| 2 | A.S. Sedra and K.C. Smith, Microelectronic Circuits, sixth edition, Oxford University Press |

Reference Books

- | | |
|---|--|
| 1 | OP-AMP and Linear Integrated Circuit, by Ramakant A. Gayakwad, Prentice Hall India Learning Private Limited, Published in 2002 |
| 2 | J.V. Wait, L.P. Huelsman and GA Korn, Introduction to Operational Amplifier theory and applications, McGraw Hill, 1992. |
| 3 | Electrical & Electronic measurement & Instrument, A. K. Sawhney, Dhanpat Rai & Co., 18th edition 2008 |

YCCE e- library book links [ACCESSIBLE FROM COLLEGE CAMPUS]

- | | |
|---|---|
| 1 | http://link.springer.com/openurl?genre=book&isbn=978-1-4613-6193-0 |
| 2 | https://onlinelibrary.wiley.com/doi/book/10.1002/9780470168042 |

MOOCs Links and additional reading, learning, video material

- | | |
|---|---|
| 1 | https://onlinecourses.nptel.ac.in/noc22_ee113/preview |
| 2 | https://nptel.ac.in/courses/108106084 |

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023

(Scheme of Examination w.e.f. 2023-24 onward)

(Department of Electronics Engineering)

B.Tech in Electronics Engineering

**SoE No.
23EE-101**

I SEMESTER

23EE1102 : Lab. Basic Electronics

Course Outcomes:

Upon successful completion of the course the students will be able to

1. Understand, define and explain the fundamental concepts of Analog Electronic Circuits
2. Apply the concepts of Electronic Circuits to obtain the desired parameter
3. Analyze Electronic Circuits to arrive at suitable Conclusions.
4. Design simple circuits using fundamentals of Electronic circuit for given application

Sr. No.	Experiments based on
1	To verify characteristics of PN Junction under Forward and Reverse bias
2	To study Half Wave Rectifier and Full wave rectifier
3	To verify Input and Output characteristics of Transistor in Common Emitter configuration
4	To verify Input and Output characteristics of Transistor in Common Base configuration
5	To verify Inverting and Non-inverting Operational amplifiers
6	To study Summing Operational amplifier
7	To study Generalized block diagram of Measurement System
8	To study Static & dynamic characteristics of measurement system
9	To study Analog to Digital converter
10	To study Digital to Analog converter

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023

(Scheme of Examination w.e.f. 2023-24 onward)

(Department of Electrical Engineering)

B.Tech in Electrical Engineering

SoE No.
23EL-101

I SEMESTER

23EL1102 : Basic Electrical Engineering

Course Outcomes:

Upon successful completion of the course the students will be able to

1. Reproduce fundamentals of dc circuits.
2. Explain, construction, working and applications of various electrical machines.
3. Analyze performance of various electrical machines

Unit:1	D.C. Circuits	7 Hours
D.C. Circuits: Basics of electrical circuits. Equivalent resistance, Kirchhoff's Laws. Current and Voltage division rule. Mesh and Nodal analysis of dc circuits. Superposition Theorem. (Contemporary Issues related to Topic)		
Unit:2	AC Circuits	7 Hours
A.C. Fundamentals: Values of alternating quantity. Concept of power factor, reactive power and apparent power with power triangle, R, L, C Series circuit and Parallel circuit, Resonance condition. (Contemporary Issues related to Topic)		
Unit:3	Three Phase AC Circuits	7 Hours
Advantages of three – phase system over single – phase system. Generation of three phase a.c. supply. Phase sequence. Interconnection of three phases. Star or Wye (Y) connection. Phase and line voltages/currents in star connection and their relationships. Delta or Mesh connection. Phase and line voltages/currents in delta connection and their relationships. Concept of balanced load. Active, reactive, and apparent power in balanced three phase circuits. (Contemporary Issues related to Topic)		
Unit:4	Single Phase Transformer	6 Hours
Working principle. EMF equation. Voltage ratio and turns ratio. Step up and step down transformers. Construction of single phase transformer. Ideal transformer. Transformer on no load and equivalent circuit. Practical transformer and its equivalent circuit. Referred values. Voltage Regulation. Losses in transformer. Open circuit and Short circuit tests on transformer. Efficiency and condition for maximum efficiency. (Contemporary Issues related to Topic)		
Unit:5	DC Motor	7 Hours
Principle, Torque Equation, Characteristics and applications of various types of D.C. Motors, Starting of D.C. Motors, Speed control of Series and Shunt motors, Power flow in DC machines, Losses and Efficiency in D.C. machines. (Contemporary Issues related to Topic)		

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023

(Scheme of Examination w.e.f. 2023-24 onward)

(Department of Electrical Engineering)

B.Tech in Electrical Engineering

SoE No.
23EL-101

Unit :6	Three Phase Induction Motor	7 Hours
Construction, Production of rotating magnetic field. Principle of operation. Speed and slip. Frequency of rotor voltage and current. Applications of three phase induction motor. (Contemporary Issues related to Topic)		
Total Lecture Hours		39 Hours

Textbooks

1	T. K. Nagsarkar and M. S. Sukhija, Basic Electrical Engineering, 1st Edition, Oxford Higher Education, 2005
2	V. N. Mittle and A. K. Mittal, Basic Electrical Engineering, 2nd Edition, 2006, The McGraw Hill Companies, New Delhi
3	B.L. Theraja, Electrical Technology, S.Chand, 2005
4	T. Kenjo and S. Nugatory, Permanent Magnet and Brushless DC motors, England, Clarendon Oxford Press, 1989

Reference Books

1	I J Nagrath and D. P. Kothari, Basic Electrical Engineering, 2nd Edition, 2002, McGraw Hill, New Delhi
2	Vincent Del Toro, Electrical Engineering Fundamentals, 2nd Edition, 2002, Prentice Hall India, New Delhi

YCCE e- library book links [ACCESSIBLE FROM COLLEGE CAMPUS]

1	http://link.springer.com/openurl?genre=book&isbn=978-3-642-25904-3
2	http://link.springer.com/openurl?genre=book&isbn=978-1-4614-0399-9

MOOCs Links and additional reading, learning, video material

1	https://nptel.ac.in/courses/108105155
----------	---

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

SoE No.
23EE-101

B.Tech in Electronics Engineering

I SEMESTER

23EE1103 : Digital Logic Design

Course Outcomes:

Upon successful completion of the course the students will be able to

1. Apply the laws of Boolean algebra to simplify logical equations and combination logic circuits.
2. Understand and demonstrate the various codes and illustrate their addition subtraction.
3. Solve logical functions using K- map to implement combinational logic circuits.
4. Design and analyze Synchronous and Asynchronous sequential Circuits.

Unit:1	Number system and codes	7 Hours
Binary, Octal, hexadecimal and decimal Number systems and their inter conversion, BCD numbers (8421-2421), Gray code, ASCII codes. Binary addition and subtraction, signed and unsigned binary numbers, 1's and 2's complement representation.		
Unit:2	Boolean Algebra	7 Hours
Basic logic circuits: Logic gates (AND, OR, NOT, NAND, NOR, Ex-OR, Ex-NOR and their truth tables), Universal Gates, Laws of Boolean algebra, De-Morgan's theorem.		
Unit:3	Minimization Techniques	7 Hours
Minterm, Maxterm, POS, SOP, K-Map, Simplification by Boolean theorems, don't care condition.		
Unit:4	Combinational Logic	7 Hours
Half adder, Full adder, Subtractor circuit. Multiplexer demultiplexer, decoder, BCD to seven segment Decoder, encoders, code converters.		
Unit:5	Sequential Circuits	7 Hours
Flipflop, set-reset latches, R-S flip-flop, D-flipflop, J-K Flip-flop, Master slave Flipflop, T flip-flop, excitation table of flip-flops. Flip-Flop to flip-flop conversion		
Unit :6	Registers & Counters	7 Hours
Serial in/Serial out shift register, Serial in/parallel out shift register, parallel in/parallel out shift register, parallel in/Serial out shift register, Bi-directional register, Synchronous/Asynchronous counter: Ring Counter, Ripple Counter Johnson's Counter operation, Up/down synchronous counter, application of counter.		
Total Lecture Hours		42 Hours

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023

(Scheme of Examination w.e.f. 2023-24 onward)

(Department of Electronics Engineering)

B.Tech in Electronics Engineering

SoE No.
23EE-101

Textbooks

- | | |
|---|---|
| 1 | Modern Digital Electronics , RP Jain, Tata McGraw Hill, 3rd Edition |
| 2 | M. Morris Mano, Digital Design, 3rd Edition, Prentice Hall of India Pvt. Ltd., 2003 Pearson Education (Singapore) Pvt. Ltd., New Delhi, 2003. |
| 3 | Donald P. Leach and Albert Paul Malvino, Digital Principles and Applications, 6th Edition, TMH, 2003. |
| 4 | Anandkumar- fundamental of digital circuit. 3rd edition. PHI |

Reference Books

- | | |
|---|--|
| 1 | Fundamentals of Logic Design, C.H. Roth, Public Work & Services, 3rd edition 2007. |
| 2 | Engg Approach to Digital Design, Fletcher, Prentice Hall of India 1993. |
| 3 | Digital Circuits & Microprocessors, Hebert Taub, Mc Graw Hill, 1988. |

YCCE e- library book links [ACCESSIBLE FROM COLLEGE CAMPUS]

- | | |
|---|---|
| 1 | http://103.152.199.179/YCCE/yccelibrary.html |
|---|---|

MOOCs Links and additional reading, learning, video material

- | | |
|---|---|
| 1 | https://www.digimat.in/nptel/courses/video/108105132/L01.html |
| 2 | https://www.digimat.in/nptel/courses/video/108105113/L01.html |
| 3 | https://www.coursera.org/learn/digital-systems |

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023

(Scheme of Examination w.e.f. 2023-24 onward)

(Department of Electronics Engineering)

B.Tech in Electronics Engineering

**SoE No.
23EE-101**

I SEMESTER

23EE1104 : Lab. Digital Logic Design

Course Outcomes:

Upon successful completion of the course the students will be able to

1. Apply the laws of Boolean algebra to simplify logical equations and combination logic circuits.
2. Understand and demonstrate the various codes and illustrate their addition subtraction.
3. Design and exhibit the methods to solve logical functions using K- map to implement combinational logic circuits.
4. Design and analyze Synchronous and Asynchronous sequential Circuits.

Sr. No.	Experiments based on
1	Basic logic circuits: Logic gates verification using kit.
2	Introduction to Bread Board and Verify Truth Tables of basic Logic gates using BreadBoard.
3	Construction of half/full adder using XOR and NAND gates and verification of its operation.
4	Verify Binary to Gray and Gray to Binary conversion using NAND gates only.
5	Implementation of 4x1 multiplexer and 1x4 demultiplexer using logic gates.
6	Verify the truth table of D-flip-flops and JK- flip-flops.
7	Design and verify the 4-Bit Synchronous Counter.
8	Introduction to SPICE Digital model and commands. Verify Truth Tables of basic Logic gates & Universal Gates using using SPICE .
9	Design & verify Truth Table of Half adder & Full adder circuits Logic simulator .
10	Design & verify Truth Table of 4:1 Multiplexer & 1:4 Demultiplexer circuits using SPICE .

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Civil Engineering)

SoE No.
23FY-101

B.Tech in FYC

I SEMESTER

23GE1117-Get Set Go

Course Outcomes:

Upon successful completion of the course the students will be able to

1. Students will understand the importance of building trust in communication and learn how to use the 3Vs of communication (Visual, Vocal, Verbal) to energize their interactions.
2. The course will focus on leadership principles and styles, emphasizing how effective communication can motivate others and gain willing cooperation. Students will participate in activities like skits and team presentations to demonstrate their leadership skills.
3. The course will equip students with team management and organization skills, enabling them to lead and participate in team-building activities effectively.

Unit:1	Build a foundation for success	6 Hours
<p>Explain the Importance of Process of improvement, stating your Name with Impact, Recall and Use Names, Name Remembering Formula o LIRA o PACE – Individual Activity o BRAMMS o Chaining Method, Introduce “My Vision”</p> <p>Communication Fundamentals for Building Trust- Be a good listener, use conversation links, show genuine interest Hi-Five of Success ♣ Build on Memory Skills and Enhance Relationships ♣ PEG words ♣ Explain Permanent PEG Memory System, energize our Communications – Explain 3Vs of communication – Visual-Vocal-Verbal</p> <p>Activity – Practice Conversations, Pause-Part-Punch, Group Activity</p>		
Unit:2	Increase Self Confidence	6 Hours
<p>Use our experiences to communicate more confidently • Communicate with clarity and conciseness • Discover how past experiences influence behaviour ,Motivate Others and Enhance Relationships- • Learning Objectives • Explain Gain Willing Cooperation Principles • Group Presentation • Explain Demonstration of Leadership Principles • Explain “Evidence” critical in establishing credibility</p> <p>Individual Activity – Sharing of defining moment, Skit to demonstrate Leadership Principles, Stranded on Island .</p>		
Unit:3	Fundamentals of Communication	6 Hours
<p>Fundamentals of Communication (Earn the right – Excite -Eagerness) ♣ Elevator Pitch ♣ Develop more Flexibility, ♣ Recap and Summarize</p> <p>Activities - – Individual Presentation, Flexibility Drills, Individual Presentations – My Vision Assignment</p>		
Unit:4	Team Management and Organization skills	5 Hours
<p>Team Management and Organization skills, Leadership Styles, Effective Communication</p> <p>Activity- Team Presentation, Team building activities.</p>		
EVALUATION	1 Hour	EVALUATION
WRITTEN TEST		
Total Lecture Hours		24 Hours

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's
Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

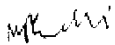

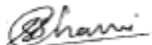
B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Civil Engineering)

SoE No.
23FY-101

B.Tech in FYC

Reference Books

- | | |
|---|---|
| 1 | Soft Skills - Enhancing Employability: Connecting Campus with Corporate. - M S Rao |
| 2 | Soft Skills Training: A Workbook to Develop Skills for Employment - Frederick H Wentz |
| 3 | Soft Skills: Know Yourself and Know the World - Alex |

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	

Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

(Accredited 'A++' Grade by NAAC with a score of 3.6)

Hingna Road, Wanadongri, Nagpur - 441 110



Bachelor of Technology SoE & Syllabus 2023 2nd Semester

(Department of Electronics Engineering)

B. Tech in VLSI



Nagar Yuwak Shikshan Sanstha's
Yeshwantrao Chavan College of Engineering
 (An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)
B.TECH SCHEME OF EXAMINATION 2023
 (Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)
B. Tech in V.L.S.I.

SoE No.
23VLSI-101

S N	Sem	Type	BoS/ Deptt	Sub. Code	Subject	T/P	Contact Hours				Credits	% Weightage			ESE Duration Hours
							L	T	P	Hrs		MSEs*	TA**	ESE	
FIRST SEMESTER (GROUP-B)															
1	1	BS	GE	23GE1102	Differential Equations, Matrices and Statistics	T	3	0	0	3	3	30	20	50	3
2	1	BS	GE	23GE1108	Engineering Physics	T	3	0	0	3	3	30	20	50	3
3	1	BS	GE	23GE1109	Lab: Engineering Physics	P	0	0	2	2	1		60	40	
4	1	BES	EE	23EE1101	Basic Electronics	T	3	0	0	3	3	30	20	50	3
5	1	BES	EE	23EE1102	Lab : Basic Electronics	P	0	0	2	2	1		60	40	
6	1	BES	EL	23EL1102	Basic Electrical Engineering	T	3	0	0	3	3	30	20	50	3
7	1	PC	EE	23EE1103	Digital Logic Design	T	3	0	0	3	3	30	20	50	3
8	1	PC	EE	23EE1104	Lab : Digital Logic Design	P	0	0	2	2	1		60	40	
9	1	VSEC	GE	23GE1117	Get Set Go	2		60	40	
10	1	CC2	GE		Liberal Learning Course (LLC2)	2		60	40	
TOTAL FIRST SEM								0	6	21	22				
MANDATORY LEARNING COURSES															
1	1	HS		GE2131	Universal Human Values (UHV)	A	2	0	0	2	0				
SECOND SEMESTER (GROUP-B)															
1	2	BS	GE	23GE1201	Calculus and Vector	T	3	0	0	3	3	30	20	50	3
2	2	BS	GE	23GE1204	Applied Chemistry	T	3	0	0	3	3	30	20	50	3
3	2	BS	GE	23GE1205	Lab: Applied Chemistry	P	0	0	2	2	1		60	40	
4	2	HS/AEC1	GE	23GE1212	Professional Communication	T	2	0	0	2	2	30	20	50	2
5	2	HS/IKS	GE	23GE1215	Indian Knowledge System	T	2	0	0	2	2	30	20	50	2
6	2	BES	EE	23EE1205	Electronics Device and Circuit	T	3	0	0	3	3	30	20	50	3
7	2	BES	EE	23EE1206	Lab: Electronics Device and Circuit	P	0	0	2	2	1		60	40	
8	2	BES	IT	23IT1203	Programming for Problem Solving	T	2	0	0	2	2	30	20	50	2
9	2	BES	IT	23IT1204	Lab: Programming for Problem Solving	P	0	0	2	2	1		60	40	
10	2	VSEC	GE	23GE1218	Functional English	2		60	40	
11	2	CC1	GE		Liberal Learning Course (LLC1)	2		60	40	
TOTAL SECOND SEM							15	0	6	21	22				

Liberal Learning Course

S N	Sem	Type	BoS/ Deptt	Sub. Code	Subject
1	2	CC2	GE	23LLC1201	Music (Vocal)
2	2	CC2	GE	23LLC1202	Music (Instrumental)
3	2	CC2	GE	23LLC1203	Indian Classical Dance
4	2	CC2	GE	23LLC1204	Other forms of Dances
5	2	CC2	GE	23LLC1205	Painting
6	2	CC2	GE	23LLC1206	Theatre and acting
7	2	CC2	GE	23LLC1207	Photography
8	2	CC2	GE	23LLC1208	Yoga
9	2	CC2	GE	23LLC1209	Chess
10	2	CC2	GE	23LLC1210	Athletics
11	2	CC2	GE	23LLC1211	Basket Ball
12	2	CC2	GE	23LLC1212	Judo
13	2	CC2	GE	23LLC1213	Elements of Japanese Language
14	2	CC2	GE	23LLC1214	Elements of German Language
15	2	CC2	GE	23LLC1215	Elements of French Language
16	2	CC2	GE	23LLC1216	Elements of Spanish Language
17	2	CC2	GE	23LLC1217	Basics of Vedic Maths
18	2	CC2	GE	23LLC1218	Skilling in Microsoft Visio and Inkscape



Nagar Yuwak Shikshan Sanstha's
Yeshwantrao Chavan College of Engineering
 (An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)
B.TECH SCHEME OF EXAMINATION 2023
 (Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)
B. Tech in V.L.S.I.

SoE No.
23VLSI-101

S N	Sem	Type	BoS/ Deptt	Sub. Code	Subject	T/P	Contact Hours				Credits	% Weightage			ESE Duration Hours
							L	T	P	Hrs		MSEs*	TA**	ESE	

Liberal Learning Course

S N	Sem	Type	BoS/ Deptt	Sub. Code	Subject
1	1	CC1	GE	23LLC1101	Music (Vocal)
2	1	CC1	GE	23LLC1102	Music (Instrumental)
3	1	CC1	GE	23LLC1103	Indian Classical Dance
4	1	CC1	GE	23LLC1104	Other forms of Dances
5	1	CC1	GE	23LLC1105	Painting
6	1	CC1	GE	23LLC1106	Theatre and acting
7	1	CC1	GE	23LLC1107	Photography
8	1	CC1	GE	23LLC1108	Yoga
9	1	CC1	GE	23LLC1109	Chess
10	1	CC1	GE	23LLC1110	Athletics
11	1	CC1	GE	23LLC1111	Basket Ball
12	1	CC1	GE	23LLC1112	Judo
13	1	CC1	GE	23LLC1113	Elements of Japanese Language
14	1	CC1	GE	23LLC1114	Elements of German Language
15	1	CC1	GE	23LLC1115	Elements of French Language
16	1	CC1	GE	23LLC1116	Elements of Spanish Language
17	1	CC1	GE	23LLC1117	Basics of Vedic Maths
18	1	CC1	GE	23LLC1118	Skilling in Microsoft Visio and Inkscape

MSEs* = Two MSEs of 15 Marks each will conducted and marks of these 2 MSEs will be considered for Continuous Assessment

TA ** = for Theory : TA1-5 marks on Proctored Online Exam, TA2-12 marks on activities decided by course teacher, TA3 - 3 marks on class attendance

TA = for Practical : MSPA will be 15 marks each**

		July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Date of Release	Version	



Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Mathematics & Humanities)

SoE No.
23FY-101

B.Tech First Year

II SEMESTER

23GE1201: Calculus and Vector

Course Outcomes :

The students will be able to

1. Apply the knowledge of differentiation to solve the Engineering problems.
2. Determine the derivatives of functions of several variables and develop the relations among the derivatives of variables.
3. Apply the knowledge of Beta and Gamma functions to find area, volume and mass.
4. Discuss Calculus of Scalar and vector point function and use appropriate theorems to evaluate integrals of functions of single and multiple variables.

Unit I: Differential Calculus

(6 Hrs.)

Successive differentiation, n^{th} derivative of rational function, Trigonometrical transformations, n^{th} derivative of the product of two functions (Leibnitz's theorem), Taylor's theorem, Use of Maclaurin's theorem for one variable, standard expansions, Examples on Taylor's Theorem. **(Contemporary Issues related to Topic)**

Unit II: Partial Differentiation

(7 Hrs.)

Functions of several variables, First and higher order derivatives, Homogeneous functions, Euler's theorem on homogeneous function, Chain rule and total differential coefficient of composite functions. Jacobians. **(Contemporary Issues related to Topic)**

Unit III: Integral Calculus

(6 Hrs.)

Improper integrals: Gamma and Beta functions, applications of integral calculus in computing area, length, volumes, and surface of solids of revolutions. **(Contemporary Issues related to Topic)**

Unit IV: Multiple integrals

(6 Hrs.)

Double integral, change of order of integral, change of variables, triple integrals and its applications. **(Contemporary Issues related to Topic)**

Unit V: Vector Calculus

(7 Hrs.)


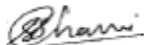
Vector fields, Vector differentiation, Gradient, Divergence and Curl, Directional derivatives with physical interpretation, Solenoidal and irrotational motions. **(Contemporary Issues related to Topic)**

Unit VI: Vector Integration & Applications

(7 Hrs.)

Vector integration: Line, surface and volume integrals, Statement of Stoke's theorem, Gauss divergence theorem and Green's theorem (without proof), Simple applications of these theorems. **(Contemporary Issues related to Topic)**

Total Lecture 39 Hours

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Mathematics & Humanities)

SoE No.
23FY-101

B.Tech First Year

Textbooks:

- | | |
|----|--|
| 1. | Erwin Kreyzig, Advance Engineering Mathematics, 10 th Edition, John Wiley and Sons, INC. |
| 2. | H.K. Dass, Engineering Mathematics, 11 th revised edition, S. Chand, Delhi. |
| 3. | H.K. Dass, Advanced Engineering Mathematics, 8 th revised edition, S. Chand, Delhi. |
| 4. | Dr. B.S. Grewal, Higher Engineering Mathematics, 42 th edition, Khanna Publishers. |
| 5. | P.N.Wartikar and J.N.Wartikar, Applied Mathematics, 4 th Edition, Vidyarthi GrihaPrakashan. |

Reference Books:


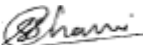
- | | |
|----|--|
| 1. | G B Thomas and R L Finney, Calculus and Analytical Geometry, 9th edition, Addison-Wesley, 1999. |
| 2. | Michael Spivak and Tom Apostol, Calculus, Vol I & Vol II 2 nd edition, Wiley. |
| 3. | N.P. Bali and Manish Goyal, A text book of Engineering Mathematics, 10 th edition, Laxmi Prakashan. |

YCCE e- library book links [ACCESSIBLE FROM COLLEGE CAMPUS]

- | | |
|---|---|
| 1 | http://103.152.199.179/YCCE/Supported%20file/Supported%20file/e-copies%20of%20books/Applied%20Sciences%20&%20Humanities/Mathematics%20and%20Humanities/ |
|---|---|

MOOCs Links and additional reading, learning, video material

- | | |
|----|---|
| 1. | https://nptel.ac.in/courses/111/106/111106146/ |
| 2. | https://nitkkr.ac.in/docs/5-Multiple%20Integrals%20and%20their%20Applications.pdf |

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Applied Chemistry)
B.Tech First Year

SoE No.
23FY-101

I/II SEMESTER

23GE1104/23GE1204: Applied Chemistry

Course Outcomes:

Upon successful completion of the course the students will be able to:

1. **Build** the knowledge of qualitative and quantitative aspects of water for industrial and domestic applications. (L3)
2. **Apply** fundamental principles of electrochemistry to understand corrosion, energy storage devices and their industrial applications. (L3)
3. **Develop** insight into engineering materials for industrial applications. (L3)
4. **Utilize** knowledge of advanced engineering materials for technological applications. (L3).

Unit I: Water Chemistry

(8 Hrs.)

Introduction, Potable water quality parameters. Hardness, Types of hardness. Sterilization. Desalination of water by R.O. Softening of water by Zeolite process and Ion Exchange Process (principle, advantages, and limitations). Numerical based on Hardness and Zeolite process. Boiler trouble (Scale and sludge). Contemporary issues related to the topic

Unit II: Electrochemistry

(8 Hrs.)

Introduction, Redox reactions, EMF of a cell, standard electrode potential, Nernst equation, numerical and applications to chemical cells. Conductance in electrolytic solutions, specific and molar conductivity, variations of conductivity with concentration, Electrolysis, laws of electrolysis and numerical.

Industrial applications: Electroplating, Electrolytic refining.

Corrosion: Definition, Causes, theories of corrosion- dry, wet and differential aeration.

Contemporary issues related to the topic

Unit III: Energy storage devices

(7 Hrs.)

Battery: Introduction, Characteristics, and General applications

Lithium-ion battery, Glass battery, H_2 - O_2 Fuel cell. Differences between Battery and Fuel cell. Recycling and safe disposal of batteries.

Supercapacitors: Definition, Types, Characteristics, and Application.

H_2 as a green fuel: Introduction, Production, Storage, and Utilization. Contemporary issues related to the topic

Unit IV: Fuels

(8 Hrs.)

Introduction, Calorific value, HCV & LCV. Determination of calorific value of fuels by Bomb & Boy's calorimeter. Dulong's formula Numerical.



Significance of Proximate and Ultimate analysis.

Knocking in Internal combustion petrol and diesel engines, Octane and Cetane number, Knocking and its relationship with structure of fuels. Catalytic cracking & advantages. Contemporary issues related to the topic

Unit V: Engineering Materials

(7 Hrs.)

Cement: Introduction, Manufacturing of Portland cement. Role of microscopic constituents. Properties-setting and hardening, heat of hydration and soundness. Types of cement-Rapid hardening cement, Low heat cement, High alumina cement. Ready-mix concrete.

			July, 2025	1.00	Applicable for AY 2025-26 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023

(Scheme of Examination w.e.f. 2023-24 onward)

(Department of Applied Chemistry)

B.Tech in ME/CV/EE/ETC/EL/VLSI

SoE No.
23FY-101

Lubricants: Introduction, Classification, Mechanism of Lubrication. Properties & Significance of liquid lubricants—Viscosity and viscosity index, Flash and fire point, Cloud and pour point, Aniline point, acid value, saponification number. Numerical on V.I. Contemporary issues related to the topic.

Unit VI: Advanced Materials

(7 Hrs.)

Nanomaterials: Definition, Carbon Nanotubes and types. Applications of Nanomaterials in Electronics, Environment and Medicine.

Liquid Crystal Polymers: Introduction, General properties and applications.

Polymers in electronic industries: Introduction, Piezo, pyroelectric, Ferroelectric polymers.

Smart materials: Introduction, Properties and applications of Chromoactive, Photoactive and Magneto rheological materials.

Spectroscopic techniques: Introduction and applications. Contemporary issues related to the topic

Total Lecture 45 Hours

Textbooks:

1. S S. Dara , A Text book of Engineering Chemistry , S.Chand & Co New Delhi. Eleventh Edition.
2. P.C. Jain and Monica Jain , Engineering Chemistry , Dhanpat Rai & sons New Delhi , Sixteenth Edition.
3. P. W. Atkins, Physical Chemistry ,Oxford Publications, Eighth edition .

Reference Books:

1. Eskel Nordell , Water treatment for industrial and other use ,Rein hold Publishing Corporation, New York.
2. Lloyd A.Munro, Chemistry in Engineering, Prentice-hall, Inc Nj, 2nd Edition.
3. Robert B Leighou Mc Graw, Chemistry of Engineering Materials, Hill Book Company, Inc New York.
4. B.K.Sharma Krishna, Engineering Chemistry, Prakashan media private LTD. 1st Edition, 2014.
5. R.V.Gadag, A.Nityananda Shetty, Engineering Chemistry ,I K International Publishing House New Delhi , First Edition.
6. Fred. Billmeyer Jr., A textbook of polymer science, Wiley India ,Third Edition.

YCCE e- library book links [ACCESSIBLE FROM COLLEGE CAMPUS]

- 1 <http://103.152.199.179/YCCE/Suported%20file/Supprted%20file/SERIES%20WISE%20BOOKS/CHEMISTRY/>

MOOCs Links and additional reading, learning, video material

1. <https://www.youtube.com/watch?v=XTt3gXB0a84>
2. <https://www.youtube.com/watch?v=i1hYXx79QiE>
3. <https://www.youtube.com/watch?v=JfJ7MIP9Dco>
4. <https://www.youtube.com/watch?v=L2VSOccUrSk>
5. <https://www.youtube.com/watch?v=p5pk4Um6lsk>
6. <https://youtu.be/-R7s17hD104>
7. <https://youtu.be/Bmj85Ihfv7w>

			July, 2025	1.00	Applicable for AY 2025-26 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)

(Department of Applied Chemistry)

B.Tech First Year

SoE No.
23FY-101

I/II SEMESTER

23GE1105/23GE1205: Applied Chemistry Lab

Course Objectives (PR)

- 1) Develop analytical ability.
- 2) Integrate chemistry fundamentals with practical applications.

Course Outcomes



Upon successful completion of the course the students will be able to

1. **Apply** the knowledge of quantitative and qualitative chemical analysis to perform record and analyze the results. (L3)
2. **Experiment** with instrumental and analytical techniques in Chemistry to solve engineering problems related to sustainability. (L3)
3. **Write** effective reports and communicate through oral presentations. (L3)
4. **Review** and apply laboratory safety protocols and procedures to acquire the ability for independent and lifelong learning. (L3)

Total 9 experiments are to be performed

(4 each from Lab I and Lab II and one demonstration experiment)

SN	Experiments based on
	List of Experiments-Lab- I
1	Estimation of Nickel.
2	Estimation of Fe^{2+} ions by redox titration
3	Determination of copper by iodometric titration
4	Determination of Cation exchange capacity of an ion exchange resin
5	To determine the strength of a given potassium dichromate solution with N/20 sodium thiosulphate solution
6	Determination of COD of water sample.
	List of Experiments-Lab- II
1	Determination of viscosity of lubricating oil by Redwood Viscometer I or II
2	Determination of molecular weight of a polymer.
3	Proximate analysis of coal

			July, 2025	1.00	Applicable for AY 2025-26 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023



(Scheme of Examination w.e.f. 2023-24 onward)

(Department of Applied Chemistry)

B.Tech in CV/ME/EE/EL/ETC/VLSI

SoE No.
23FY-101

4	Determination of electrochemical equivalence of copper using Faradays Law
5	Determination of strength of the given acid conductometrically.
6	To verify Beer-Lambert law for KMnO_4 calorimetrically and determine the concentration of the given solution of KMnO_4 .
	List of Demonstration Experiments
1	Synthesis of urea formaldehyde.
	Advanced Topics (CBS)
1.	To Determine optimum alum dosage for water or wastewater treatment by turbidity measurement using nephelometer and residual chlorine testing using chloroscope.
2.	Comparative study of effects of different drying techniques on the quality of fruits and vegetables.

			July, 2025	1.00	Applicable for AY 2025-26 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Mathematics & Humanities)

SoE No.
23FY-101

B.Tech First Year

II SEMESTER

23GE1212 : Professional Communication

Course Outcomes :

Upon successful completion of the course the students will be able to:

1. Apply different modes for effective communication
2. Produce competently the Phonology of English language
3. Apply nuances of LSRW skills
4. Practice Communication through different channels

Unit I: Basics of Communication	(6 Hrs.)
Process of Communication, Levels of Communication, Flow of Communication, Networks of Communication, Classification of Barriers (Intrapersonal, Interpersonal, Organizational).	
Unit II: English Phonetics	(7 Hrs.)
Speech Mechanism, Organs of speech, Consonant and Vowels sounds symbols, word stress rules	
Unit III: Presentation & Interview Skills	(6 Hrs.)
Presentation-Nuances of presentation- Kinesics, Proxemics, Chronemics, Vocalics, Modes of Presentation, Interview-Purpose, expectations of employer and preparation for Interview, Types, Types of Questions & Answering Techniques, Telephonic Interviews – preparation and guidelines	
Unit IV: Technical Reports, Memo & E-Mail Etiquettes	(7 Hrs.)
Report -Types, Characteristics, prewriting aspects of report and preparing writing of reports Memo- Objectives, Types, Structure and Layout Email-Etiquette, acronyms.	
Total Lecture	26 Hours

Textbooks:

1.	Meenakshi Raman & Sangeeta Sharma, Technical Communication, Raman & Sharma, Oxford University Press Orford University Press
2.	T. Balasubramaniam, Textbook of English Phonetics for Indian Students, Macmillan India Ltd
3.	

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Mathematics & Humanities)

SoE No.
23FY-101


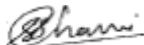
B.Tech First Year

Reference Books:

1.	Dale Carnegie ,How to Develop Self – Confidence & Influence People by Public Speaking
2.	Asha Kaul, Communication Skills
3.	Allen Peas ,Body Language
4.	Gerson's Gerson, Technical Communication

MOOCs Links and additional reading, learning, video material

1.	https://dl.uswr.ac.ir/bitstream/Hannan/141245/1/9781138219120.pdf
2.	https://www.pdfdrive.com/word-power-made-easy-the-complete-handbook-for-building-a-superiorvocabulary-e157841139.html
3.	https://www.pdfdrive.com/improve-your-communication-skills-present-with-confidence-write-with-stylelearn-skills-of-persuasion-e156963640.html
4.	https://www.pdfdrive.com/21-days-of-effective-communication-everyday-habits-and-exercises-to-improveyour-communication-skills-and-social-intelligence-e158273760.html

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Mathematics & Humanities)

SoE No.
23FY-101

B.Tech First Year

II SEMESTER

23GE1215 : Indian Knowledge System

Course Outcomes:

Upon successful completion of the course the students will be able to

1. Apply primary requirements pertaining towards awareness of Indian Knowledge System.
2. Analyze various Indian society, culture and literature to enhance their traditions.
3. Evaluate structure of Indian art.
4. Understand Indian heritage and architectural skills.

Unit:1	Introduction to Indian Civilization	6 Hours
Development of Human Civilization with specific reference: Stone age: Tool Technology and Cultural Development, Indus Valley civilization, Vedic Civilization. (Contemporary Issues related to Topic)		
Unit:2	Indian Society, Culture and Literature	6 Hours
Society and its types, Culture and its Characteristics, Foundational Literature. (Contemporary Issues related to Topic)		
Unit:3	Tradition of Indian Art and Painting	7 Hours
Indian Traditional Painting, Art style folk, mural with Gandhara and Mathura school of art. (Contemporary Issues related to Topic)		
Unit:4	Indic Traditions of Architecture, Design and Planning	7 Hours
Monumental studies of architectural skill: Rock Cut Caves, Stupa and Temple Architecture, The Ancient cities of Indus Saraswati region. Town Planning and drainage system. (Contemporary Issues related to Topic)		
Total Lecture Hours		26 Hours

Textbooks

1	Reader's Digest: Vanished Civilizations, THE READER'S DIGEST ASSOCIATION LIMITED, LONDON,NEWYORK.
2	Qaiser Zoha Alam ; Language and Literature Divers Indian Experience
3	Bal Ram Singh (Author), Nath Girish (Author) ; Science and Technology in Ancient Indian Texts
4	NCERT Books

			July,2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Mathematics & Humanities)

SoE No.
23FY-101

B.Tech First Year

Reference Books


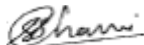
1	B S Harishankar; Art and Archaeology of India: Stone Age to the Present, 2003.
2	Gupte R S and Mahajan B D; Ajanta, Ellora and Aurangabad, 1962.
3	Dharampal, Some Aspects of Earlier Indian Society and Polity and Their Relevance Today, New Quest Publications, Pune, 1987.
4	Michel Lorblanchet, "Rock Art In The Old World" IGNCA series, in India
5	Percy Brown, "Indian Architecture" D. B. Taraporevala sons & co. Pvt. Ltd. Bombay(1959).

PPT's/Research papers

1	https://www.researchgate.net/publication/360889208_STONE_AGE_TOOL_TECHNOLOGY_and_CULTURAL_DEVELOPMENT
2	https://scholar.google.com/citations?view_op=view_citation&hl=en&user=iT1KSV8AAAAJ&sortBy=pubdate&citation_for_view=iT1KSV8AAAAJ:UcHWp8X0CEIC

MOOCs Links and additional reading, learning, video material

1	https://prepp.in/news/e-492-indian-architecture-art-and-culture-notes
2	https://www.artzolo.com/blog/most-famous-indian-painting-styles
3	https://www.researchgate.net/publication/360889332_Stone_Age_Tool_Technology_Cultural_Development
4	https://testbook.com/ias-preparation/ancient-history-16-mahajanapadas

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

SoE No.
23EE-101

B.Tech in Electronics Engineering

II SEMESTER

23EE1205 : Electronics Device and Circuit

Course Outcomes:

Upon successful completion of the course the students will be able to

1. Understand the principles of semiconductor Physics and apply it to electronic devices
2. Appreciate different devices for different applications.
3. Understand and utilize the mathematical models of semiconductor devices for circuits.
4. Understand the basic processes required for fabrication of electronic devices.

Unit:1	Introduction to Semiconductor Physics:	7 Hours
Review of Quantum Mechanics, Electrons in periodic Lattices, E-k diagrams. Energy bands in intrinsic and extrinsic silicon; Carrier transport: diffusion current, drift current, mobility and resistivity.		
Unit:2	Semiconductor Physics for devices:	7 Hours
Generation and recombination of carriers; Poisson and continuity equation, P-N junction characteristics, I-V characteristics, and small signal switching models; Avalanche breakdown, Zener diode, Schottky diode.		
Unit:3	Diode Circuits and applications	7 Hours
Rectifiers, Clippers, Clampers, zener Voltage regulators, LED, photodiode and solar cell.		
Unit:4	Transistors	7 Hours
Bipolar Junction Transistor, I-V characteristics, Ebers Moll Model, MOS capacitor, MOSFET, I-V characteristics, and small signal models of MOS transistor.		
Unit:5	Transistors Biasing	7 Hours
Biasing schemes for BJT and FET amplifiers, bias stability, various configurations (such as CE/CS, CB/CG, CC/CD) and their features.		
Unit :6	Integrated circuit fabrication process:	6 Hours
Oxidation, diffusion, ion implantation, photolithography, etching, chemical vapor deposition, sputtering, twin-tub CMOS process.		
Total Lecture Hours		41 Hours

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023

(Scheme of Examination w.e.f. 2023-24 onward)

(Department of Electronics Engineering)

B.Tech in Electronics Engineering

SoE No.
23EE-101

Textbooks

- | | |
|---|---|
| 1 | G. Streetman, and S. K. Banerjee, Solid State Electronic Devices, 7th edition, Pearson, 2014. |
| 2 | Donald Neamen, Dhrub Biswas "Semiconductor Physics and Devices" McGraw-Hill Education |
| 3 | Jacob Millman, Christos Halkias & Chetan D Parikh, "Integrated Electronics", 2nd Edition, McGraw Hill India, 2017 |

Reference Books

- | | |
|---|---|
| 1 | S. M. Sze and K. N. Kwok, Physics of Semiconductor Devices, 3rd edition, John Wiley & Sons, 2006. |
| 2 | Y. Tsividis and M. Colin, Operation and Modeling of the MOS Transistor. Oxford Univ. Press, 2011. |
| 3 | A.S. Sedra and K.C. Smith, Microelectronic Circuits, Saunders College Publishing, Edition IV |

YCCE e-library book links [ACCESSIBLE FROM COLLEGE CAMPUS]

- | | |
|---|---|
| 1 | http://103.152.199.179/YCCE/yccelibrary.html |
|---|---|

MOOCs Links and additional reading, learning, video material

- | | |
|---|---|
| 1 | https://nptel.ac.in/courses/117103063 |
| 2 | https://nptel.ac.in/courses/108108112 |
| 3 | https://onlinecourses.nptel.ac.in/noc23_ee120/preview |
| 4 | https://nptel.ac.in/courses/108107142 |

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023

(Scheme of Examination w.e.f. 2023-24 onward)

(Department of Electronics Engineering)

B.Tech in Electronics Engineering

**SoE No.
23EE-101**

II SEMESTER

23EE1206 : Lab. Electronics Device and Circuit

Course Outcomes:

Upon successful completion of the course the students will be able to

1. Understand the principles of semiconductor Physics and apply it to electronic devices
2. Appreciate different devices for different applications.
3. Understand and utilize the mathematical models of semiconductor devices for circuits.
4. Understand the basic processes required for fabrication of electronic devices.

Sr. No.	Experiments based on
1	To plot the V- I characteristics of PN junction diode (Si and Ge) using breadboard and on experimental kit.
2	To plot the V- I characteristics of Zener diode.
3	To study half wave and full wave rectifier with and without capacitive filter.
4	To perform the clipper and clamper circuit using breadboard.
5	To plot I/P & O/P Characteristics of Common Base Transistor Configuration. Find I/P & O/P Resistance and Current Gain.
6	To plot I/P & O/P Characteristics of Common Emitter Transistor Configuration. Find I/P & O/P Resistance and Current Gain.
7	To perform the Drain and Transfer characteristics of Field Effect Transistor (FET).
8	To perform the Fixed Bias circuit of transistor.
9	To perform the Self Bias circuit of transistor

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023

(Scheme of Examination w.e.f. 2023-24 onward)

(Department of Information Technology)

B.Tech in Information Technology

**SoE No.
23IT-101**

II SEMESTER

23IT1203 : Programming for Problem Solving

Course Outcomes :

- 1) Understand the basics of computer system operations and algorithms, flowcharts.
- 2) Apply the basics of C programming for problem solving.
- 3) Apply and analyze the different dimensional arrays for problem solving.
- 4) Understand the basics of string, structure, and union and apply them to problem solving.

Unit I: Computer System Basics:

(3 Hrs.)

Basics of programming and problem solving. Introduction to algorithms and flowcharts, Types of programming errors, basic input/output statements and functions (scanf, printf, getch, putch, gets, puts), Introduction to library functions,

Unit II: Basic of C Programming

(6 Hrs.)

Basic building blocks of C: Character set, variables, identifiers & keywords, Data types, Operators: arithmetic, logical and relational operators, , bitwise operators, precedence of operators, Expressions, sizeof() operator, constants, typedef statement, writing straight line programs. Decision control statements: if, if - else and nested if-else statements, else-if ladder statement, switch-case control statement.

Unit III: Loop Structures:

(5 Hrs.)

While, do while and for loops, break and continue statement, “goto” statement, real life programming examples based on these loop structures, real life programming examples.

Unit IV: Modular Programming:

(6 Hrs.)

Concept of functions, user defined functions, function prototypes, formal parameters, actual parameters, return types, call by value , call by reference, C programs using functions, Recursive functions, comparing recursion against iteration, C programs using recursive functions, real life programming examples

Unit V: Arrays:

(6 Hrs.)

One dimensional array, array manipulation, insertion, deletion of an element, searching techniques- Linear and binary search, sorting technique – Bubble sort. Two-dimensional arrays: matrix representation, programs for basic matrix operations such as addition, multiplication and transpose, Array as function arguments. real life programming examples

Unit VI: String, Structure and Union:

(4 Hrs.)

Strings: string representation and string handling functions, Introduction to pointer, structure and union. real life programming examples

Total Lecture 30 Hours

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023

(Scheme of Examination w.e.f. 2023-24 onward)

(Department of Information Technology)

B.Tech in Information Technology

SoE No.
23IT-101

Text books

1	The C Programming Language, J.B.W.Kernighan & D.M.Ritchie, Prentice Hall
2	Mastering C, K.R.Venugopal & S.R. Prasad, TMH, 2007.
3	Programming in ANSI C, E. Balaguruswamy, Mc Graw Hill Education

Reference Books

1	Problem Solving And Program Design In C, Jeri. R. Hanly, Elliot B. Koffman, Pearson Education.
2	Programming with C, Byron Gottfried, Schaum;s Outline Series
3	How to solve it by computers, R. G. Dromey, Prentice Hall India

YCCE e- library book links [ACCESSIBLE FROM COLLEGE CAMPUS]

1	http://103.152.199.179/YCCE/Suported%20file/Supprted%20file/e-copies%20of%20books
---	---

MOOCs Links and additional reading, learning, video material

1	https://nptel.ac.in/courses/106104128
2	https://nptel.ac.in/courses/106104128
3	https://www.youtube.com/watch?v=rQoqCP7LX60&list=PLxgZQoSe9cg1drBnejUaDD9GEJBGQ5hMt

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023

(Scheme of Examination w.e.f. 2023-24 onward)

(Department of Information Technology)

B.Tech in Information Technology

**SoE No.
23IT-101**

II SEMESTER

23IT1204 : Lab. Programming for Problem Solving

Course Outcomes: Students will be able to

- 1) Understand the basics of computer system operations and algorithms, flowcharts.
- 2) Apply the basics of C programming for problem solving.
- 3) Apply and analyze the different dimensional arrays for problem solving.
- 4) Understand the basics of string, structure, and union and apply them to problem solving.

Unit I: Computer System Basics:	(3 Hrs.)
Basics of programming and problem solving. Introduction to algorithms and flowcharts, Types of programming errors, basic input/output statements and functions (scanf, printf, getch, putch, gets, puts), Introduction to library functions,	
Unit II: Basic of C Programming	(6 Hrs.)
Basic building blocks of C: Character set, variables, identifiers & keywords, Data types, Operators: arithmetic, logical and relational operators, , bitwise operators, precedence of operators, Expressions, sizeof() operator, constants, typedef statement, writing straight line programs. Decision control statements: if, if - else and nested if-else statements, else-if ladder statement, switch-case control statement.	
Unit III: Loop Structures:	(5 Hrs.)
While, do while and for loops, break and continue statement, “goto” statement, real life programming examples based on these loop structures, real life programming examples.	
Unit IV: Modular Programming:	(6 Hrs.)
Concept of functions, user defined functions, function prototypes, formal parameters, actual parameters, return types, call by value , call by reference, C programs using functions, Recursive functions, comparing recursion against iteration, C programs using recursive functions, real life programming examples	
Unit V: Arrays:	(6 Hrs.)
One dimensional array, array manipulation, insertion, deletion of an element, searching techniques- Linear and binary search, sorting technique – Bubble sort. Two-dimensional arrays: matrix representation, programs for basic matrix operations such as addition, multiplication and transpose, Array as function arguments. real life programming examples	
Unit VI: String, Structure and Union:	(4 Hrs.)
Strings: string representation and string handling functions, Introduction to pointer, structure and union. real life programming examples	
Total Lecture	30 Hours

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023

(Scheme of Examination w.e.f. 2023-24 onward)

(Department of Information Technology)

B.Tech in Information Technology

SoE No.
23IT-101

Text books

1	The C Programming Language, J.B.W.Kernighan & D.M.Ritchie, Prentice Hall
2	Mastering C, K.R.Venugopal & S.R. Prasad, TMH, 2007.
3	Programming in ANSI C, E. Balaguruswamy, Mc Graw Hill Education

Reference Books

1	Problem Solving And Program Design In C, Jeri. R. Hanly, Elliot B. Koffman, Pearson Education.
2	Programming with C, Byron Gottfried, Schaum;s Outline Series
3	How to solve it by computers, R. G. Dromey, Prentice Hall India

YCCE e- library book links [ACCESSIBLE FROM COLLEGE CAMPUS]

1	http://103.152.199.179/YCCE/Suported%20file/Supprted%20file/e-copies%20of%20books
---	---

MOOCs Links and additional reading, learning, video material

1	https://nptel.ac.in/courses/106104128
2	https://nptel.ac.in/courses/106104128
3	https://www.youtube.com/watch?v=rQoqCP7LX60&list=PLxgZQoSe9cg1drBnejUaDD9GEJBGQ5hMt

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Information Technology)

**SoE No.
23IT-101**

B.Tech in Information Technology

List of Practical

SN	Unit	Name Of The Practical	Remark	CO'S Mapped	PO'S Mapped
1(A)		Introduction to Linux Operating system & it's different commands.	Manual	CO 1	PO1
1(B)		Introduction to Vi editor, Compilation and Execution of a program in Linux.	Manual	CO 1	PO1
2	II	Practical based on Arithmetic and Conditional operators.	Operators	CO 1	PO1
3	II	Practical based on Conditional and Unconditional Statements.	Conditional Statements	CO 1	PO1
4	III	Practical based on Entry Controlled Looping Statements.	For / While Loop	CO 2	PO 1, PO 2
5	III	Practical based on Exit Controlled Looping Statement	Do while Loop	CO 2	PO 1, PO 2
6	IV	Practical based on Functions and Recursion.	Functions / Recursion	CO 3	PO2, PO3
7	V	Practical based on 1-D Array.	1D Array	CO 3	PO2, PO3
8	V	Practical based on 2-D Array.	2D Array	CO 3	PO2, PO3
9	VI	Practical based on Strings.	Strings & Pointers	CO 3	PO2, PO3
10	VI	Practical based on Structures.	Structures	CO 4	PO1, PO2, PO3

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Mathematics & Humanities)

SoE No.
23FY-101

B.Tech First Year

II SEMESTER

23GE1218 : Functional English

Course Outcomes:

Upon successful completion of the course the students will be able to

1. Understand the concept of FE (Functional English) and its application in various real-life scenarios.
2. Develop basic interactive communication skills, including greetings, asking for information, stating opinions, and providing feedback.
3. Acquire knowledge of social networking, texting, instant messaging, blogs, and discussion boards, along with the ethical considerations associated with online communication.
4. Successfully complete quizzes and assignments assessing knowledge in the covered topics of FE, social media, tenses, and effective communication.

Unit:1	Introduction to Functional English	6 Hours
What is FE? And Areas of application. Basic Interactive sentences - Greetings & Replies, Asking for information, Telling people what you do, Asking somebody's opinion, Giving your opinion, Saying someone is correct, Saying that someone is wrong, Apologizing, Praising someone's work, Saying goodbye. Introduction & Basics of Common Expressions – Offer, Request, Gratitude, Apology. Modal Verbs - Words used often: Can- could, Will – would, Shall – should, Ought to-Must, May-might. Practice exercises, Practice Conversations, Script Activity		
Unit:2	Internet & Social Media Communication	6 Hours
Introduction & Basics to Social Networking, Texting & Instant messaging, Blogs & Discussion Board- discussion with examples, Ethics of social media & communication Topic: Introduction to Creative Ads Why Ads, What's in it for me? Characteristics of ads. Assignment Quiz on the above Topics, Exercises for Evaluation		
Unit:3	TENSES	6 Hours
Introduction & Basics, Simple Tense (Past, Present, Future), Continuous Tense (Past, Present, Future) – discussion with examples. Introduction & Basics, Perfect Tense (Past, Present, Future), Perfect Continuous Tense (Past, Present, Future) – discussion with examples Introduction to Movie Magic, Learn English with films, Film Vocabulary, Describing a film, Types of Films Assessment – Letter and Email Writing, Tenses – Quiz		
Unit:4	Written Communication	5 Hours
Introduction & Basics of Writing, five methods of communication, Mind your grammar, Commonly confusing words Letters – Format, Parts of a business letter, When does communication fail?, Things to remember, Positive language not negative language, Active voice not passive voice Effective emailing -How to make an effective e-mail, Few common e-mail habits that cause problems, Parts of an e-mail, Some other important aspects.		

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Mathematics & Humanities)

SoE No.
23FY-101

B.Tech First Year

Assignment Presentation on Mad Ads, Quiz on Tenses and social media-Internet Communication
Topic: Activity Extempore

EVALUATION			1 Hour
WRITTEN TEST	TA=60	ESE=40	TOTAL=100
Total Lecture Hours			24 Hours

Reference Books

- 1 How to win friends & influence people – Dale Carnegie
2. Functional English for Communication - Ujjwala Kakarla
- 3 Functional English for Technical Students – Dr Prathibha Mahato & Dr Dora Thompson

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	

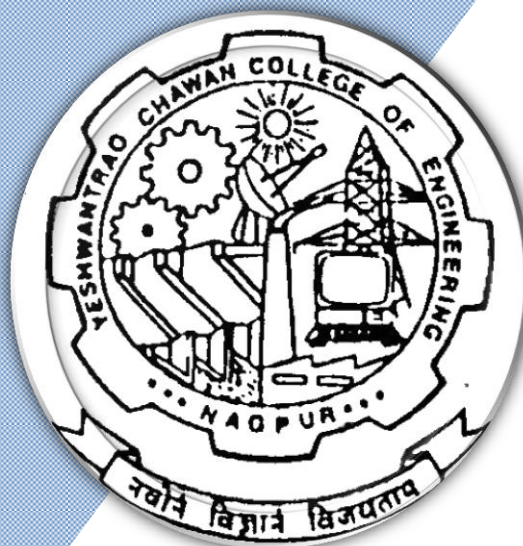
Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

(Accredited 'A++' Grade by NAAC with a score of 3.6)

Hingna Road, Wanadongri, Nagpur - 441 110



Bachelor of Technology SoE & Syllabus 2023 3rd Semester

(Department of Electronics Engineering)

B. Tech in VLSI



Nagar Yuwak Shikshan Sanstha's
Yeshwantrao Chavan College of Engineering
 (An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)
B.TECH SCHEME OF EXAMINATION 2023
 (Scheme of Examination w.e.f. 2023-24 onward)
 (Department of Electronics Engineering)
B. Tech Electronics Engineering(VLSI Design and Technology)

SoE No.
23VLSI-101

SN	Sem	Type	BoS/ Deptt	Sub. Code	Subject	T/P	Contact Hours				Credits	% Weightage			ESE Duration Hours
							L	T	P	Hrs		MSEs*	TA**	ESE	
THIRD SEMESTER															
1	3	HSSM-1	GE	23GE1301	Fundamentals of Management & Economics	T	2	0	0	2	2	30	20	50	3
2	3	PC	EE	23VLS1301	Analog Circuits	T	3	0	0	3	3	30	20	50	3
3	3	PC	EE	23VLS1302	Lab : Analog Circuits	P	0	0	2	2	1		60	40	
4	3	PC	EE	23VLS1303	Network Analysis	T	3	0	0	3	3	30	20	50	3
5	3	PC	EE	23VLS1304	Lab : Network Analysis	P	0	0	2	2	1		60	40	
6	3	PC	EE	23VLS1305	Signal and Systems	T	3	0	0	3	3	30	20	50	3
7	3	VEC-2	EE	23VLS1306	Basics of Python Programming	T	2	0	0	2	2	30	20	50	3
8	3	CEP	EE	23VLS1307	Community Engagement Project	P	0	0	2	4	2		60	40	
9	3	OE-1	OE		Open Elective-I	T	2	0	0	2	2	30	20	50	3
10	3	MDM	MDM		MD Minor Course-I	T	2	0	0	2	2	30	20	50	3
TOTAL							17	0	6	25	21				

List of Mandatory Learning Course (MLC)

1	3	HS	T&P	MLC2123	YCAP3 : YCCE Communication Aptitude Preparation	A	3	0	0	3	0				
---	---	----	-----	---------	---	---	---	---	---	---	---	--	--	--	--

Open Elective - I

SN	Sem	Type	BoS / Deptt	Sub. Code	Subject
1	3	OE1	GE	23OE1301	OE-I : Combinatorics
2	3	OE1	GE	23OE1302	OE-I : Fuzzy Set Theory, Arithmetic And Logic
3	3	OE1	GE	23OE1303	OE-I : Green Chemistry & Sustainability
4	3	OE1	GE	23OE1304	OE-I : Hydrogen Fuel
5	3	OE1	GE	23OE1305	OE-I : Electronic Materials And Applications
6	3	OE1	GE	23OE1306	OE-I : Laser Technology And Applications
7	3	OE1	MGT	23OE1307	OE-I : Finance And Cost Management
8	3	OE1	MGT	23OE1308	OE-I : Operation Research Techniques
9	3	OE1	MGT	23OE1309	OE-I : Project Evaluation & Management
10	3	OE1	MGT	23OE1310	OE-I : Total Quality Management
11	3	OE1	MGT	23OE1311	OE-I : Value Engineering
12	3	OE1	MGT	23OE1312	OE-I : Maintenance Management
13	3	OE1	MGT	23OE1313	OE-I : Industrial Safety
14	3	OE1	MGT	23OE1314	OE-I : Industry 4.0
15	3	OE1	MGT	23OE1315	OE-I : Operation Management
16	3	OE1	MGT	23OE1316	OE-I : Material Management
17	3	OE1	MGT	23OE1317	OE-I : Hospitality Management
18	3	OE1	MGT	23OE1318	OE-I : Human Resource Management & Organizational Behaviour
19	3	OE1	MGT	23OE1319	OE-I : Agri-Business Management
20	3	OE1	MGT	23OE1320	OE-I : Rural Marketing
21	3	OE1	MGT	23OE1321	OE-I : Marketing Management
22	3	OE1	MGT	23OE1322	OE-I : Health Care Management
23	3	OE1	MGT	23OE1323	OE-I : Designated approved online NPTEL/KKSU Course
24	3	OE1	MGT	23OE1324	OE-I : Indian Archeology
25	3	OE1	MGT	23OE1325	OE-I : Social & Positive Psychology
26	3	OE1	MGT	23OE1326	OE-I : Seismology & Earthquake

		July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

SoE No.
23VLSI-101

B.Tech in V.L.S.I.

III SEMESTER

23GE1301: Fundamentals of Management & Economics

Course Outcomes:

Upon successful completion of the course the students will be able to

1. Develop the Managerial Perspective and perform the various functions of management for optimum utilization of Engineering Resources
2. Identify and Analyze the role of Financial Accountancy and Marketing Management in the Organization
3. Develop perspective about economy based on logical reasoning and estimate the economic outcomes.
4. Interprets comparative advantage of resources.

Unit I:

7 Hrs.

Principles of Management: Evolution of Management Thought: Scientific and Administrative Theory of Management, Definition and Concept of Management, Functions of Management: Planning, Organizing, Directing, Staffing and Controlling, Motivational Theories, Concept of Leadership.

Unit II:

8 Hrs.

Marketing and Financial Management: Marketing and Financial Management –Marketing Theories and Concept-Marketing Mix, Market Segmentation, Targeting and Positioning and Functions Financial Management and Accountancy- Accountancy Rules and Capital, Preparation of Books of Account- Journal posting of Transaction into ledger and preparation of trial Balance, Introduction of Trading Account, Profit and loss account and balance sheet.

Unit III:

7 Hrs.

Introduction to Microeconomics: Nature and Scope of Microeconomics, Demand Analysis: Meaning and determinants of demand, law of demand, Elasticity of Demand - types and degrees, Utility analysis, Law of diminishing marginal utility, supply- law of supply, Law of Variable proportions and Return to Scale, Classification of market structure.

Unit IV:

8 Hrs.

Introduction to Macroeconomics: Nature and Scope of Macroeconomics, Concept of GDP, GNP, NDP, NNP, Measurement of GDP; Economic Growth and development, Money – definition, types and function of money, Inflation – meaning, types, causes and measure to control, concept of deflation, functions of central and commercial bank, Sources of public revenue - direct and indirect taxes.

Total Lecture 30 Hours

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

SoE No.
23VLSI-101

B.Tech in V.L.S.I.

Textbooks:

1	Principle of Management, 9 th edition, Harold Koontz Ramchandra, Tata McGraw hills
2	Marketing Management: Planning, Implementation and Control, 3 rd Edition, Ramaswamy V.S. and Namakumari S, Macmillian
3	Fundamentals of Accounting Gupta R.L. & Radhaswamy ;
4	Modern Economics, 13 th Edition, H. L. Ahuja, S. Chand Publisher, 2009
5	Modern Economic Theory, 3 rd edition, K. K. Devett, S. Chand Publisher, 2007
6	Principle of Economics, 7 th edition, Mankiw N. Gregory, Thomson, 2013

Reference Books:

1	Foundations of Financial Markets and Institutions, 3 rd Edition, Fabozzi, Prentice Hall
2	Fundamentals of Financial Instruments, 2 nd Edition, Parameshwaran, Wiley India
3	Marketing Management, 3 rd Edition, Rajan Saxena, Tata McGraw Hill
4	Advance Economic Theory, 17 th Edition, H. L. Ahuja, S. Chand Publisher, 2009
5	International Trade, 12 th edition, M. L. Zingan, Vindra Publication, 2007
6	Macro Economics, 11 th edition, M. L. Zingan, Vindra Publication, 2007
7	Monitory Economics, 1 st Edition, M. L. Sheth, Himayalaya Publisher, 1995

YCCE e- library book links [ACCESSIBLE FROM COLLEGE CAMPUS]

1	http://link.springer.com/openurl?genre=book&isbn=978-1-4613-6193-0
2	https://onlinelibrary.wiley.com/doi/book/10.1002/9780470168042

MOOCs Links and additional reading, learning, video material

1	https://onlinecourses.nptel.ac.in/noc22_mg104/preview
2	https://archive.nptel.ac.in/courses/110/101/110101131/
3	https://onlinecourses.nptel.ac.in/noc23_mg122/preview
4	https://onlinecourses.nptel.ac.in/noc21_hs52/preview
5	https://onlinecourses.nptel.ac.in/noc22_hs67/preview

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

SoE No.
23VLSI-101

B.Tech in V.L.S.I.

III SEMESTER 23VLS1301: Analog Circuits

Course Outcomes:

Upon successful completion of the course the students will be able

1. Understand different circuit configuration of different devices for various applications.
2. Design circuits by using appropriate device models
3. Design various analog circuits required in electronic systems.
4. Design mixed circuits such as ADC and DACs

Unit:1	Amplifier models: Voltage amplifier, current amplifier, trans-conductance amplifier and trans-resistance amplifier. Small signal analysis, low frequency transistor models, estimation of voltage gain, Current gain, input resistance, output resistance.	8 Hours
Unit:2	Amplifier at high frequency: High frequency transistor models, frequency response of single stage and multistage amplifiers, Feedback topologies: Voltage series, current series, voltage shunt, current shunt, effect of feedback on gain, bandwidth etc., calculation with practical circuits, concept of stability, gain margin and phase margin.	7 Hours
Unit:3	Oscillators: Review of the basic concept, Barkhausen criterion, RC oscillators (phase shift, Wien bridge etc.), LC oscillators (Hartley, Colpitt, Clapp etc.)	8 Hours
Unit:4	Differential amplifier: Basic structure and principle of operation, calculation of differential gain, common mode gain, CMRR and ICMR, Constant Current Sources, Current Mirror: Basic topology and its variants, Design of differential amplifier for a given specification	7 Hours
Unit:5	OP-AMP applications: Review of inverting and non-inverting amplifiers, integrator and differentiator, summing amplifier, precision rectifier, Schmitt trigger and its applications.	8 Hours
Unit :6	Digital-to-analog converters (DAC): Weighted resistor, R-2R ladder, resistor string etc. Analog-to-digital converters (ADC): Single slope, dual slope, successive approximation, flash etc. Switched capacitor circuits: Basic concept, practical configurations, application in amplifier, integrator, ADC etc.	7 Hours
Total Lecture Hours		45 Hours

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

SoE No.
23VLSI-101

B.Tech in V.L.S.I.

Textbooks

- | | |
|---|---|
| 1 | Millman & Halkies, "Electronic Device and Circuits", 2 nd Edition, Tata McGraw Hill. |
| 2 | Boylestead & Nashelsky, "Electronic devices and Circuits Theory" 8 th edition, PHI |
| 3 | Linear Integrated Circuits, S. Salivahanan, V. S. Bhaaskaran, 3 rd Edition, Tata McGraw Hill Publication |

Reference Books




- | | |
|---|---|
| 1 | Millman Halkies, "Integrated Electronics", Tata McGraw Hill. |
| 2 | A.S. Sedra and K.C. Smith, "Microelectronic Circuits", 4 th Edition, Saunder's College Publishing, |
| 3 | D Roy Choudhary, Shail Bala Jain, "Linear Integrated Circuits", 5 th Edition, New Age International Publishers |
| 4 | Ramakant A. Gayakwad, "Op-amps and Linear Integrated Circuits", 3 rd Edition, , Prentice Hall Publication |

YCCE e- library book links [ACCESSIBLE FROM COLLEGE CAMPUS]

- | | |
|---|---|
| 1 | http://103.152.199.179/YCCE/yccelibrary.html |
|---|---|

MOOCs Links and additional reading, learning, video material

- | | |
|---|---|
| 1 | http://nptel.iitm.ac.in/video.php?subjectId=117103063 |
| 2 | NPTEL Video: mod07lec29: BJT |
| 3 | https://archive.nptel.ac.in/courses/108/108/108108111/# |

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

B.Tech in V.L.S.I.

SoE No.
23VLSI-101

III SEMESTER 23VLS1302: Lab. Analog Circuits

Course Outcomes:

Upon successful completion of the course the students will be able

1. **Understand** different circuit configuration of different devices for various applications.
2. **Design** circuits by using appropriate device models
3. **Design** various analog circuits required in electronic systems.
4. **Design** mixed circuits such as ADC and DACs
5. Use simulation tools and hardware to **implement** experiments on analog circuits

Sr. No.	Experiments based on
1	To Plot the Frequency Response of a single stage RC coupled CE amplifier at low frequency
2	To Plot the Frequency Response of a single stage RC coupled CE amplifier at high frequency
3	Simulation of Differential Amplifier configuration using LTSpice
4	IC 741 OP-AMP as a inverting amplifier / non-inverting amplifier with frequency response
5	Different OPAMP parameters: CMRR, Slew rate of OP-AMP.
6	IC 741 OP-AMP as a Integrator.
7	IC 741 OP-AMP as a Differentiator.
8	OP-AMP IC 741 as a Astable Multivibrator.
9	OP-AMP IC 741 as a Monostable Multivibrator.
10	OP-AMP IC 741 as a Schmitt trigger.

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

SoE No.
23VLSI-101

B.Tech in V.L.S.I.

III SEMESTER

23VLS1303: Network Analysis

Course Outcomes:

Upon successful completion of the course the students will be able to

1. **Define, understand and explain** concepts related to electrical networks.
2. **Apply** the knowledge of network theorems to the electrical networks to acquire the desired parameter.
3. **Understand and analyze** electrical circuits in transform domain.
4. **Apply** the concept of two – port networks to **evaluate** different two-port parameters.
5. **Analyze** network concepts using EDA Tool.

Unit:1	Nodal Analysis of Electric Circuits	8 Hours
Basics of electric circuits, circuit elements and their voltage – current relationship, classification of circuit elements, sources - their types and characteristics, concept of equivalent sources, source transformation and duality, concept of supernode, nodal analysis of circuits containing resistors, inductors, capacitors, transformers, and both independent and dependent sources to determine current, voltage and power.		
Unit:2	Mesh Analysis of Electric Circuits	7 Hours
Mesh Analysis, Concept of super mesh, mutual inductance, coefficient of coupling, dot convention, dot marking in coupled coils, mesh analysis of circuits containing resistors, inductors, capacitors, transformers, and both independent and dependent sources to determine current, voltage and power.		
Unit:3	Network Theorem	9 Hours
Superposition Theorem, Thevenin's Theorem, Norton's Theorem, Maximum Power Transfer Theorem		
Unit:4	Initial and Final Conditions, Impedance Functions and Circuit Analysis with Laplace Transform	7 Hours
Concept of initial and final conditions, behaviour of resistor, inductor and capacitor at $t = 0^-$ and at $t = 0^+$, procedure for evaluating initial and final conditions, analytical treatment. Review of Laplace Transform, transform impedance and admittance, s – domain impedance and admittance models for resistor, inductor and capacitor, series and parallel combinations of elements. Transformed network on loop and mesh basis, mesh and node equations for transformed networks, time response of electrical network with and without initial conditions by Laplace transform.		
Unit:5	Transforms of other Signal Waveforms, Network Functions, Poles and Zeros of network functions	7 Hours
Unit step, ramp and impulse functions with and without time delay, their Laplace transform, waveform synthesis and its application to electrical networks. Terminal pairs or ports, network functions for one port and two port networks, definition and physical interpretation of poles and zeros, pole-zero plot for network functions, restrictions on pole and zero locations for driving point and transfer functions, time domain behaviour from the pole – zero plot, network synthesis using pole – zero plot.		

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

B.Tech in V.L.S.I.

SoE No.
23VLSI-101

Unit :6	Two Port Parameters	7 Hours
Standard reference directions for the voltages and currents of a two – port network, defining equations for open circuit impedance, transmission, inverse transmission, hybrid and inverse hybrid parameters, relationships between parameter sets, conditions for reciprocity and electrical symmetry in terms of two – port parameters, interconnections of two - port networks.		
Total Lecture Hours		45 Hours

Text books	
1	M.E.VanValkenburg, Network Analysis, 3 rd Edition, PHI Learning Private Limited.
Reference Books	
1	Sudhakar,A.,Shyammoan,S.P., Circuits and Network, Tata McGraw-Hill New Delhi
2	A William Hayt ,Engineering Circuit Analysis,8th Edition, McGraw-Hill Education.
YCCE e- library book links [ACCESSIBLE FROM COLLEGE CAMPUS]	
1	http://103.152.199.179/YCCE/yccelibrary.html
MOOCs Links and additional reading, learning, video material	
1	https://nptel.ac.in/courses/108105159
2	https://archive.nptel.ac.in/courses/108/105/108105159/

			July,2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

B.Tech in V.L.S.I.

SoE No.
23VLSI-101

III SEMESTER 23VLS1304: Lab. Network Analysis

Course Outcomes:

Upon successful completion of the course the students will be able to

1. **Define, understand** and **explain** concepts related to electrical networks.
2. **Apply** the knowledge of network theorems to the electrical networks to acquire the desired parameter.
3. **Understand** and **analyze** electrical circuits in transform domain.
4. **Apply** the concept of two – port networks to **evaluate** different two-port parameters.
5. **Analyze** network concepts using EDA Tool.

Sr. No.	Experiments based on
1	Introduction to PSPICE and Perform nodal analysis on simple electrical circuits.
2	Perform nodal analysis on electrical circuits with dependent energy sources.
3	Perform mesh analysis on simple electrical circuits.
4	Perform mesh analysis on electrical circuits with dependent energy sources.
5	Verification of Superposition Theorem.
6	Verification of Thevenin's Theorem.
7	Verification of Norton's Theorem.
8	Verification of Maximum Power Transfer Theorem.
9	Perform nodal analysis on RLC circuits.
10	Perform mesh analysis on RLC circuits.

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

B.Tech in V.L.S.I.

SoE No.
23VLSI-101

III SEMESTER

23VLS1305: Signal and Systems

Course Outcomes:

Upon successful completion of the course the students will be able to

1. Classify continuous time signals and systems, transformation of independent variable.
2. Analyse Fourier series, Fourier transform representation of continuous-time periodic and aperiodic signals.
3. Determine and evaluate Laplace Transform of continuous time signals.
4. Analyze time & frequency characterization of Signals and Systems & Sampling

Unit:1	Continuous time and discrete time signals: Signal representation, Transformation of the independent variable, classification of signals, Signal Energy and Power, Periodic, Even & Odd, Real and Exponential Signals	8 Hours
Unit:2	Continuous and Discrete time System Continuous-Time Systems, system properties: linearity: additivity and homogeneity, shift-invariance, causality, stability, convolution	8 Hours
Unit:3	Fourier Series Representation of Periodic Signals Fourier Series Representation of Continuous-Time Periodic Signals, convergence of the Fourier Series.	7 Hours
Unit:4	Fourier Transform: Convergence of Fourier Transform and its Properties, Representation of Aperiodic Signals, The Fourier Transform for Periodic Signals. Analysis and Characterization of LTI Systems using the Fourier Transform.	7 Hours
Unit:5	The Laplace Transform: The Region of Convergence for Laplace Transforms. The Inverse Laplace Transform. Properties of the Laplace Transform. Analysis and Characterization of LTI Systems Using the Laplace Transform. The Unilateral Laplace Transform	8 Hours
Unit :6	The Z Transform. The Region of Convergence for Z Transforms. The Inverse Z Transform. Properties of the Z Transform. Analysis and Characterization of LTI Systems Using the Z Transform	7 Hours
Total Lecture Hours		45 Hours

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

B.Tech in V.L.S.I.

SoE No.
23VLSI-101

Text books

1	Signals and Systems, Alan V. Oppenheim, Alan S. Willsky, with S. Hamid, 2nd Edition, 1996, Prentice Hall
2	Digital signal processing –Principles, algorithms and applications, J. G. Proakis, D. G. Manolakis, 3rd Edition, 1996, PHI

Reference Books

1	Outline of Signals and Systems, Hwei Hsu, Schaum's, 1st Ed 1995, McGraw-Hill
2	Signals & Systems, Simon Haykin and Van Veen 2nd Edition, 2002 Wiley
3	Signals & Systems, I.J.Nagrath, S.N.Sharan, R.Ranjan, S.Kumar, 2001 Pearson education

YCCE e- library book links [ACCESSIBLE FROM COLLEGE CAMPUS]

1	http://103.152.199.179/YCCE/yccelibrary.html
---	---

MOOCs Links and additional reading, learning, video material

1	https://onlinecourses.nptel.ac.in/noc21_ee2
2	https://archive.nptel.ac.in/courses/108/104/108104100/

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

B.Tech in V.L.S.I.

SoE No.
23VLSI-101

III SEMESTER

23VLS1306: Basics of Python Programming

Course Outcomes:

Upon successful completion of the course the students will be able to

1. Interpret the fundamental Python syntax and semantics and be fluent in the use of Python control flow statements.
2. Express proficiency in the handling of strings and functions.
3. Determine the methods to create and manipulate Python programs by utilizing the data structures like lists, dictionaries, tuples and sets.

Unit:1	5 Hours
Introduction to Python Programming Language, Identifiers, Keywords, Statements and Expressions, Variables, Operators, Data Types, Indentation, Comments, Reading Input, Print Output, Type Conversions, The type() Function and Is Operator.	
Unit:2	5 Hours
Control Flow Statements, The if Decision Control Flow Statement, The if...else Decision Control Flow Statement, The if...elif...else Decision Control Statement, Nested if Statement, The while Loop, The for Loop, The continue and break Statements,	
Unit:3	5 Hours
Strings, Creating and Storing Strings, Basic String Operations, Accessing Characters in String by Index Number, String Slicing and Joining, String Methods, Formatting Strings, Lists, Creating Lists, Basic List Operations, Indexing and Slicing in Lists, Built-In Functions Used on Lists, List Methods, The del Statement.	
Unit:4	5 Hours
Dictionaries, Creating Dictionary, Accessing and Modifying key:value Pairs in Dictionaries, Built-In Functions Used on Dictionaries, Dictionary Methods, The del Statement,	
Unit:5	5 Hours
Tuples and Sets, Creating Tuples, Basic Tuple Operations, Indexing and Slicing in Tuples, Built-In Functions Used on Tuples, Relation between Tuples and Lists, Relation between Tuples and Dictionaries, Tuple Methods, Using zip() Function, Sets, Set Methods, Traversing of Sets, Frozenset	
Unit :6	5 Hours
Visualizing Information: what is data visualization, use of Pyplot Matplotlib Library, Creating Line charts and scatter plot, Creating bar charts and Pie Charts, Customizing the plots, Creating Histogram with PyPlot and other library, Creating Frequency Polygons, Creating Box plot, Plotting data from Data frame.	
Total Lecture Hours	
30 Hours	

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

B.Tech in V.L.S.I.

SoE No.
23VLSI-101

Text books

- | | |
|---|--|
| 1 | "Introduction to Python Programming", 1st Edition, Gowrishankar S, Veena A CRC Press/Taylor & Francis. |
|---|--|

Reference Books

- | | |
|---|---|
| 1 | "Python Data Science Handbook: Essential Tools for Working with Data", 1st Edition, Jake VanderPlas, O'Reilly Media |
| 2 | "Core Python Applications Programming", 3rd Edition, Wesley J Chun, Pearson Education |

YCCE e- library book links [ACCESSIBLE FROM COLLEGE CAMPUS]

- | | |
|---|---|
| 1 | http://103.152.199.179/YCCE/yccelibrary.html |
|---|---|

MOOCs Links and additional reading, learning, video material

- | | |
|---|---|
| 1 | https://www.python.org/ |
| 2 | https://www.w3schools.com/python/ |
| 3 | https://www.geeksforgeeks.org/python-programming-language/ |

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

B.Tech in V.L.S.I.

SoE No.
23VLSI-101

III SEMESTER

23VLS1307: Lab : Sensor based mini project and report writing

Course Outcomes:

Upon successful completion of the course the students will be able to

1. Develop a deeper understanding of the importance of healthy living and its impact on overall well-being.
2. Develop a sense of community and belonging among participants through collaborative activities and shared experiences.
3. Make positive lifestyle changes and will be equipped with resources

Sr. No.	Experiments based on (Sensor based mini project and report writing)
1	Soiling testing project (MSPA-1)
2	Temperature and Humidity testing project (MSPA-2)
3	Air pollution related project (MSPA-3)
4	Solar power related project (MSPA-4)

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's
Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

B.Tech in V.L.S.I.

SoE No.
23VLSI-101

III SEMESTER
Multidisciplinary Minor Courses

Track 1
MDMT1VLS101 : Digital VLSI

Courses	Sem	MDMT1VLS101 : Digital VLSI
MDM-I	3	(MDM1VLS101) Introduction to electronic Components
MDM-II	4	(MDM2VLS102) Introduction to Digital Logic
MDM-III	5	(MDM3VLS103) Switching Theory
MDM-IV	6	(MDM4VLS104) Digital System Design
MDM-V	7	(MDM5VLS105) Computer Architecture
MDM-VI	8	(MDM6VLS106) Data acquisition and signal conditioning

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

B.Tech in V.L.S.I.

SoE No.
23VLSI-101

III SEMESTER

Open Elective -I : Basket

SN	Sem	Type	BoS/ Deptt	Sub. Code	Subject
1	3	OE1	GE	23OE1301	OE-I : Combinatorics
2	3	OE1	GE	23OE1302	OE-I : Fuzzy Set Theory, Arithmetic And Logic
3	3	OE1	GE	23OE1303	OE-I : Green Chem. & Sustainability
4	3	OE1	GE	23OE1304	OE-I : Hydrogen Fuel
5	3	OE1	GE	23OE1305	OE-I : Electronic Materials And Applications
6	3	OE1	GE	23OE1306	OE-I : Laser Technology And Applications
7	3	OE1	MGT	23OE1307	OE-I : Finance And Cost Management
8	3	OE1	MGT	23OE1308	OE-I : Operation Research Techniques
9	3	OE1	MGT	23OE1309	OE-I : Project Evaluation & Management
10	3	OE1	MGT	23OE1310	OE-I : Total Quality Management
11	3	OE1	MGT	23OE1311	OE-I : Value Engineering
12	3	OE1	MGT	23OE1312	OE-I : Maintenance Management
13	3	OE1	MGT	23OE1313	OE-I : Industrial Safety
14	3	OE1	MGT	23OE1314	OE-I : Industry 4.0
15	3	OE1	MGT	23OE1315	OE-I : Operation Management
16	3	OE1	MGT	23OE1316	OE-I : Material Management
17	3	OE1	MGT	23OE1317	OE-I : Hospitality Management
18	3	OE1	MGT	23OE1318	OE-I : Human Resource Management & Organizational Behaviour
19	3	OE1	MGT	23OE1319	OE-I : Agri-Business Management
20	3	OE1	MGT	23OE1320	OE-I : Rural Marketing
21	3	OE1	MGT	23OE1321	OE-I : Marketing Management
22	3	OE1	MGT	23OE1322	OE-I : Health Care Management

Link for Open Electives syllabus: <https://ycce.edu/syllabus/>

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

B.Tech in V.L.S.I.

SoE No.
23VLSI-101

III SEMESTER
Mandatory Learning Course (MLC)
MLC2123 : YCAP3

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	

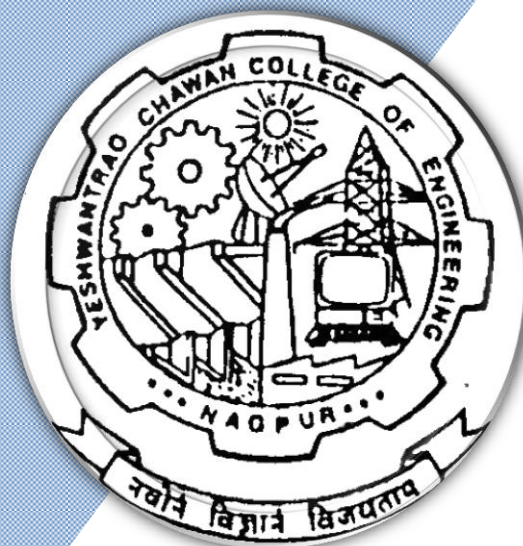
Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

(Accredited 'A++' Grade by NAAC with a score of 3.6)

Hingna Road, Wanadongri, Nagpur - 441 110



Bachelor of Technology SoE & Syllabus 2023 4th Semester

(Department of Electronics Engineering)

B. Tech in VLSI



Nagar Yuwak Shikshan Sanstha's
Yeshwantrao Chavan College of Engineering
 (An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)
B.TECH SCHEME OF EXAMINATION 2023
 (Scheme of Examination w.e.f. 2023-24 onward)
 (Department of Electronics Engineering)
B. Tech Electronics Engineering(VLSI Design and Technology)

SoE No.
23VLSI-101

SN	Sem	Type	BoS/ Deptt	Sub. Code	Subject	T/P	Contact Hours				Credits	% Weightage			ESE Duration Hours
							L	T	P	Hrs		MSEs*	TA**	ESE	
FOURTH SEMESTER															
1	4	BS	GE	23GE1404	Probability Theory and Sampling Theory	T	3	0	0	3	3	30	20	50	3
2	4	HSSM-2	GE	23GE1401	Entrepreneurship Development	T	2	0	0	2	2	30	20	50	3
3	4	AEC-2	GE	23GE1405 23GE1406	Marathi Language / Hindi Language	T	2	0	0	2	2	30	20	50	3
4	4	VEC-1	CV	23CV1411	Environmental Sustainability, Pollution and Management	T	2	0	0	2	2	30	20	50	3
5	4	PC	EE	23VLS1401	Microcontrollers and Computer Architecture	T	3	0	0	3	3	30	20	50	3
6	4	PC	EE	23VLS1402	Lab : Microcontrollers and Computer Architecture	P	0	0	2	2	1		60	40	
7	4	PC	EE	23VLS1403	Lab : Workshop Lab	P	0	0	2	2	1		60	40	
8	5	PC	EE	23VLS1404	Control System Engineering	T	3	0	0	3	3	30	20	50	3
9	4	VSEC-3	EE	23VLS1405	Lab : PCB design or CAD	P	0	0	2	4	2		60	40	
10	4	OE-2	OE		Open Elective-II	T	2	0	0	2	2	30	20	50	3
11	4	MDM	EE		MD Minor Course-II	T	2	0	0	2	2	30	20	50	3
TOTAL							19	0	6	27	23				

List of Mandatory Learning Course (MLC)															
1	4	HS	T&P	MLC2124	YCAP4 : YCCE Communication Aptitude Preparation	A	3	0	0	3	0				

Open Elective - II

SN	Sem	Type	BoS/ Deptt	Sub. Code	Subject
1	4	OE2	GE	23OE2401	OE-II : Combinatorics
2	4	OE2	GE	23OE2402	OE-II : Fuzzy Set Theory, Arithmetic And Logic
3	4	OE2	GE	23OE2403	OE-II : Green Chem. & Sustainability
4	4	OE2	GE	23OE2404	OE-II : Hydrogen Fuel
5	4	OE2	GE	23OE2405	OE-II : Electronic Materials And Applications
6	4	OE2	GE	23OE2406	OE-II : Laser Technology And Applications
7	4	OE2	MGT	23OE2407	OE-II : Finance And Cost Management
8	4	OE2	MGT	23OE2408	OE-II : Operation Research Techniques
9	4	OE2	MGT	23OE2409	OE-II : Project Evaluation & Management
10	4	OE2	MGT	23OE2410	OE-II : Total Quality Management
11	4	OE2	MGT	23OE2411	OE-II : Value Engineering
12	4	OE2	MGT	23OE2412	OE-II : Maintenance Management
13	4	OE2	MGT	23OE2413	OE-II : Industrial Safety
14	4	OE2	MGT	23OE2414	OE-II : Industry 4.0
15	4	OE2	MGT	23OE2415	OE-II : Operation Management
16	4	OE2	MGT	23OE2416	OE-II : Material Management
17	4	OE2	MGT	23OE2417	OE-II : Hospitality Management
18	4	OE2	MGT	23OE2418	OE-II : Human Resource Management & Organizational Behaviour
19	4	OE2	MGT	23OE2419	OE-II : Agri-Business Management
20	4	OE2	MGT	23OE2420	OE-II : Rural Marketing
21	4	OE2	MGT	23OE2421	OE-II : Marketing Management
22	4	OE2	MGT	23OE2422	OE-II : Health Care Management
23	4	OE2	MGT	23OE2423	OE-II : Designated approved online NPTEL/KKSU Course
24	4	OE2	MGT	23OE2424	OE-II : Indian Archeology
25	4	OE2	MGT	23OE2425	OE-II : Social & Positive Psychology
26	4	OE2	MGT	23OE2426	OE-II : Seismology & Earthquake

		July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Date of Release	Version	



Yeshwantrao Chavan College of Engineering

Nagar Yuwak Shikshan Sanstha's
(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

B.Tech in V.L.S.I.

SoE No.
23VLSI-101

IV SEMESTER

23GE1404 : Probability Theory and Sampling Theory

Course Outcomes:

Upon successful completion of the course the students will be able to

1. Identify an appropriate probability distribution for a given discrete or continuous random variable and compute probabilities.
2. Use probability distributions to solve a given problem
3. Apply concepts of sampling theory to find probabilities and estimate parameters of various problems.
4. Test the hypothesis and estimate confidence intervals at different levels.

Unit I:

8 Hrs.

Random Variables and Probability Distributions: Conditional probability, Baye's theorem. Discrete and Continuous random variables, Probability function and Distribution function, Joint distributions. Independent Random variables, Conditional Distribution.

Unit II:

7 Hrs.

Mathematical Expectation: Mathematical Expectation, Variance and Standard Deviation, Moments, Moment generating function, Skewness and Kurtosis.

Unit III:

7 Hrs.

Special Probability Distributions: Binomial, Geometric, Poisson, Exponential, Normal, Central Limit theorem.

Unit IV:

8 Hrs.

Sampling Theory: Unbiased and efficient estimates, Point estimates and interval estimates. Confidence interval for means, Confidence interval for proportions, Confidence interval for differences and sums of mean and proportions.

Unit V:

7 Hrs.

Estimation: Unbiased and efficient estimates. Point estimates and interval estimates. Confidence interval for means, Confidence interval for proportions, Confidence interval for differences and sums of mean and proportions.

Unit VI:

8 Hrs.

Hypothesis Testing: Definition of hypothesis, Testing of hypothesis for large samples using normal distributions. Testing of hypothesis for small distributions (student's t-test, F-test). Goodness of fit test (Chi-square distribution).

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

B.Tech in V.L.S.I.

SoE No.
23VLSI-101

	Total Lecture	45 Hours
--	----------------------	-----------------

Textbooks:

1	M. R. Spiegel, The theory and problems of probability and Statistics, 3 rd edition, Schaum series. (McGraw Hill)
2	Michael J. Evans and Jeffrey S. Rosenthal, Probability and Statistics, 2 nd edition, W. H. Freeman publisher, 2009

Reference Books:

1	S. C. Gupta and V.K. Kapoor, Fundamentals of Mathematical statistics, 10th Edition, Sultan chand and son, 2001.
2	G Balaji, Probability and Statistics, 15 th edition, G Balaji publisher, 2017

YCCE e- library book links [ACCESSIBLE FROM COLLEGE CAMPUS]

1	http://103.152.199.179/YCCE/Supported%20file/Supported%20file/e-copies%20of%20books/Applied%20Sciences%20&%20Humanities/Mathematics%20and%20Humanities/
---	---

MOOCs Links and additional reading, learning, video material

1	https://nptel.ac.in/courses/111106051
2	https://archive.nptel.ac.in/courses/111/104/111104137/
3	https://archive.nptel.ac.in/courses/111/106/111106135/

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

B.Tech in V.L.S.I.

SoE No.
23VLSI-101

IV SEMESTER

23GE1401 : Entrepreneurship Development

Course Outcomes:

Upon successful completion of the course the students will be able to

1. Appreciate role of entrepreneurs in society and develop entrepreneurial abilities by providing information about skill sets.
2. Develop an understanding of how and what form of business organization to choose for start up.
3. Stimulate to innovate, develop prototypes or ideas by applying theory into practice.
4. Identify the Support rendered by various Government Agencies.

Unit I:

7 Hrs.

Entrepreneur & Entrepreneurship: Meaning of Entrepreneur, Evolution of the concept – Theories and Models, Types of Entrepreneur, Stages in entrepreneurial process- Idea Generation, Screening, Selection and Managing Resources.

Unit II:

8 Hrs.

Legal Compliances for Incorporating Start up: Fundamentals of choosing the Business Organization form for startup, Incorporation of Partnership, LL.P & Co – operative, Incorporation of One Person Company, Pvt. Ltd., Pub. Ltd. and not for profit company, Financing the legal Venture and Legal Compliances.

Unit III:

7 Hrs.

Entrepreneurship and IP Strategy: Intellectual Property : Definition and Concept of Trade Mark, Patent, Copyright, Industrial Design, IP Strategy and Entrepreneurship.

Unit IV:

8 Hrs.

Support to Entrepreneurs: Financing new ventures, Business Incubators – Government Policy for Small Scale Enterprises, Growth Strategies in small industry – Expansion, Diversification, Joint Venture, Merger and Subcontracting.

Total Lecture 30 Hours

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

B.Tech in V.L.S.I.

SoE No.
23VLSI-101

Student activities:

1. Interview at least four entrepreneurs or businessman and identify Traits of successful entrepreneurs.
2. Analyse case studies of any two successful entrepreneurs.
3. Download product development and innovative films from internet.
4. Identify your hobbies and interests and convert them into business idea

Textbooks

1. Khanka. S.S., "Entrepreneurial Development" S.Chand & Co. Ltd., Ram Nagar, New Delhi, 2013.
2. Donald F Kuratko, "Entrepreneurship – Theory, Process and Practice", 9th Edition, Cengage Learning 2014.
3. Corporate Law, 33rd ed. 2016, Taxman New Delhi.
4. Narayanan, V. K., Managing technology and innovation for competitive advantage, first edition, Pearson education, New Delhi, (2006)
5. Idris, K. (2003), Intellectual property: a power tool for economic growth, second edition, WIPO publication no. 888, Switzerland
6. Khanka. S.S., "Entrepreneurial Development" S.Chand & Co. Ltd., Ram Nagar, New Delhi, 2013.
7. Ramaiya's Guide to the Companies Act, 18th ed. 2014, Lexis Nexis New Delhi.

Reference Books

1. Mehta, Monica- The Entrepreneurial Instinct : How everyone has the innate ability to start a successful small business – McGraw – Hill Education, New Delhi 2012, ISBN 978-0-07-179742-9
2. Prasanna Chandra "Protect Preparation, Appraisal, Implementation" Tata McGraw Hill. New Delhi
3. S Anil Kumar "Entrepreneurship Development" New Age International Publishers
4. Nishith Dubey "Entrepreneurship Development" PHI Learning

YCCE e- library book links [ACCESSIBLE FROM COLLEGE CAMPUS]

- 1 <http://link.springer.com/openurl?genre=book&isbn=978-1-4613-6193-0>
- 2 <https://onlinelibrary.wiley.com/doi/book/10.1002/9780470168042>

MOOCs Links and additional reading, learning, video material

- 1 https://onlinecourses.swayam2.ac.in/cec23_mg24/course- entrepreneurship development
- 2 https://onlinecourses.nptel.ac.in/noc23_mg74/announcements?force=true-entrepreneur
- 3 https://onlinecourses.nptel.ac.in/noc23_mg126/announcements?force=true-Business fundamentals for entrepreneurship

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

B.Tech in V.L.S.I.

SoE No.
23VLSI-101

IV SEMESTER 23GE1405 : Marathi Language

Course Objectives		
<ol style="list-style-type: none"> मराठी भाषेच्या समृद्धीची जाणीव करून देणे. विद्यार्थ्यांमध्ये भाषा कौशल्याचा विकास करणे आणि त्यातून रोजगाराच्या संधीचा शोध घेणे. 		
Course Outcomes		
<ol style="list-style-type: none"> भाषेचा जीवन व्यवहारात योग्य पद्धतीने वापर करण्याचा प्रयत्न करणे. संत साहित्याच्या शिकवणुकीमुळे मानवता आणि मानवी व्यवहाराची सांगड घालणे, नैतिक मूल्ये रुजविणे. विद्यार्थ्यांना रोजगाराभिमुख बनविणे. 		
Unit:1	गद्य विभाग	8 Hours
१. भारतीय लोकशाहीचे भवितव्य काय?	- डॉ. बाबासाहेब आंबेडकर	
२. काळी आई	- व्यंकटेश माडगूळकर	
३. संत तुकारामांचे अभंग	- निर्मलकुमार फडकुले	
४. माझी शाळा	- प्रकाश खरात	
५. समतेचे वारकरी संत गाडगेबाबा आणि राष्ट्रसंत तुकडोजी महाराज	- अशोक राणा	
६. लोककल्याणकारी राजा :	- शरयू तायवाडे	
Unit:2	पद्य विभाग	8 Hours
१. ज्ञानेश्वरांचे अभंग	- संत ज्ञानेश्वर	
२. वनसुधा	- वामन पंडित	
३. नवा शिपाई	- केशवसुत	
४. मेंढरं	- विठ्ठल वाघ	
५. पोरी	- अनुराधा पाटील	
६. गाव	- हेमंतकुमार कांबळे	

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's
Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

B.Tech in V.L.S.I.

SoE No.
23VLSI-101

Unit:3	व्यावहारिक मराठी	7 Hours
१. म्हणी		
२. मुलाखतलेखन	- डॉ. वैशाली धनविजय	
३. वाक्प्रचार		
४. जाहिरातलेखन	- डॉ. अजय देशपांडे	
Unit:4	रोजगाराभिमुख मराठी व्यावहारिक कौशल्ये	7 Hours
१. प्रत्यक्ष मुलाखत कौशल्य		
२. वाचन कौशल्य - (अ) बातमी वाचन (ब) कथा वाचन		
३. ऑनलाईन कौशल्य - (अ) ग्राहक सेवा केंद्राशी संवाद, (ब) ऑनलाईन अर्ज करणे		

Reference Books

- पाठ्यपुस्तक : शब्दसाधना - भाग १
- रोजगाराभिमुख मराठी व्यावहारिक कौशल्ये

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

B.Tech in V.L.S.I.

SoE No.
23VLSI-101

IV SEMESTER 23GE1406 : Hindi Language

Course Objectives

- विद्यार्थियों में देशभक्तिपरक एवं पारिवारिक मूल्यों का विकास |
- विद्यार्थियों पर्यावरण-संरक्षण के प्रति सजग करना |
- एकांकी, कहानी, निबंध आदि विधाओं के मध्य का अंतर अवगत कराना |
- हिंदी के प्रयोजनमूलक स्वरूप से परिचित कराना |
- विद्यार्थियों को आधुनिक प्रौद्योगिकी (तकनीक) का प्रयोग करने में सक्षम बनाना |.

Course Outcomes

- पौराणिक अथवा ऐतिहासिक घटनाओं को तार्किक आधार पर स्वीकार करेंगे | अपने परिवेश के उचित और अनुचित व्यवहारों के प्रति आकलन शक्ति बढ़ेगी |
- एकांकी, कहानी, निबंध आदि विधाओं के मध्य का अंतर बताने में सक्षम होंगे |
- कविता का रसास्वादन करने में समर्थ होंगे |
- 'अनुवाद' के स्वरूप एवं प्रक्रिया से अवगत होंगे |
- 'मार्गिक नक्शे' का दैनिक जीवन में उपयोग करने में सक्षम होंगे |

Unit:1	गद्य विभाग	8 Hours
१. भाईसाहब (कहानी)	- प्रेमचंद	
२. स्मृति (निबंध)	- श्रीराम शर्मा	
३. गिल्लू (रेखाचित्र)	- महादेवी वर्मा	
४. अभाव (कहानी)	- विष्णु प्रभाकर	
५. महाभारत की साँझ (एकांकी)	- भारतभूषण	
६. उखड़े खंबे (व्यंग्य)	- हरिशंकर परसाई	

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

B.Tech in V.L.S.I.

SoE No.
23VLSI-101

Unit:2	पद्य विभाग	8 Hours
१. कबीर के दोहे	- कबीरदास	
२. ले चल यहाँ भुलावा देकर	- जयशंकर प्रसाद	
३. स्नेह-निर्झर बह गया	- हैसूर्यकांत त्रिपाठी "निराला"	
४. प्रथम रश्मि	- सुमित्रानंदन पंत	
५. जीवन का झरना	- आरसीप्रसाद सिंह	
६. कविता के साथ	- दामोदर खड़से	
Unit:3	अन्य पाठ्य सामग्री	7 Hours
१. मुहावरे और लोकोक्तियाँ: पाठ्यपुस्तक में मुहावरे और लोकोक्तियाँ का अर्थ एवं वाक्य प्रयोग		
२. विज्ञापन कला : अर्थ, परिभाषा, प्रकार, शीर्षक का महत्त्व, विज्ञापन के प्रयोजन, सत्य, लक्ष्य, विज्ञापन की भाषा, अच्छे विज्ञापन के गुण इत्यादि ।		
Unit:4	कौशल्य आधारित घटक	7 Hours
१. वाचन कौशल्य (समाचार-वाचन, कहानी-वाचन)		
२. सोशल मीडिया के शिष्टाचार		
३. ऑनलाइन आवेदन, ग्राहक-सेवा केंद्र से संवाद		

Reference Books

३. पाठ्यपुस्तक : "पलाश"

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Yeshwantrao Chavan College of Engineering

Nagar Yuwak Shikshan Sanstha's
(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

B.Tech in V.L.S.I.

SoE No.
23VLSI-101

III/IV SEMESTER 23CV1311/23CV1411

Environmental Sustainability, Pollution and Management

Course Outcomes :

Upon successful completion of the course, the students will be able to

The student will be able to

1. Gain insights into the efforts to safeguard the Earth's environment and resources.
2. Develop a critical understanding of the contemporary environmental issues of concern
3. Have an overview of pollution, climate change and national and global efforts to address adaptation and mitigation to changing environment through environmental management.
4. Learn about the major international treaties and our country's stand on and responses to the major international agreements.

Unit:1	Environment and Sustainable Development	8 Hours
The man-environment interaction; Overview of natural resources: renewable, and non-renewable energy resources; Introduction to sustainable development: Sustainable Development Goals (SDGs)- targets and indicators, challenges and strategies for SDGs; Environmental issues: Global change, Climate Change and Mitigation.		
Unit:2	Environmental Pollution and Health	7 Hours
Understanding pollution: Production processes and generation of wastes, Air pollution, Water pollution, Soil pollution and solid waste, Noise pollution, Thermal and Radioactive pollution. Impact on biotic and abiotic things.		
Unit:3	Environmental Management	8 Hours
Environmental management system: ISO 14001, Concept of Circular Economy, Life cycle analysis; Cost-benefit analysis, Environmental audit and impact assessment; Waste Management and sustainability; Ecolabeling /Eco mark scheme		
Unit:4	Environmental Treaties and Legislation	7 Hours
Introduction to environmental laws and regulation, An overview of instruments of international cooperation, Major International Environmental Agreements, Major Indian Environmental Legislations, Major International organizations, and initiatives		
Total Lecture		30 Hours

Text books

1	Chiras, D. D and Reganold, J. P. (2010). Natural Resource Conservation: Management for a Sustainable Future. 10th edition, Upper Saddle River, N. J. Benjamin/Cummins/Pearson
2	Rajagopalan, R. (2011). Environmental Studies: From Crisis to Cure. India: Oxford University Press
3	Krishnamurthy, K.V. (2003) Textbook of Biodiversity, Science Publishers, Plymouth, UK
4	Jackson, A. R., & Jackson, J. M. (2000). Environmental Science: The Natural Environment and Human Impact. Pearson Education
5	Pittock, Barrie (2009) Climate Change: The Science, Impacts and Solutions. 2nd Edition. Routledge.
6	Theodore, M. K. and Theodore, Louis (2021) Introduction to Environmental Management, 2nd Edition. CRC Press
7	Kanchi Kohli and Manju Menon (2021) Development of Environment Laws in India, Cambridge University Press

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

B.Tech in V.L.S.I.

SoE No.
23VLSI-101

Reference Books

1	Headrick, Daniel R. (2020) Humans versus Nature- A Global Environmental History, Oxford University Press
2	Gilbert M. Masters and W. P. (2008). An Introduction to Environmental Engineering and Science, Ela Publisher (Pearson)
3	William P. Cunningham and Mary A. (2015). Cunningham Environmental Science: A global concern, Publisher (Mc-Graw Hill, USA)
4	Varghese, Anita, Oommen, Meera Anna, Paul, Mridula Mary, Nath, Snehlata (Editors) (2022) Conservation through Sustainable Use: Lessons from India. Routledge.
5	Central Pollution Control Board Web page for various pollution standards. https://cpcb.nic.in/standards
6	Barnett, J. & S. O'Neill (2010). Maladaptation. Global Environmental Change—Human and Policy Dimensions 20: 211–213
7	Richard A. Marcantonio, Marc Lane (2022). Environmental Management: Concepts and Practical Skills. Cambridge University Press
8	Ministry of Environment, Forest and Climate Change (2019) A Handbook on International Environment Conventions & Programmes. https://moef.gov.in/wp-content/uploads/2020/02/convention-V-16-CURVE-web.pdf

YCCE e- library book links [ACCESSIBLE FROM COLLEGE CAMPUS]

1	
---	--

MOOCs Links and additional reading, learning, video material

1	
---	--

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

B.Tech in V.L.S.I.

SoE No.
23VLSI-101

IV SEMESTER

23VLS1401 : Microcontrollers and Computer Architecture

Course Outcomes:

Upon successful completion of the course the students will be able to

1. Understand & Learn concept of Architecture of 8085 μ P & 8051 Microcontroller
2. Write Program for an assigned task.
3. Apply different address decoding techniques while interfacing Memory to Microprocessor
4. Analyze and Design interfacing of Peripheral devices to Microprocessor & Microcontroller

Unit:1	Introduction to Microprocessor Micro Computer organization with I/O devices and Memory , Memory organization (RAM, ROM Memory) , Microprocessor 8085 architecture , Flag Register , Pins diagram of 8085, Demultiplexing of Address & Data Bus, Generation of various control signals for I/O & Memory	8 Hours
Unit:2	Instruction set & Programming of 8085 Addressing modes of 8085, Basic Instruction set :Data Transfer operations, Arithmetic operations, Logic Operations, Branch operation, Subroutines, Interrupt Control, Programs based on instructions	7 Hours
Unit:3	Memory & I/O Device Interfacing with 8085 Memory Interfacing - ROM, RAM With 8085, 8255 PPI, ADC,DAC, 8253 PIT	8 Hours
Unit:4	Introduction to Microcontroller 8051 Architecture, Memory Organization, Internal RAM, Flag Register, Register Banks, SFRs , Functional pin description .	7 Hours
Unit:5	Instruction set & Programming of 8051 Addressing modes, Basic Instruction set, Loop, Jump and Call instructions, Bit manipulation, , Delay Programs. Programs based on instructions.	8 Hours
Unit :6	I/O Device Interfacing with 8051 8051 I/O programming, I/O Interfacing such as LED, switches, 7segment display, keyboard matrix programming	7 Hours
Total Lecture Hours		45 Hours

			July,2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

B.Tech in V.L.S.I.

SoE No.
23VLSI-101

Text books

1	Ramesh Gaonkar, Microprocessor Architecture ,Programming & Application with the 8085, Publication : 1 Dec 2000, Pearson Publication, V'th Edition
2	The 8051 Microcontroller and Embedded systems , Muhammad Ali Mazidi , J.G. Mazidi, 2nd edition Pearson Education, Prentice Hall of India.
3	8051 Microcontrollers programming and practice By Mike Predcko.
4	The 8051 Microcontroller Architecture, programming and Applications By Kenneth Ayala, Penram India publication.
5	Advanced Microprocessors and Peripherals , A. K. Ray, K. M. Bhurchandi, Second edition, Tata McGraw Hill, 2000.

Reference Books

1	D. V. Hall , Microprocessors & interfacing ,Publication : Tata Mc-Graw Hill ,2005
2	Intel or Atmel MCS 51 Family Microcontrollers Data Sheets.
3	Computer System Architecture, Mano M M , Prentice Hall India

YCCE e- library book links [ACCESSIBLE FROM COLLEGE CAMPUS]

1	http://103.152.199.179/YCCE/yccelibrary.html
2	

MOOCs Links and additional reading, learning, video material

1	NptelVideo : https://www.youtube.com/watch?v=0t4LROuEVnw&list=PLwdnzlV3ogoXgNjr_oe5cWQIbf72ZY4Zf
2	https://www.youtube.com/watch?v=oRPluYsxF28&list=PLuv3GM6-gsE01L9yDO0e5UhQapkCPGnY3&index=7
3	https://www.electronicwings.com/
4	https://www.youtube.com/watch?v=-YYpIdk4_W8&list=PLuv3GM6-gsE01L9yDO0e5UhQapkCPGnY3&index=25
5	https://nptel.ac.in/courses/106102157

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

B.Tech in V.L.S.I.

SoE No.
23VLSI-101

IV SEMESTER

23VLS1402 : Lab. Microcontrollers and Computer Architecture

Course Outcomes:

Upon successful completion of the course the students will be able to

1. Understand & Learn concept of Architecture of 8085 μ P & 8051 Microcontroller
2. Write Program for an assigned task.
3. Apply different address decoding techniques while interfacing Memory to Microprocessor
4. Analyze and Design interfacing of Peripheral devices to Microprocessor & Microcontroller

Sr. No.	Experiments based on
1	Arithmetic & Logical Operation 8085
2	Data block transfer 8085
3	Find the maximum data byte in a block 8085
4	Count Positive data Bytes 8085 from a block.
5	Interfacing & Programming Based on 8255 PPI
6	Interfacing & Programming Based on 8253 PIT
7	Add data bytes in an internal RAM (8051)
8	Find the maximum data byte in a block (8051)
9	Data block transfer (8051)
10	Count negative data bytes from a block.
11	Program to blink LED connected to pin P0.4 of 8051
12	Program to turn on LED if Push button is Pressed. LED is connected to P2.3 and Push Button is connected to P2.4 of 8051
13	Common Anode Seven Segment Display is connected with P2 of 8051 . Write program to display 0 to 9 at an interval of 1 sec

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

B.Tech in V.L.S.I.

SoE No.
23VLSI-101

IV SEMESTER 23VLS1403 : Lab : Workshop Lab

Course Outcomes:

Upon successful completion of the course the students will be able to

- **Understand** and identify Different Electronics Components.
- **Apply** the basic knowledge of Electronics Components to select the mini project.
- **Demonstrate** their practical Knowledge to do Artwork, printing, Etching & drilling of PCB for mini project.
- **Prepare** the mini project report and three minute video.

Sr. No.	Experiments based on
1	Identification of Various electronic components used in electronics workshop.
2	Identification of various equipment used in electronics workshop.
3	Testing of various electronics components.
4	Soldering and De-Soldering Practice.
5	PCB Design using EDA Tools (Orcad Layout Plus /Allegro/ Multisim Ultiboard /EasyEDA / Express PCB)
6	Etching and fabrication
7	Mini Project (Arduino / Node MCU / Raspberry Pi)
8	Report Writing

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

B.Tech in V.L.S.I.

SoE No.
23VLSI-101

IV SEMESTER

23VLS1404 : Control System Engineering

Course Outcomes:

1. Understand concepts related to linear control system
2. Apply the concepts of control system to obtain the system Transfer function
3. Analyze time domain analysis of given control system
4. Apply frequency domain analysis method to various linear control systems

Unit:1	8 Hours
Introduction to Control Systems: History of control system, Basic Components of Control System. Open loop control and close loop control with examples. Classification of control systems, Transfer function, block Diagram and signal flow graph:-Transfer function and gain. Order of a system. Block diagram algebra & reduction techniques Signal flow graph, its constructions and Mason's gain formula.	
Unit:2	7 Hours
Mathematical modeling of physical system: Mathematical modelling of physical system such as –electrical, mechanical, electro-mechanical, thermal, hydraulic, pneumatic etc., Analogous systems, Characteristics of Feedback Control Systems: Effect of negative feedback compared to open loop system such as –sensitivity to parameter variation. sensitivity to parameter variation such gain and forward path, Speed of time response, bandwidth, and disturbance rejection., Linearizing effect, Effect of positive feedback.	
Unit:3	8 Hours
Time Domain Analysis of Control Systems: Concept of transient response, Steady state response, time response, standard test signals, Time response of first order systems, Transfer function of second order system, Time response of second order system, Time response specifications of second order system, steady state error (ess) analysis, static error constants and system type, dominant poles. Relation between roots of characteristic equation, damping ratio and transient response.	
Unit:4	7 Hours
Stability of Linear Control Systems: Concept of stability, stable, unstable and marginally stable system, Absolutely stable and conditionally stable system, Necessary conditions for stability, method to determine stability, Routh-Hurwitz stability criterion with special cases, relative stability analysis, Routh-Hurwitz stability criterion with special cases, relative stability analysis. State Variable Analysis.	

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

SoE No.
23VLSI-101

B.Tech in V.L.S.I.

Unit:5		8 Hours
Root Locus Technique: Definition, magnitude and angle criteria, properties of root locus, construction rules, for root locus plot of negative feedback systems, determining the gain from root locus plot, effect of addition of poles and zeros of $G(s)$ $H(s)$.		
Unit :6		7 Hours
Frequency domain analysis of control systems: Concept of frequency response and sinusoidal transfer function, resonant frequency, resonant peak, cut off frequency, bandwidth, and correlation between time and frequency response, polar plot, Bode plot, all pass and minimum, log magnitude verses phase plot. Stability in Frequency domain: Nyquist stability criteria, concept of gain margin and phase margin and its computation using polar plot and log magnitude verses phase plot. Lag, lead and lag-lead compensation		
Total Lecture Hours		45 Hours

Text books	
1	I.J. Nagrath. M. Gopal, Control system Engineering Sixth Edition, Prentice Hall
Reference Books	
1	Katsuhiko Ogata, Modern Control system, Fifth Edition, Prentice Hall.
2	Joseph J. DiStefano, Feedback and Control Systems, 2nd Edition. McGraw-Hill Education
YCCE e- library book links [ACCESSIBLE FROM COLLEGE CAMPUS]	
1	http://103.152.199.179/YCCE/yccelibrary.html
MOOCs Links and additional reading, learning, video material	
1	https://onlinecourses.nptel.ac.in/noc22_ee31/preview

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Yeshwantrao Chavan College of Engineering

Nagar Yuwak Shikshan Sanstha's
(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

B.Tech in V.L.S.I.

SoE No.
23VLSI-101

IV SEMESTER **23VLSI405 : Lab : PCB design or CAD**

Course Outcomes:

Upon successful completion of the course the students will be able to

1. Understand of fundamental concepts related to PCB design
2. Gain proficiency in using industry-standard EDA tools for PCB design
3. apply design rules and best practices in PCB layout, component placement
4. Analyse and optimize signal integrity in PCB designs, soldering practices
5. Prototype development, and practical testing to ensure that the designed circuits

Sr. No.	Experiments based on
1	Introduction to PCB Design Process
2	Introduction to EDA tools
3	PCB materials
4	PCB layout methods
5	Etching Process
6	Soldering Process
7	Fabrication and Testing
8	Mini Project

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's
Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

B.Tech in V.L.S.I.

SoE No.
23VLSI-101

IV SEMESTER
Multidisciplinary Minor Courses

Track 1
MDMT1VLS101 : Digital VLSI

Courses	Sem	MDMT1VLS101 : Digital VLSI
MDM-I	3	(MDM1VLS101) Introduction to electronic Components
MDM-II	4	(MDM2VLS102) Introduction to Digital Logic
MDM-III	5	(MDM3VLS103) Switching Theory
MDM-IV	6	(MDM4VLS104) Digital System Design
MDM-V	7	(MDM5VLS105) Computer Architecture
MDM-VI	8	(MDM6VLS106) Data acquisition and signal conditioning

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

B.Tech in V.L.S.I.

SoE No.
23VLSI-101

IV SEMESTER Open Elective -II : Basket

SN	Sem	Type	BoS/ Deptt	Sub. Code	Subject
1	4	OE2	GE	23OE2401	OE-II : Combinatorics
2	4	OE2	GE	23OE2402	OE-II : Fuzzy Set Theory, Arithmetic And Logic
3	4	OE2	GE	23OE2403	OE-II : Green Chem. & Sustainability
4	4	OE2	GE	23OE2404	OE-II : Hydrogen Fuel
5	4	OE2	GE	23OE2405	OE-II : Electronic Materials And Applications
6	4	OE2	GE	23OE2406	OE-II : Laser Technology And Applications
7	4	OE2	MGT	23OE2407	OE-II : Finance And Cost Management
8	4	OE2	MGT	23OE2408	OE-II : Operation Research Techniques
9	4	OE2	MGT	23OE2409	OE-II : Project Evaluation & Management
10	4	OE2	MGT	23OE2410	OE-II : Total Quality Management
11	4	OE2	MGT	23OE2411	OE-II : Value Engineering
12	4	OE2	MGT	23OE2412	OE-II : Maintenance Management
13	4	OE2	MGT	23OE2413	OE-II : Industrial Safety
14	4	OE2	MGT	23OE2414	OE-II : Industry 4.0
15	4	OE2	MGT	23OE2415	OE-II : Operation Management
16	4	OE2	MGT	23OE2416	OE-II : Material Management
17	4	OE2	MGT	23OE2417	OE-II : Hospitality Management
18	4	OE2	MGT	23OE2418	OE-II : Human Resource Management & Organizational Behaviour
19	4	OE2	MGT	23OE2419	OE-II : Agri-Business Management
20	4	OE2	MGT	23OE2420	OE-II : Rural Marketing
21	4	OE2	MGT	23OE2421	OE-II : Marketing Management
22	4	OE2	MGT	23OE2422	OE-II : Health Care Management

Link for Open Electives syllabus: <https://ycce.edu/syllabus/>

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

B.Tech in V.L.S.I.

SoE No.
23VLSI-101

IV SEMESTER
Mandatory Learning Course (MLC)
MLC2124 : YCAP4

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	

Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

(Accredited 'A++' Grade by NAAC with a score of 3.6)

Hingna Road, Wanadongri, Nagpur - 441 110



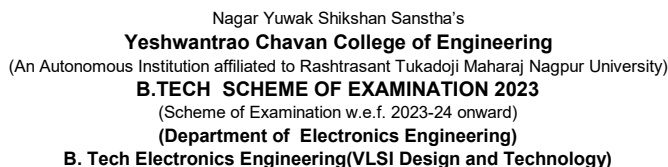
Bachelor of Technology

SoE & Syllabus 2023

5th Semester

(Department of Electronics Engineering)

B. Tech in VLSI



SN	Sem	Type	BoS/Deptt	Sub. Code	Subject	T/P	Contact Hours				Credits	% Weightage			ESE
							L	T	P	Hrs		MSEs*	TA**	ESE	Duration Hours
FIFTH SEMESTER															
1	5	PC	EE	23VLS1501	Embedded System	T	3	0	0	3	3	30	20	50	3
2	5	PC	EE	23VLS1502	Lab : Embedded System	P	0	0	2	2	1		60	40	
3	5	PC	EE	23VLS1503	CMOS VLSI Design	T	3	0	0	3	3	30	20	50	3
4	5	PC	EE	23VLS1504	Lab : CMOS VLSI Design	P	0	0	2	2	1		60	40	
5	5	PC	EE	23VLS1505	Digital System Modelling	T	3	0	0	3	3	30	20	50	3
6	5	PC	EE	23VLS1506	Lab : Digital System Modelling	P	0	0	2	2	1		60	40	
7	6	PC	EE	23VLS1507	Object Oriented Programming	T	2	0	0	2	2	30	20	50	3
8	6	PC	EE	23VLS1508	Lab : Object Oriented Programming	P	0	0	2	2	1		60	40	
9	5	PE	EE		Professional Elective-I	T	3	0	0	3	3	30	20	50	3
10	5	OE-3	OE		Open Elective-III	T	3	0	0	3	3	30	20	50	3
11	5	MDM	EE		MD Minor Course-III	T	3	0	0	3	3	30	20	50	3
12	5	STR	EE	23VLS1509	Internship and Indsutrial Visit	P	0	0	2	2	1		60	40	
TOTAL							20	0	10	30	25				

1	5	HS	T&P	MLC2125	YC&P5 : YCCE Communication Aptitude Preparation	A	3	0	0	3	0						
---	---	----	-----	---------	--	----------	---	---	---	---	----------	--	--	--	--	--	--

Professional Electives I					
1	5	PE-I	EE	23VLS1521	PE-I : CAD for VLSI
2	5	PE-I	EE	23VLS1522	PE-I : Algorithm and Data Structure
3	5	PE-I	EE	23VLS1523	PE-I : Semiconductor Device Modeling

SN	Sem	Type	BoS/Dept	Sub. Code	Subject	FACULTY
1	5	OE3	CSE	23OE3501	OE-III : Social Reformers in Modern Maharashtra	ARTS
2	5	OE3	CSE	23OE3502	OE-III : Independent India 1948-2010	ARTS
3	5	OE3	CT	23OE3503	OE-III : Introduction To Cognitive Psychology	ARTS
4	5	OE3	CT	23OE3504	OE-III : Introduction To Engineering Psychology	ARTS
5	5	OE3	CT	23OE3505	OE-III : Introduction To Behavioural Psychology	ARTS
6	5	OE3	CT	23OE3506	OE-III : Introduction To Emotional Psychology	ARTS
7	5	OE3	EL	23OE3507	OE-III : Elements of Public Administration	ARTS
8	5	OE3	ETC	23OE3508	OE-III : Ancient Indian History	ARTS
9	5	OE3	IT	23OE3509	OE-III : Consciousness Studies	ARTS
10	5	OE3	IT	23OE3510	OE-III : Psychology for Professionals	ARTS
11	5	OE3	IT	23OE3511	OE-III : Introduction to Sociology and Human Behavior	ARTS
12	5	OE3	GE	23OE3512	OE-III : Economics of Money and Banking	ARTS
13	5	OE3	GE	23OE3513	OE-III : Economics of Capital Market	ARTS
14	5	OE3	GE	23OE3514	OE-III : Digital Humanities	ARTS
15	5	OE3	GE	23OE3515	OE-III : Introduction to Political Science	ARTS
16	5	OE3	CT	23OE3516	OE-III : Bhagwat Geeta - An Engineer's Interpretation	ARTS - IKS
17	5	OE3	CT	23OE3517	OE-III : Artha shastra by Kautiliya	ARTS - IKS
18	5	OE3	CSD	23OE3518	OE-III : Glimpses of Ancient science and Technology	ARTS - IKS
19	5	OE3	CV	23OE3519	OE-III : Indian taxation system	COMMERCE
20	5	OE3	CV	23OE3520	OE-III : Elements of share trading	COMMERCE
21	5	OE3	EE	23OE3521	OE-III : Introduction to Fintech	COMMERCE
22	5	OE3	EE	23OE3522	OE-III : Financial Analytics	COMMERCE
23	5	OE3	ETC	23OE3523	OE-III : Fundamentals of Investments	COMMERCE
24	5	OE3	EE	23OE3524	OE-III : Lifestyle Diseases	HEALTHCARE & MEDICINE
25	5	OE3	EE	23OE3525	OE-III : Holistic Nutrition	HOME SCIENCE
26	5	OE3	EL	23OE3526	OE-III : Community Organization & Development	HOME SCIENCE
27	5	OE3	CSE	23OE3527	OE-III : Human Rights & International Laws	LAW
28	5	OE3	CSE	23OE3528	OE-III : Cyber Crime Administration	LAW
29	5	OE3	MATHS	23OE3529	OE-III : Finite Differences & Numerical Methods	SCIENCE
30	5	OE3	MATHS	23OE3530	OE-III : Business Statistics	SCIENCE
31	5	OE3	PHY	23OE3531	OE-III : Crystalline Solids: Properties and Applications.	SCIENCE
32	5	OE3	PHY	23OE3532	OE-III : Nanotechnology: Fundamental to Applications	SCIENCE
33	5	OE3	CHE	23OE3533	OE-III : Chemistry in daily life	SCIENCE
34	5	OE3	CHE	23OE3534	OE-III : Battery Systems and Management	SCIENCE
35	5	OE3	NPTEL	23OE3535	OE-III : Designated approved online NPTEL Course	NPTEL

July, 2023

1.00

Applicable for
AY 2023-24 Onwards

Chairperson

Dean (Acad. Matters)

Date of Release

Version



Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

SoE No.
23VLSI-101

B.Tech in V.L.S.I.

V SEMESTER

23VLSI501 : Embedded System

Course Outcomes:

After completion of the course, student will demonstrate the ability to:

CO1: Describe the ARM microprocessor architectures, its features and instructions.

CO2: Write program for specific task.

CO3: Analyze and Interface the peripherals to ARM based microcontroller.




CO4: Develop embedded system application using ARM based microcontroller.

CO5: Write program and Debug using IDE tool like KEIL MDK410.

Unit:1	Introduction to ARM, Advantages of architectural features of ARM Processor, Processor modes, Register organization, Exceptions and its handling, 3/5- stage pipeline ARM organization	7 Hours
Unit:2	ARM and THUMB instruction sets, ARM programmer's model, addressing modes, Instruction set in detail and programming, data processing instruction, data transfer instruction, Control flow instructions, simple assembly language programs.	7 Hours
Unit:3	ARM assembly language programs and C language programs. Code conversion programs.	7 Hours
Unit:4	LPC 2148 architecture block diagrams, pins and signals. GPIO, I / O Interfaces like LED and Switch and their Programs.	7 Hours
Unit:5	Display interfacing with LPC 2148. 7segment display interfacing. LCD interfacing and programs.	7 Hours
Unit :6	LPC 2148 TIMER and PWM Applications. Embedded ARM applications	7 Hours
Total Lecture Hours		42 Hours

Text books

1	ARM System on-chip Architecture, 2nd edition, 2000, Steve Furber, Pearson Education Asia
2	Embedded Linux, Hardware, Software and interfacing, 2002. Craig Hallabaugh, Addison-Wesley Professional
3	ARM System Developer's Guide: Designing and Optimizing, 2005 Sloss Andrew N, Symes Dominic, Wright Chris Morgan Kaufman Publication

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

B.Tech in V.L.S.I.

SoE No.
23VLSI-101

Reference Books

1 Technical references on www.arm.com.

2 Web base resources for RTOS and μ COS.




YCCE e- library book links [ACCESSIBLE FROM COLLEGE CAMPUS]

1 <http://172.16.1.9/LocalGuru/listLectures.php?cid=29086f3420285fdf&bid=927d7542627865a3>

MOOCs Links and additional reading, learning, video material

1 <https://nptel.ac.in/courses/106105159>

2 <https://nptel.ac.in/courses/106105193>

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

SoE No.
23VLSI-101

B.Tech in V.L.S.I.

V SEMESTER

23VLSI502 : Lab. Embedded System

Course Outcomes:

Upon successful completion of the course the students will be able to

1. **Write** program for specific task
2. **Analyze** and Interface the peripherals to ARM based microcontroller
3. **Develop** embedded system application using ARM based microcontroller
4. **Write program** and **Debug** using IDE tool like KEIL MDK410 for ARM

Expt. No.	Name of Experiment / Problem Statement
1	a) Write program to perform addition of two 16 bit nos. and store result in R5 b) Write program to perform subtraction of two 16 bit nos. and store result in R5
2	Write program to add two nos. x and y present in memory at address 4000000H and 40000004H and store in memory 40000008H
3	Write program to add Five 8 bit nos. present in memory from address 40000004H and store result in memory 4000 0030H
4	Write program to multiply data of two array $z_i = x_i * y_i$ <ul style="list-style-type: none"> • x_i and y_i are 32 bit nos • array1 (x_i) stored from address 40000000H • array 2 (y_i) stored from address 40000020H • no. of elements in array $i = 5$ • Store result array3 (z_i) from address 40000040H
5	Compare two strings of 3 ASCII characters, One string starts at 0x40000000 and other at 0x40000010. If both the string match store 11H in memory location 0x40000030 otherwise store 22H in memory location 0x40000030.
6	Draw Interfacing of 1 LED with LPC2148 and write program to blink LED connected to port pin P1.16. Use LPC 2148 ARM Kit to demonstrate.
7	Draw Interfacing of 8 LED with LPC2148 and Write program to blink 8 LEDs alternately connected to port pins P1.23 to P1.16. Use LPC 2148 ARM Kit to demonstrate.
8	Draw Interfacing of 1 LED and 1 switch with LPC2148 and Write program to turn ON LED, if Switch is pressed else LED OFF. LED is connected to port pin P1.16 and switch is connected to input pin P0.10 and SW is grounded by using output pin P0.14. Use LPC 2148 ARM Kit to demonstrate.
9	Draw Interfacing of common cathode 7 segment display with LPC2148 and write program to display 0 to 9 at an interval of 2 sec. 7 segment display is connected to port pins P1.23 to P1.16. Use LPC 2148 ARM Kit to demonstrate.
10	Draw Interfacing of common anode 7 segment display with LPC2148 and write program to display 0 to 5 at an interval of 3 sec. 7 segment display is connected to port pins P1.23 to P1.16. Use LPC 2148 ARM Kit to demonstrate.

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

SoE No.
23VLSI-101

B.Tech in V.L.S.I.

V SEMESTER

23VLSI503 : CMOS VLSI Design

Course Outcomes:

Upon successful completion of the course the students will be able to

1. Describe and interpret the basic concepts of MOS transistors.
2. Construct digital CMOS circuits as per specifications.
3. Analyze inverter design, characteristics and Performance parameters of CMOS Circuits.
4. Design and implement combinational and sequential circuits using different CMOS styles

Unit:1	Introduction of CMOS	8 Hours
Introduction of MOSFETs: CMOS Fabrication Process steps, NMOS Enhancement Transistor, MOS Transistor Operations, PMOS Enhancement Transistor, Regions of Operations, Threshold Voltage, MOS Device Equations.		
Unit:2	Logic Design With CMOS	7 Hours
Logic Design With MOSFETs: Ideal Switches and Boolean Operations, MOSFETs as Switches, Basic Logic Gates in CMOS, Compound Gates in CMOS, Transmission Gate Circuits (TG), Pass Transistor.		
Unit:3	CMOS inverter	7 Hours
MOS inverter Characteristics: Resistive load inverter, Inverters with n type MOSFET load, CMOS inverter, Principle of operation, DC characteristics, Tristate Inverter, Noise Margin, Introduction to Bi-CMOS Inverter.		
Unit:4	Combinational circuit design	8 Hours
Static CMOS, Ratioed Logic circuits, Analysis of CMOS Logic Gates: MOS Device Capacitance, Switching Characteristics, Rise Time, Fall Time, Propagation Delay, Power Dissipation in CMOS, Fan-in, Fan-out, Complex Logic Structures, Complementary Static CMOS, Pseudo NMOS Logic, Dynamic CMOS Logic, CMOS Domino Logic, CMOS Pass Transistor Logic		
Unit:5	Sequential Circuit Design	7 Hours
Sequential Circuit Design, Latches and Flip Flops: D-latch, S-R latch and flip flop, J-K latch and flip flop.		
Unit :6	Data path VLSI System Component	8 Hours
Data path VLSI System Components: Half and full adder, half and full subtractor, Comparators, barrel shifters, Multiplexers, Demultiplexer, Binary Decoders, Equality Detectors, Priority Encoders.		
Total Lecture Hours		45 Hours

Text books

1	Neil H. E. WesteHarris, Principle of CMOS VLSI Design, 4th Edition, Addison Wesley VLSI Series.
----------	---

Reference Books

1	John P. Uyemura, Introduction to VLSI Circuits and Systems, Students Edition, Wiley Publication.
2	Sung-Mo Kang, Yusuf leblebici, CMOS VLSI Design, Third edition, 2008, TataMcGraw Hill.

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

B.Tech in V.L.S.I.

SoE No.
23VLSI-101

YCCE e- library book links [ACCESSIBLE FROM COLLEGE CAMPUS]	
1	http://103.152.199.179/YCCE/yccelibrary.html
MOOCs Links and additional reading, learning, video material	
1	https://nptel.ac.in/courses/108107129
2	https://nptel.ac.in/courses/106103116
3	https://nptel.ac.in/courses/117106092

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

B.Tech in V.L.S.I.

SoE No.
23VLSI-101

V SEMESTER **23VLS1504 : Lab. CMOS VLSI Design**

Course Outcomes:

Upon successful completion of the course the students will be able to

1. Understand and interpret the basic concepts of MOS transistors.
2. Apply the concept of CMOS as a switch to design digital logic circuits.
3. Analyze inverter design, characteristics and Performance parameters of CMOS Circuits.
4. Design and implement combinational and sequential circuits using different CMOS styles
5. Evaluate the performance of digital CMOS circuits using simulation tools.

Sr. No.	Experiments based on
1	To implement CMOS Inverter
2	To implement NAND and AND gate using CMOS
3	To implement NOR and OR gate using CMOS
4	To implement 3 input NAND and NOR gate using CMOS
5	To implement different Functions using CMOS
6	To implement Function MUX and DMUX using CMOS
7	To implement NAND and NOR gate S-R flip-flop using CMOS logic.
8	To implement NAND and NOR gate J-K flip-flop using CMOS logic.
9	To implement Full adder using CMOS
10	To implement Full Subtractor using CMOS
11	To implement Binary encoder using CMOS
12	Mini Project

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

SoE No.
23VLSI-101

B.Tech in V.L.S.I.

V SEMESTER

23VLS1505 : Digital system Modelling

Course Outcomes:

Upon successful completion of the course the students will be able to

1. **Understand** hardware description language and able to design and simulate digital systems using different abstraction levels.
2. **Apply and design** combinational and sequential logic circuits.
3. **Apply and design** the basics of synchronous sequential logic and finite state machines.
4. **Analyze** building blocks in digital system and explain the programmable devices and able to design digital systems using modern design tools.
5. **Evaluate** practical experiments to solve problems using an appropriate designing method.

Unit:1 Introduction of HDL

8 Hours

HDL Based Design flow, Requirements of HDL, Design Methodologies, Different Modelling styles, Introduction to Verilog, Elements of Verilog, Verilog Module definition, Elements of Module, Basic Concepts in Verilog, Reserved Keywords, Syntax & Semantics, Comments, Identifiers, Number Representation, System Representation, Verilog Ports, Verilog Data Types, Wire & Variables, Physical & Abstract, Constants, Parameter, Verilog Data Operators.

Unit:2 Data Flow Modelling

7 Hours

Data Flow Modelling, Delay, Continuous Assignment, Delayed Continuous assignment Design entry in Verilog & Test bench, Combinational blocks design, Compilation and synthesis, Timing analysis resolving signal values

Unit:3 Structural Modelling

8 Hours

Structural Modelling Feature, Module Instantiation, Gate level Primitives, Gate Delays, Switch Level Primitives, User Defined Primitives.

Unit:4 Behavioural Modelling,

7 Hours

Behavioural Modelling, Initial, Always, Procedural Assignment, Blocking and Non- Blocking assignments, Sequential & Parallel Blocks, Race around Condition, Timing Control, Procedural Statements, Conditional Statements if case loop repeat forever etc, Zero Delay Control, Event Based Timing Control, Compiler Directives, Assign Design, Force Release, Latch Models, FF Models, State Machine Coding, Moore and Mealy Machines.

Unit:5 Combinational & sequential system

8 Hours

Combinational & sequential system Design examples like Shift Registers, Counters, LFSR, Stacks and Queues, Multi bit Adders & Multiplier, Huffman Coding, Processor and Memory Model, CPU, System Tasks and Functions, Design Verification.




Unit :6 Introduction to FPGA

7 Hours

Digital Design Fundamentals, Combinational & Sequential design issues, Introduction to finite state machines, Moore & Mealy Machine, Introduction to programmable devices, PLA, PAL, PROM, Structure of CPLDs, Introduction to FPGA, Architecture, CLB, IOB, Programmable Interconnect Points, Different type of programmable switches used in PLDs.

Total Lecture Hours

45 Hours

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

SoE No.
23VLSI-101

B.Tech in V.L.S.I.

Text books

- | | |
|---|--|
| 1 | Samir Palnitkar , Verilog HDL: A Guide to Digital Design and Synthesis, 2 nd Edition, 2003, Prentice Hall |
|---|--|

Reference Books




- | | |
|---|--|
| 1 | Zainalabedin Navabi , Verilog Digital System Design, Second Edition ,Tata McGraw Hill, 2009. |
|---|--|

YCCE e- library book links [ACCESSIBLE FROM COLLEGE CAMPUS]

- | | |
|---|---|
| 1 | http://103.152.199.179/YCCE/yccelibrary.html . |
|---|---|

MOOCs Links and additional reading, learning, video material

- | | |
|---|---|
| 1 | https://onlinecourses.nptel.ac.in/noc20_cs63/ |
|---|---|

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

B.Tech in V.L.S.I.

SoE No.
23VLSI-101

V SEMESTER

23VLS1506 : Lab:- Digital System Modelling

Course Outcomes:

Upon successful completion of the course the students will be able to

1. **Understand** hardware description language and able to design and simulate digital systems using different abstraction levels.
2. **Apply and design** combinational and sequential logic circuits.
3. **Apply and design** the basics of synchronous sequential logic and finite state machines.
4. **Analyze** building blocks in digital system and explain the programmable devices and able to design digital systems using modern design tools.
5. **Evaluate** practical experiments to solve problems using an appropriate designing method.

Sr. No.	Experiments based on
1	Write data flow Verilog Codes of basic gates
2	Write data flow Verilog Codes for Multiplexer & Demultiplexer
3	Write data flow Verilog Codes for Decoder & Encoder
4	Write gate level Verilog Codes for Adder & Subtractor
5	Write gate level Verilog Codes for flip flops
6	Write structural Verilog Codes for Full adder using half adder
7	Write structural Verilog Codes for 3:8 Decoder using 2:4 decoder
8	Write behavioural Verilog code of digital circuits using if-else statement.
9	Write behavioural Verilog code of digital circuits using case statement.
10	Write Verilog code for Mealy and Moore sequence detector
11	Write a verilog code for 4 bit SISO using D-Flip Flop.
12	Write a verilog code for 4 bit Ripple Carry Adder
13	Mini Project

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

B.Tech in V.L.S.I.

SoE No.
23VLSI-101

V SEMESTER

23VLS1507 : Object Oriented Programming

Course Outcomes:

Upon successful completion of the course the students will be able to

1. Understand the concept of Object-Oriented Programming
2. Develop programs using arrays, functions.
3. Analyse the concept of classes, and objects
4. Analyse the concept of constructor, destructor and inheritance

Unit:1	Introduction	7 Hours
History of C++ and its relation to C , Structure of a C++ program , Principles of Object-Oriented Programming (OOP), OOP Paradigm, Basic Concepts of OOP, Benefits of OOP, Input/Output using cin, cout		
Unit:2	Token Expressions & Control Structures	8 Hours
Tokens, Keywords, Identifiers and Constants, Data Types, Type Compatibility, Variables, Operators in C++, Implicit Conversions, Operator Precedence, Control Structures.		
Unit:3	Functions in C++, Classes & Objects	7 Hours
The Main Function, Function Prototyping, Call by Reference, Return by Reference, Inline Functions, Function Overloading, Friend and Virtual Functions. Specifying a class, Member Functions, Static Member Functions, Arrays of Objects, Friend Function.		
Unit:4	Constructors & Destructors, Operator Overloading, Inheritance	8 Hours
Constructors, Parameterized Constructors, Copy Constructors, Dynamic Constructors, Destructors, Operator Overloading, Inheritance , types of inheritance, Polymorphism and virtual functions.		
Total Lecture Hours		30 Hours

Text books

- 1 Object Oriented programming with C++, E. Balagurusamy

Reference Books

- 1 Fundamentals of Data Structures in C++, Robert Lafore

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

B.Tech in V.L.S.I.




SoE No.
23VLSI-101

YCCE e- library book links [ACCESSIBLE FROM COLLEGE CAMPUS]

1	http://172.16.1.9/LocalGuru/listLectures.php?cid=29086f3420285fdf&bid=927d7542627865a3
---	---

MOOCs Links and additional reading, learning, video material

1	https://nptel.ac.in/courses/106105153
2	https://archive.nptel.ac.in/courses/106/105/106105153/
3	https://nptel.ac.in/courses/106105151
4	https://onlinecourses.nptel.ac.in/noc19_cs48/preview

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

B.Tech in V.L.S.I.

SoE No.
23VLSI-101

V SEMESTER

23VLS1508 : Lab. Object Oriented Programming

Course Outcomes:

Upon successful completion of the course the students will be able to

1. Understand the concept of Object Oriented Programming
2. Analyse the concept of Inheritance , Polymorphism, overloading
3. Develop appropriate data structure and algorithm design method for specific application
4. Understand the concept of File handling and exception handling

Sr. No.	Experiments based on
1	Implement the concept of Class and its data members and member functions in C++
2	Implement the concept of function and operator overloading in C++
3	Implement the concept of friend function
4	Implement the concept of class constructor and its type in C++
5	Implement the concept of Abstraction in C++
6	Implement the concept of all types of inheritance in C++
7	Implement the concept of run time polymorphism in C++
8	Implement the concept of Files using command line arguments in C++
9	Implement the concept of function templates and class template in C++
10	Implement the concept of exception in C++

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

SoE No.
23VLSI-101

B.Tech in V.L.S.I.

V SEMESTER 23VLS1521 : PE I:CAD for VLSI

Course Outcomes:

Upon successful completion of the course the students will be able to

1. Understand optimization techniques applied in the design and synthesis of VLSI circuits
2. Demonstrate proficiency in understanding and implementing algorithms used in VLSI CAD tools
3. Understand the fundamentals of Computer-Aided Design (CAD) tools for the design, analysis, synthesis, test, verification.
4. Use Computer-Aided Design (CAD) tools for the design, analysis, synthesis, test, verification.

Unit:1	Overview of digital logic design	6hrs
--------	----------------------------------	------

Simplification of switching functions, K-map-based reduction of switching functions.
Combinational logic design, Complex combinational logic modules such as multiplexers/demultiplexers, decoders, PLAs, and their use in standardized combinational logic design.

Unit:2	Overview of sequential logic design	6hrs
--------	-------------------------------------	------

Memory elements and time delay concepts, Flip-flops, latches, registers; Sequential circuit concepts and state diagrams; Clock-mode sequential circuits analysis and design; Synthesis of state diagrams; Fundamental-mode sequential circuits

Unit:3	Overview of hazards	6hrs
--------	---------------------	------

Analysis and design, hazards, races, and cycles. Logic element realization, Ideal switch based implementation

Unit:4	Introduction to VLSI CAD Algorithms and Tools	7hrs
--------	---	------

Overview of CAD algorithms and tools in VLSI design. , Introduction to key optimization and automation concept

Unit:5	Logic Synthesis Algorithms	7hrs
--------	----------------------------	------

Study of logic synthesis algorithms, Optimization techniques in logic synthesis, Hands-on exercises with logic synthesis tools.

Unit :6	Verification Algorithms in VLSI	7hrs
---------	---------------------------------	------

Functional and timing verification algorithms ,Model checking and formal verification techniques, Introduction to cutting-edge CAD tools

Total Lecture Hours	39 Hours
---------------------	----------

Text books

1	De Micheli G., Synthesis and Optimization of Digital Circuits, McGraw Hill, (1994).
---	---

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

B.Tech in V.L.S.I.

SoE No.
23VLSI-101

Reference Books

1	Devadas, S. A., Abhijith Ghosh, A., and Keutzer, K., Logic Synthesis, Kluwer Academic, (1998).
2	Brunvand, E., Digital VLSI Chip Design with Cadence and Synopsys CAD Tools, Addison-Wesley, (2010).

YCCE e- library book links [ACCESSIBLE FROM COLLEGE CAMPUS]

1	http://103.152.199.179/YCCE/yccelibrary.html
---	---

MOOCs Links and additional reading, learning, video material

1	https://archive.nptel.ac.in/courses/106/106/106106088/
2	https://archive.nptel.ac.in/courses/106/106/106106089/

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Yeshwantrao Chavan College of Engineering

Nagar Yuwak Shikshan Sanstha's
(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

B.Tech in V.L.S.I.

SoE No.
23VLSI-101

V SEMESTER

23VLS1522 : PE-I: Algorithm and Data Structure

Course Outcomes:

Upon successful completion of the course the students will be able to

1. Understand the trade-offs of algorithms and programming aspects
2. Apply various operation on data Structure
3. Analyze various types of Data Structure
4. Implement various types of algorithms and analyze performance of system
5. Develop programs using data structures and latest compilers

Unit:1	Introduction to Algorithms	8 Hours
Introduction to Algorithms, Basics of Algorithm, Sub Algorithms, Procedures and Functions, Analysis of Algorithms, Time and Space Complexity, Programming aspects with respect to structured programming, Top down and bottom Up Approach.		
Unit:2	Arrays	8 Hours
Arrays, Operations, Types, Representation of 1D, 2D arrays in memory, Sparse Matrices, Sorting, Quick Sort, Merge Sort, Insertion, Radix, Selection and Bubble Sort, Heap Sort, Searching , Linear, Binary Search, Hashing and collision Handling mechanism.		
Unit:3	Stack	7 Hours
Stack , Fundamentals, Operations, Push , Pop , Applications of Stacks, Evaluation of Expressions, Recursion, Stack Machines and Multiple Stacks, Queues , Operations, Add , Delete, Types of Queues , Priority Queues, Circular Queue, Dequeue.		
Unit:4	Linked Stacks and Queues	8 Hours
Fundamentals of singly, Doubly, Circular, Linked Stacks and Queues, Examples of Linked List, Circular Linked List, Doubly Linked List and Dynamic Storage Management, Garbage Collection, Compaction and Applications of Linked List, Operations of Polynomials, Generalized Linked List.		
Unit:5	Binary Tree	8 Hours
Basic Terminology, Binary Tree Traversals, Threaded Storage Representation, Binary Search Tree, Applications of Tree, Preliminary Treatment of AVL Trees, B-Trees, B+ Trees.		
Unit :6	List	7 Hours
Basic Terminology, Graph Representation, Matrix, List, Multi-List, Graph Traversals, Breath First Search, Depth First Search, Minimum Cost Spanning Trees, Shortest Path Algorithm, Topological Sort, Critical Path.		
Total Lecture Hours		45 Hours

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

SoE No.
23VLSI-101

B.Tech in V.L.S.I.

Textbooks

- 1 Fundamentals of Data Structures, Ellis Horowitz and Sartaj Sahani, Galgotia, Publication,
- 2 Data structure using C, Second Edition, Reema Thareja, Oxford Univ. Press

Reference Books




- 1 Data Structures and Program, Design in C, Kruse, Leung and Tondo, PHI
- 2 An Introduction to Data Structures with Applications, Tremblay & Sorenson, TMH
- 3 Data Structures, Schaum Series, Seymour Lipschutz, G.A. V. Pai, TMH

YCCE e- library book links [ACCESSIBLE FROM COLLEGE CAMPUS]

- 1 <http://103.152.199.179/YCCE/yccelibrary.html>

MOOCs Links and additional reading, learning, video material

- 1 <https://nptel.ac.in/courses/106102064>
- 2 <https://archive.nptel.ac.in/courses/106/106/106106127/>
- 3 https://onlinecourses.nptel.ac.in/noc20_cs85/preview

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

SoE No.
23VLSI-101

B.Tech in V.L.S.I.

V SEMESTER

23VLS1523 : PE-I: Semiconductor Device Modelling

Course Outcomes:

Upon successful completion of the course the students will be able to

1. **Understand** the physics of a new device
2. **Apply** suitable approximations and techniques to derive the model starting from drift-diffusion transport equations
3. **Analyze** MOS capacitance voltage characteristics and quantum mechanical effect
4. **Simulate** characteristics of a simple device using SPICE tools

Unit:1	Semiconductor Devices: Electrons and holes in semiconductor, Energy band model, Density of states, thermal equilibrium and the fermi function	7 Hours
Unit:2	Motion and Recombination of Electrons and holes, Thermal motion, drift, diffusion current, Thermal generation, Quasi equilibrium and quasi fermi levels	6 Hours
Unit:3	PN and metal semiconductor junctions, Energy band diagram, depletion layer model, Capacitance voltage characteristics, junction breakdown, current continuity equation	6 Hours
Unit:4	small signal model of diode, Metal semiconductor junctions, Schottky barriers, Quantum mechanical tunnelling, Schottky diodes, ohmic contacts	6 Hours
Unit:5	MOS capacitor, MOS capacitance voltage characteristics, Poly Si gate depletion, quantum mechanical effect.	7 Hours
Unit :6	MOSFET, High mobility FETs, GaAs MESFET, HEMT, Steep retrograde doping	7 Hours
Total Lecture Hours		39 Hours

Textbooks

1	B. G. Streetman and S. Banerjee, Solid State Electronic Devices, 6th Edition, PHI Private Limited, 2011.
	C. C. Hu, Modern Semiconductor Devices for Integrated Circuits, Pearson Education, 2010
2	Robert E. Miles, Christopher M. Snowden, Semiconductor device modelling, 1989
3	G. Massobrio and P. Antognetti, Semiconductor Device Modelling with SPICE, 2nd Edition, TMH, 2010.

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

B.Tech in V.L.S.I.

SoE No.
23VLSI-101

Reference Books




- | | |
|---|---|
| 1 | Introduction to Semiconductor Materials and devices by M.S Tyagi, John Wiley & Sons, 5th Edition, 2005. |
| 2 | T. A. Fjeldly, T. Ytterdal, and M. Shur, "Introduction to Device Modelling and Circuit Simulation", John Wiley, 1998. |
| 3 | Semiconductor Physics and Devices Basic Principles, Donald A. Neuman, fourth edition, Mc Graw Hill. |

YCCE e- library book links [ACCESSIBLE FROM COLLEGE CAMPUS]

- | | |
|---|---|
| 1 | http://103.152.199.179/YCCE/yccelibrary.html |
|---|---|

MOOCs Links and additional reading, learning, video material

- | | |
|---|---|
| 1 | https://onlinecourses.nptel.ac.in/noc23_ee35/preview |
| 2 | https://archive.nptel.ac.in/courses/117/106/117106033/ |

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

SoE No.
23VLSI-101

B.Tech in V.L.S.I.

V SEMESTER

23OE3521 : Introduction to Fintech

Course Outcomes:

Upon successful completion of the course the students will be able to:

1.Understand the Evolution and Ecosystem of FinTech: Demonstrate knowledge of the historical development of FinTech and the various players in the ecosystem including startups, financial institutions, regulators, and consumers.

2.Analyze Key FinTech Technologies and Trends: Explain and evaluate the core technologies driving FinTech innovation such as blockchain, artificial intelligence, machine learning, big data, and APIs.

3.Apply FinTech Concepts in Real-world Scenarios: Apply FinTech tools and techniques to solve problems in banking, investment, insurance, and personal finance using case studies and practical examples.

4. Design Innovative FinTech Solutions: Develop or propose innovative financial products or services leveraging emerging technologies, with a focus on improving accessibility, efficiency, and transparency in financial services.

Unit:1	Introduction to Fintech	8 Hrs
---------------	--------------------------------	--------------

Definition and evolution of fintech, Traditional finance vs. fintech innovations, Key players in the fintech ecosystem (startups, incumbents, regulators), Fintech's role in financial inclusion

Unit:2	Core Technologies Powering Fintech	7 Hrs
---------------	---	--------------

Blockchain, Bitcoin, Stock Market and cryptocurrencies, Artificial intelligence and machine learning in finance, Big data analytics and its applications, Cyber-security and fraud prevention in fintech

Unit 3	Digital Payments and Open Banking	8 Hrs
---------------	--	--------------

Evolution of digital payments (mobile wallets, contactless payments), Open banking and API-driven financial services, The role of fintech in remittances and cross-border transactions Case studies: PayPal, Stripe, Revolut

Unit 4	Financial Markets	7 Hrs
---------------	--------------------------	--------------

Introduction to Financial Markets, Types of Financial Markets, Key Functions of Financial Markets, Capital Formation & Investment Platform

Unit:5	Algorithmic Trading & Quantitative Finance	8 Hrs
---------------	---	--------------

Trading Mechanisms, Technical & Fundamental Analysis, Basics of algorithmic trading, Intro to quant models and backtesting, Using Python/R in trading algorithms, API-based trading and data fetching, FinTech Applications in Stock Markets

Unit :6	Regulatory Environment, Framework and Future Trends	7 Hrs
----------------	--	--------------

Fintech regulations and compliance, Ethical considerations and data privacy in fintech, Role of SEBI and other regulators, Insider trading and market manipulation laws, Compliance and audit practices.

Emerging trends: DeFi (Decentralized Finance), Central Bank Digital Currencies (CBDCs), The future of fintech: Opportunities and challenges

Total Lecture Hours	45 Hours
----------------------------	-----------------

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

B.Tech in V.L.S.I.

SoE No.
23VLSI-101

Textbooks:

1. Susanne Chishti, Janos Barberis (2016). The FINTECH Book: The Financial Technology
2. Susanne Chishti, Janos Barberis (2016), THE FINTECH BOOK: The financial technology handbook for investors, entrepreneurs and visionaries, Wiley.
3. Sanjay Phadke (2020) Fintech future, The Digital DNA of Finance, SAGE Publishing.

Reference Books:

1. Agustin Rubini (2018). Fintech in a Flash: Financial Technology Made Easy, Zaccheus Entertainment, 3rd edition (2018), ISBN-10: 1547417161, ISBN-13: 978-1547417162.
2. Choudhary, P., & Thenmozhi, M. (2024). Fintech and financial sector: ADO analysis and future research agenda. International Review of Financial Analysis, 103201.
3. Harsono, I., & Suprati, I. A. P. (2024). The Role of Fintech in Transforming Traditional Financial Services. Accounting Studies and Tax Journal (COUNT), 1(1), 81-91.
4. EY Tech Trends Chapter VIII: top FinTech trends in 2023

MOOCs Links and additional reading, learning, video material

1. <https://corporatefinanceinstitute.com/course/intro-to-fintech/>
2. <https://www.udemy.com/course/fintech-frontiers-introduction-to-fintech/>
3. <https://www.futurelearn.com/courses/introduction-to-fintech-and-financial-innovation>
4. <https://www.mygreatlearning.com/academy/learn-for-free/courses/introduction-to-fintech>

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

B.Tech in V.L.S.I.

SoE No.
23VLSI-101

V SEMESTER 23OE3522 : Financial Analytics

Course Outcomes		
Upon successful completion of the course the students will be able to: <ol style="list-style-type: none"> 1. Apply financial analytics techniques to real-world business problems. 2. Analyze financial data using statistical and computational tools to Construct and interpret financial models for forecasting and decision-making. 3. Evaluate risks and optimize financial portfolios. 		
Unit 1	Introduction to Financial Analytics	7 Hrs.
Introduction to Financial Systems and Statements: Overview of Financial Analytics and its role in decision-making, Introduction to financial markets and instruments, Time value of money, interest rates, annuities, Financial statements: Balance Sheet, Income Statement, and Cash Flow Statement, Financial ratios and performance metrics		
Unit 2	Financial Data and Preprocessing Techniques	8 Hrs.
Basic corporate financial predictive modelling- Project analysis- cash flow analysis- cost of capital Financial Break even modelling, Capital Budget model-Payback, NPV, IRR.		
Unit 3	Exploratory Financial Data Analysis	8 Hrs.
Time-series components: trend, seasonality, cyclical, Descriptive analytics of stock and commodity data, Moving averages and smoothing techniques, Correlation and covariance of financial assets, Visualization: candlestick charts, return plots, correlation heatmaps		
Unit 4	Predictive Modeling in Finance:	8Hrs.
Introduction to regression analysis (linear, multiple), Time-series forecasting: AR, MA, ARIMA models, Introduction to machine learning in finance: decision trees, random forests, Case study: Stock price prediction using ARIMA/ML models		
Unit 5	Basics of Investment and Risk Analysis	8 Hrs.
Return and risk: Definitions and examples, Types of financial risk: market, credit, operational, Calculating returns and standard deviation using stock data, Diversification and correlation		
Unit 6	Risk Management and Portfolio Analytics	7 Hrs
Intro to Portfolio Analytics, What is a portfolio? Portfolio basics: building a basket of assets, calculating portfolio return and risk, Diversification benefits using correlation matrix, Introduction to efficient frontier (conceptual only)		
Total Lecture		45 Hours

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

SoE No.
23VLSI-101

B.Tech in V.L.S.I.

Textbooks:

1. Financial analytics with R by Mark J. Bennett, Dirk L. Hugen, Cambridge university press.
2. Haskell Financial Data Modeling and Predictive Analytics Paperback – Import, 25 Oct 2013 by Pavel Ryzhov.
3. Statistics and Data Analysis for Financial Engineering: With R Examples
David Ruppert, Springer 2nd Edition ISBN: 978-1493926138

Reference Books:

1. Quantitative Financial Analytics: The Path To Investment Profits Paperback – Import, 11 Sep 2017
2. Introduction to Financial Analysis by Kenneth S. Bigel, Touro College, OPEN TOURO, NEW YORK.

YCCE e- library book links [ACCESSIBLE FROM COLLEGE CAMPUS]

1. <http://103.152.199.179/YCCE/yccelibrary.html>

MOOCs Links and additional reading, learning, video material

1. <https://www.coursera.org/learn/financial-analysis>
2. <https://www.edx.org/learn/financial-analysis/babson-college-financial-analysis-for-decision-making>
3. <https://www.youtube.com/watch?v=hnlByld08Io>

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

SoE No.
23VLSI-101

B.Tech in V.L.S.I.

V SEMESTER 23OE3524 : Lifestyle Diseases

Course Outcomes

Upon successful completion of the course the students will be able to:

- 1. Understand Public Health and Lifestyle Diseases:**
Recognize and explain the fundamental principles of public health and the impact of lifestyle on health. Discuss various lifestyle-related diseases and how they can be prevented through effective lifestyle management.
- 2. Analyze Causes and Risk Factors of Lifestyle Diseases:**
Identify and enumerate the causes, risk factors, and pathophysiology of common lifestyle diseases such as atherosclerosis, hypertension, stroke, diabetes, obesity, nephritis, and liver diseases. Study cases before and post COVID-19.
- 3. Apply Diagnostic and Preventive Strategies:**
Demonstrate the ability to outline diagnostic methods, interpret basic test results, and describe preventive, therapeutic, and management strategies for lifestyle-related diseases.
- 4. Integrate Nutrition and Holistic Health Approaches:**
Relate the principles of nutrition, Yoga, and Meditation to health and disease prevention. Identify common nutritional disorders and discuss dietary guidelines for managing specific health conditions.

Unit 1	Introduction to Public Health and Lifestyle Diseases	8 Hrs.
Concepts of lifestyle and its impact on health, Introduction to lifestyle diseases: definition, prevalence, and significance, Role of behavioral and environmental factors in lifestyle diseases, Impact of pandemics on public health: Focus on COVID-19, Behavioral changes during and after COVID-19: hygiene, mobility, mental health, Role of public health systems and global responses to COVID-19		
Unit 2	Causes and Risk Factors of Lifestyle Diseases – Part I	8 Hrs.
Pathophysiology and risk factors of: Atherosclerosis, Hypertension, Stroke Role of genetics, diet, physical activity, stress, and addiction, Early signs, symptoms, and progression of these diseases Increased cardiovascular risk due to COVID-19 infection and lockdown-related inactivity, Exacerbation of hypertension and cerebrovascular conditions during the pandemic, Role of stress, anxiety, and social isolation during lockdowns as risk factors		
Unit 3	Causes and Risk Factors of Lifestyle Diseases – Part II	7 Hrs.
Pathophysiology and risk factors of: Diabetes mellitus (Type 1 and Type 2), Obesity and metabolic syndrome, Nephritis and liver diseases (e.g., fatty liver, hepatitis), Complications and co-morbidities associated with these diseases, Link between COVID-19 and metabolic disorders like diabetes and obesity, post-COVID complications affecting kidneys and liver, Impact of steroid use and viral infection on metabolic health		

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

SoE No.
23VLSI-101

B.Tech in V.L.S.I.

Unit 4	Diagnosis, Prevention, and Management	8Hrs.
Common diagnostic tools: blood tests, imaging, and clinical assessments, Basics of interpreting diagnostic results, Prevention strategies: primary, secondary, and tertiary levels, Conventional and lifestyle-based treatment approaches, Public health policies and screening programs, COVID-19 diagnostic methods and interpreting test results (RT-PCR, antibody tests), Managing post-COVID conditions: fatigue, inflammation, long COVID symptoms, Preventive strategies: vaccines, immunity, and their public health implications		
Unit 5	Holistic Approaches to Health – Yoga and Meditation	7 Hrs.
Principles and practices of Yoga and their physiological benefits, Role of Meditation in stress management and mental health, Scientific evidence supporting Yoga and Meditation in disease prevention and recovery, Integrating Yoga and Meditation into daily routines for holistic health, Role of Yoga and Meditation in COVID-19 recovery and mental well-being, Evidence-based studies on Yoga for lung function, stress reduction during/post-COVID		
Unit 6	Nutrition and Dietary Management in Lifestyle Diseases	7 Hrs
Basics of nutrition: macronutrients and micronutrients, Common nutritional disorders and deficiencies, Role of diet in prevention and management of lifestyle diseases, Dietary guidelines and therapeutic diets for diabetes, hypertension, obesity, liver and kidney diseases, Role of traditional diets and functional foods, Nutrition for immunity: Key nutrients during and after COVID-19, Dietary support in COVID-19 recovery: high-protein, anti-inflammatory diets, Addressing post-COVID appetite loss, taste/smell dysfunction, and digestive issues, Nutritional rehabilitation in post COVID cases.		
Total Lecture		45 Hours
Textbooks:		
1.	"Textbook of Lifestyle Medicine" by James M. Rippe, Publisher: CRC Press	
2.	"Nutrition and Lifestyle for Health and Wellness" by Garry Egger, Katrina Arthur, and Tamara Bucher, Publisher: Oxford University Press	
Reference Books:		
1	“Lifestyle Medicine” by Garry Egger, Andrew Binns, and Stephan Rossner, Publisher: Academic Press	
2	“Essentials of Human Nutrition” by Jim Mann and A. Stewart Truswell, Publisher: Oxford University Press	
3	“Yoga and Cardiovascular Management” by Swami Satyananda Saraswati, Publisher: Bihar School of Yoga	
4	“Clinical Dietetics and Nutrition” by F.P. Antia and Philip Abraham, Publisher: Oxford University Press (India)	
5	5. “Post-COVID Recovery: Diet, Lifestyle, and Mental Health” by Rujuta Diwekar (for popular/scientific audience) Publisher: Self-published	

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

B.Tech in V.L.S.I.

SoE No.
23VLSI-101

YCCE e- library book links [ACCESSIBLE FROM COLLEGE CAMPUS]

1 <http://103.152.199.179/YCCE/yccelibrary.html>

MOOCs Links and additional reading, learning, video material

1 1. Lifestyle Medicine: Improving the Future of Health Care

- Platform: edX (Offered by Doane University)

Link: <https://www.edx.org/course/lifestyle-medicine>

2 Nutrition, Exercise and Sports

- Platform: Coursera (Offered by Wageningen University)

Link: <https://www.coursera.org/learn/nutrition-exercise>

3 Yoga and Well-being

- Platform: SWAYAM (offered by various Indian universities)

Link: <https://swayam.gov.in> → Search “Yoga” or “Health & Wellness”

4 CDC Resources:

- Chronic Disease Prevention Tools

<https://www.cdc.gov/chronicdisease/index.htm>

Post-COVID Conditions (Long COVID)

<https://www.cdc.gov/coronavirus/2019-ncov/long-term-effects/>

5 TED Talks

- Dean Ornish: The world's killer diet

https://www.ted.com/talks/dean_ornish_on_healing

On reversing heart disease with lifestyle changes

Rujuta Diwekar: The Indian Diet Wisdom

(YouTube Link): <https://www.youtube.com/watch?v=d8CkP3Ioxcc>

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

SoE No.
23VLSI-101

B.Tech in V.L.S.I.

V SEMESTER 23OE3525 : Holistic Nutrition

Course Outcomes		
Upon successful completion of the course the students will be able to:		
1. Discuss the role of essential nutrients in physical, mental and emotional wellness		
2. Discuss the role of deficiencies in essential nutrients in the disease process		
3. Explain how the standard American diet relates to the disease process		
4. Identify five contemporary eating “styles” and lists the pros and cons of each		
Unit 1	NUTRITION AND HEALTH	8 Hrs.
Introduction to the principles of nutrition; Basics of nutrition including; micronutrients (vitamins and minerals), the energy-yielding nutrients (Carbohydrates, Lipids and Proteins), metabolism, digestion, absorption and energy balance.		
Unit 2	AYURVEDA – MIND/BODY HEALING	7 Hrs.
Philosophy of Holistic Nutrition with spiritual and psychological approaches towards attaining optimal health; Principles and practical applications of Ayurveda, the oldest healing system in the world. Three forces – Vata, Pitta and Kapha, that combine in each being into a distinct constitution. Practical dietary and lifestyle recommendations for different constitutions will also be explored in real case studies.		
Unit 3	COMPARATIVE DIETS	8 Hrs.
Evaluating principles of food dynamics, nutrient proportions, holistic individuality, the law of opposites, food combining, and more. Therapeutic benefits and limitations of several alternative diet approaches, including: modern diets, food combining, high protein diets, Vegetarian approaches, cleansing and detoxification diets		
Unit 4	PREVENTIVE HEALTH CARE	7 Hrs.
Proper nutrition protection against, reverse and/or retard many ailments including: osteoporosis, diabetes, atherosclerosis and high blood pressure, arthritis, cancer, anemia, kidney disease and colon cancer. Current research developments on phytochemicals, antioxidants and nutraceuticals will be explored.		
Unit 5	NUTRITION AND ENVIRONMENT	7 Hrs.
Maintain and promote health, Right to self-determination and self-knowledge, Nutrition principles which promote health and prevent disease, Safety of our food supply, naturally occurring and environmental toxins in foods, microbes and food poisoning.		
Unit 6	CASE STUDY	8 Hrs
Practical dietary and lifestyle recommendations for different constitutions will also be explored in real case studies. Case study for Body and Mind Healing		
Total Lecture		45 Hours

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

B.Tech in V.L.S.I.

SoE No.
23VLSI-101

Textbooks:

- | | |
|----|---|
| 1. | Desai, B. B., Handbook of Nutrition and Diet. Marcel Dekker, New York. 2000 |
| 2. | Macrae, R., Rolonson Roles and Sadlu, M.J. 1994. Encyclopedia of Food Science & Technology & Nutrition. Vol. XI. Academic Press |

Reference Books:




- | | |
|---|---|
| 1 | Modern Nutrition in Health & Disease by Young & Shils. |
| 2 | Nutritive Value of Indian Foods.- by C. Gopalan, B. V. Rama Sastri, S. C. Balasubramanian |

YCCE e- library book links [ACCESSIBLE FROM COLLEGE CAMPUS]

- | | |
|---|---|
| 1 | http://103.152.199.179/YCCE/yccelibrary.html |
|---|---|

MOOCs Links and additional reading, learning, video material

- | | |
|---|---|
| 1 | https://ayurhealing.net/blog/ayurveda-and-mind-body-health/ |
| 2 | https://www.healthline.com/nutrition/ayurvedic-diet |
| 3 | https://headachejournal.onlinelibrary.wiley.com/doi/10.1111/head.12363 |
| 4 | https://www.ayurveda-products.eu/content/ayurvedic-lifestyle-and-recipes/ayurvedic-nutrition |

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

SoE No.
23VLSI-101

B.Tech in V.L.S.I.

V SEMESTER

MDM3VLS103 : Switching Theory

Course Outcomes:

Upon successful completion of the course the students will be able to
CO1: Design and Analyze multilevel logic Network and Threshold logic for nanotechnologies.
CO2: Analyze testing of combinational circuits, Fault Models.
CO3: Design and analyze the synchronous and asynchronous sequential circuits.
CO4: Identify and test the sequential machines with experiments

Unit:1	Multi-level logic synthesis Technology-independent synthesis: Factoring, Decomposition, Extraction, Substitution and Technology mapping: steps in technology mapping.	7 Hours
Unit:2	Threshold logic for nanotechnologies Threshold elements, Capabilities and limitations of threshold logic, Elementary properties, synthesis of threshold networks: Unate function, Identification & Realization of threshold function	7 Hours
Unit:3	Testing of combinational circuits Fault models, Structural testing, Delay fault testing, Synthesis for testability, Testing for nanotechnologies	7 Hours
Unit:4	Synchronous sequential circuits Memory elements and their excitation functions, synthesis of synchronous sequential circuits, Moore and Mealy machines, finite state machine flow charts, tables	7 Hours
Unit:5	Asynchronous sequential circuits Asynchronous sequential circuits, Modes of operation, Hazards, Synthesis of SIC fundamental-mode circuits.	7 Hours
Unit :6	Testing of sequential circuits Experiments, Homing experiments, Distinguishing experiments, Machine Identification, Checking experiments, Built-in-self-test(BIST)	7 Hours
Total Lecture Hours		42 Hours

Textbooks

1	Switching & Finite Automata Theory: ZviKohavi, Niraja K. Jha, Third Edition 2010, Cambridge University Press
---	--

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

B.Tech in V.L.S.I.

SoE No.
23VLSI-101

Reference Books

1 Modern Switching Theory and Digital Design, Lee S.C, PHI Edition

2 Digital Logic and Computer Design, M.Morris Mano, PHI Edition

YCCE e- library book links [ACCESSIBLE FROM COLLEGE CAMPUS]

1 <http://103.152.199.179/YCCE/yccelibrary.html>

MOOCs Links and additional reading, learning, video material




1 https://onlinecourses.nptel.ac.in/noc19_cs74/unit?unit=64&lesson=65

2 https://onlinecourses.nptel.ac.in/noc19_cs74/unit?unit=64&lesson=66

3 https://onlinecourses.nptel.ac.in/noc19_cs74/unit?unit=64&lesson=67

4 https://onlinecourses.nptel.ac.in/noc19_cs74/unit?unit=64&lesson=68

5 https://onlinecourses.nptel.ac.in/noc19_cs74/unit?unit=64&lesson=69

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)



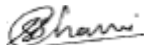
B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

B.Tech in V.L.S.I.

SoE No.
23VLSI-101

V SEMESTER

Mandatory Learning Course (MLC)
MLC2125 : YCAP5

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	

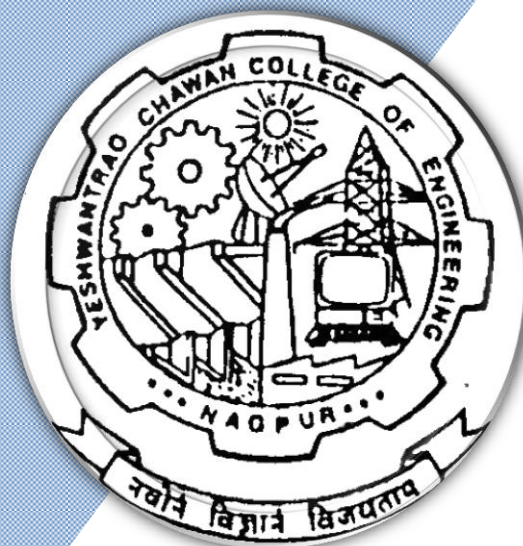
Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

(Accredited 'A++' Grade by NAAC with a score of 3.6)

Hingna Road, Wanadongri, Nagpur - 441 110



Bachelor of Technology SoE & Syllabus 2023 6th Semester

(Department of Electronics Engineering)

B. Tech in VLSI



Nagar Yuwak Shikshan Sanstha's
Yeshwantrao Chavan College of Engineering
 (An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)
B.TECH SCHEME OF EXAMINATION 2023
 (Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)
B. Tech Electronics Engineering(VLSI Design and Technology)

SoE No.
23VLSI-101

SN	Sem	Type	BoS/Deptt	Sub. Code	Subject	T/P	Contact Hours				Credits	% Weightage			ESE Duration Hours
							L	T	P	Hrs		MSEs*	TA**	ESE	
SIXTH SEMESTER															
1	6	PC	EE	23VLS1601	Digital Signal Processing	T	3	0	0	3	3	30	20	50	3
2	6	PC	EE	23VLS1602	Lab: Digital Signal Processing	P	0	0	2	2	1		60	40	
3	6	PC	EE	23VLS1603	VLSI Verification and Testing	T	3	0	0	3	3	30	20	50	3
4	6	PC	EE	23VLS1604	Design Thinking and Research Methodology	T	2	0	0	2	2	30	20	50	3
5	6	PE	EE		Professional Elective-II	T	3	0	0	3	3	30	20	50	
6	6	PE	EE		Lab : Professional Elective-II	P	0	0	2	2	1		60	40	3
7	6	PE	EE		Professional Elective-III	T	3	0	0	3	3	30	20	50	3
8	6	PE	EE		Lab : Professional Elective-III	P	0	0	2	2	1		60	40	
9	6	MDM	EE		MD Minor Course-IV	T	3	0	0	3	3	30	20	50	3
10	5	VSEC-4	EE	23VLS1605	Lab : Electronics Design Automation	P	0	0	2	4	2		60	40	
11	6	STR	EE	23VLS1606	Project Phase-I	P	0	0	4	4	2		60	40	
TOTAL							17	0	12	31	24				

List of Mandatory Learning Course (MLC)

1	6	HS		MLC126	YCAP6 :	A	3	0	0	3	0				
---	---	----	--	--------	---------	---	---	---	---	---	---	--	--	--	--

Professional Electives - II

1	6	PE-II	EE	23VLS1621	PE-II : CMOS Subsystem Design
2	6	PE-II	EE	23VLS1622	PE-II : Lab : CMOS Subsystem Design
3	6	PE-II	EE	23VLS1623	PE-II : Synthesis & Optimisation of VLSI Circuits
4	6	PE-II	EE	23VLS1624	PE-II : Lab : Synthesis & Optimisation of VLSI Circuits
5	6	PE-II	EE	23VLS1625	PE-II : Quantum Computing
6	6	PE-II	EE	23VLS1626	PE-II : Lab : Quantum Computing

Professional Electives - III

1	6	PE-III	EE	23VLS1641	PE-III : Analog VLSI Design
2	6	PE-III	EE	23VLS1642	PE-III : Lab : Analog VLSI Design
3	6	PE-III	EE	23VLS1643	PE-III : FPGA-Based System Design
4	6	PE-III	EE	23VLS1644	PE-III : Lab : FPGA-Based System Design
5	6	PE-III	EE	23VLS1645	PE-III : System C
6	6	PE-III	EE	23VLS1646	PE-III : Lab : System C

		July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Date of Release	Version	



Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

B.Tech in V.L.S.I.

SoE No.
23VLSI-101

VI SEMESTER **23VLS1601 : Digital Signal Processing**

Course Outcomes:

Upon successful completion of the course the students will be able to

1. Interpret, represent and process discrete signals and systems
2. Analyse Discrete Fourier transform using standard transforms and properties and compute DFT efficiently by using decimation in time and decimation in frequency algorithms.
3. Design, implement, analyze IIR & FIR digital filters for processing of discrete time signals.
4. Explore multirate filter banks and develop understanding of both theoretical and practical aspects of multirate signal processing

Unit:1	Discrete Time (DT) Signals and System, Classification of DT signals, classification of DT systems, linear Convolution, Sampling and reconstruction.	8 Hours
Unit:2	Discrete Time Fourier Transform, Discrete Fourier Transform, Computation of DFT, Properties of DFT, convolution of data sequences, FFT algorithms, Decimation in time, Decimation in Frequency	7 Hours
Unit:3	Digital Filter structures: FIR digital filter structures, IIR digital filter structures, Lattice structures, Finite word length effect	8 Hours
Unit:4	IIR Digital filter Design, Bilinear transformation, Impulse invariant transformation, Low pass IIR digital filters, Butterworth and Chebyshev filter	7 Hours
Unit:5	FIR Digital Filter Design, FIR filter design using windowing techniques	8 Hours
Unit :6	Multi-rate Digital Signal processing fundamentals of Multirate Digital Signal Processing, sampling rate alteration, multi-rate structures, Decimator and Interpolator and Multistage design.	7 Hours
Total Lecture Hours		45 Hours

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

B.Tech in V.L.S.I.

SoE No.
23VLSI-101

Textbooks

- | | |
|---|---|
| 1 | Digital Signal Processing: Principles, Algorithms, and Applications Dimitris Manolakis and John G Proakis 4th Edition Pearson |
| 2 | Digital Signal Processing Oppenheim 3rd Edition Prentice Hall |

Reference Books




- | | |
|---|---|
| 1 | Ifeachor and Jervis, "Digital Signal Processing", Pearson Education India. |
| 2 | DeFatta D J, Lucas J G and Hodgkiss W S, "Digital Signal Processing", J Wiley and Sons, Singapore, 1988 |

YCCE e- library book links [ACCESSIBLE FROM COLLEGE CAMPUS]

- | | |
|---|---|
| 1 | http://103.152.199.179/YCCE/yccelibrary.html |
|---|---|

MOOCs Links and additional reading, learning, video material

- | | |
|---|---|
| 1 | https://archive.nptel.ac.in/courses/108/101/108101174/ |
| 2 | https://nptel.ac.in/courses/117102060 |

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

B.Tech in V.L.S.I.

SoE No.
23VLSI-101

VI SEMESTER **23VLS1602 : Lab. Digital Signal Processing**

Course Outcomes:

Upon successful completion of the course the students will be able to

- 1 Understand and Apply the Knowledge of discrete-time signals and systems for signal analysis
2. Apply DFT for the analysis of digital signals and systems
3. Design various Filter structures and IIR and FIR filters, Muti-rate Systems
4. Apply Matlab Programming concept on Discrete signal and perform its software analysis

Sr. No.	Experiments based on
1	To Perform Sampling and Reconstruction
2	Generation of Discrete Time Signal
3	Operations on Discrete time signals
4	To compute DFT and IDFT of Discrete Time Signals.
5	Calculate the DFT of the given sequence using FFT
6	Linear Convolution using FFT
7	Circular Convolution using FFT
8	Design of filter using Bilinear Transformation
9	To design FIR and IIR filter.
10	To perform Upsampling and Downsampling on discrete time signal.
11	To illustrate signal processing application

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

B.Tech in V.L.S.I.

SoE No.
23VLSI-101

VI SEMESTER **23VLS1603 : VLSI Verification and Testing**

Course Outcomes:

Upon successful completion of the course the students will be able to

1. **Understands** the fundamental concepts of VLSI testing, including fault models, test generation, and Design-for-Testability (DFT) techniques.
2. **Apply** functional and structural testing methods to verify digital circuits.
3. **Analyze** different fault models and evaluate their impact on circuit performance and test coverage.
4. **Evaluate** the effectiveness of test methodologies by measuring fault coverage and optimizing test patterns for better defect detection.

Unit:1	Overview Of Testing	8 Hours
---------------	---------------------	----------------

Design Process, Verification, Faults & Their Detection, Test Pattern Generation, Fault Coverage, Types Of Tests, Test Application, Testing Economics. Defects, Failures, and Faults: Physical Defects, Failures Modes, Faults, Fault Equivalence and Dominance, Fault Collapsing

Unit:2	Simulation.	8 Hours
---------------	-------------	----------------

Logic Simulation, Approaches to Simulation, Fault Simulation & Their Results. Testability Measures: SCOAP Controllability and Observability

Unit:3	Automatic Test Pattern Generator	8 Hours
---------------	----------------------------------	----------------




Binary Decision Diagram, Reduction rules and Algorithms, Ordered Binary Decision Diagram, ROBDDs, Automatic Test Pattern Generation: D-Algorithm, Critical Path Extensions to D-Algorithm PODEM, FAN.

Unit:4	Scan Design & Boundary Scan Architecture	7 Hours
---------------	--	----------------

Ad Hoc Techniques, Scan-Path Design, Test pattern generation, Test Pattern Application, Scan architectures, multiple scan chains, Partial Scan Testing, Boundary Scans Architecture, Modes of Operation.

Unit:5	Built In Self-Test:	7 Hours
---------------	---------------------	----------------

Pseudorandom Test Pattern Generation, Response Compaction, BIST Architectures.

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

B.Tech in V.L.S.I.

SoE No.
23VLSI-101

Unit :6	Testing	7 Hours
Memory Testing: Types of Memory Testing, Functional Testing Schemes, Testing FPGAs and Microprocessors: Testability Of FPGAs, Testing RAM- Based FPGAs, Testing Microprocessors, Synthesis For Testability.		
Total Lecture Hours		45 Hours

Text books

- 1 "Essentials of Electronic Testing for Digital, Memory, and Mixed-Signal VLSI Circuits", Michael L. Bushnell and Vishwani D. Agrawal, B.S.Publications, 2000

Reference Books

- 1 "Principles of Testing Electronic Systems", 2nd edition Samiha Mourad, Yervant Zorian
- 2 "Digital Systems Testing and Testable Design" , Miron Abramovici, Melvin Breuer and Arthur Friedman, IEEE press.
- 3 "A Guide to VHDL" by Stanley Mazor, 2nd Edition, Kluwer Academic Press, 2007
- 4 "HDL Chip Design" by Douglas Smith, 3rd Edition, Doone Publications, 2008
- 5 "Rapid Prototyping of Digital Systems", by J. O. Hamblen and M. Furman, Kluwer Academic Publishers. 2001

YCCE e- library book links [ACCESSIBLE FROM COLLEGE CAMPUS]

- 1 <http://103.152.199.179/YCCE/yccelibrary.html>

MOOCs Links and additional reading, learning, video material

- 1 <https://archive.nptel.ac.in/courses/106/103/106103116/>
- 2 <https://nptel.ac.in/courses/106103016>

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

SoE No.
23VLSI-101

B.Tech in V.L.S.I.

VI SEMESTER

23VLS1604 : Design Thinking in VLSI Design & Research Methodology

Course Outcomes:

Upon successful completion of the course the students will be able to

- 1: Explain the principles of design thinking and the phases of the research process in engineering contexts.
- 2: Apply appropriate research methods and data collection techniques to identify and define engineering problems.
- 3: Analyze collected data using suitable statistical tools and evaluate research findings to draw valid conclusions.
- 4: Design and construct technical reports and research papers adhering to ethical standards and scholarly conventions.

Unit:1	Introduction to Research and the Design Thinking Process in Electronics Engineering:	7 Hours
---------------	---	----------------

Basics of Engineering Research - Definition and scope of research in Electronics Engineering, Role of innovation in Electronics. Introduction to Design Thinking - Five phases: Empathize, Define, Ideate, Prototype, Test. Problem Identification in Electronics- Observation techniques, Understanding user needs: interviews and surveys in technical contexts, Problem statement formulation (e.g. Signal and Image processing and analysis, Healthcare and Biomedical Engineering, etc.). Empathy and Need Finding in Electronics Engineering- Empathizing with end-users: healthcare, communication, automation, etc., Case studies of empathetic design in electronics products.




Unit:2	Research Design, Data Interpretation, and Ethics in Electronics:	8 Hours
---------------	---	----------------

Research Process in Engineering- Research design: experimental, analytical, simulation-based, Formulating hypotheses in electronics. Data Collection and Analysis - Tools: sensors, simulation software, MATLAB, Python, Quantitative and qualitative data in electronics research, Data interpretation and drawing conclusions.

IPR, Scholarly Publishing And Entrepreneurships: IPR- intellectual property rights and patent law, commercialization, copy right, royalty, trade related aspects of intellectual property rights (TRIPS); scholarly publishing- IMRAD concept and design of research paper, citation and acknowledgement, Opportunities & statutory requirements – information of Government Regulations – Gomasta, Company formation – types, Startups, entrepreneurial decision process, business opportunities, preparing business plan & feasibility, financing.

Unit:3	Research Fundamentals, Research Problem and Design, Literature Review	8 Hours
---------------	--	----------------

Research Fundamentals: Definition, objectives, and significance of research, Types of research: Basic, Applied, Descriptive, Analytical, Quantitative, and Qualitative. Research Problem and Design: Criteria of good research, Techniques for defining and identifying a research problem, Features of good research problem/design, Necessity of defining the problem, Meaning of research design, Types of research design – Exploratory, Descriptive, Diagnostic, and Experimental Literature Review: Importance and methods of conducting a literature review, Sources of information: Journals, conferences, patents, etc., Technical reading strategies.

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

SoE No.
23VLSI-101

B.Tech in V.L.S.I.

Unit:4	Sampling and Data Collection, Data Analysis and Interpretation, Technical Writing, Research Ethics	7 Hours
Sampling and Data Collection: Sampling techniques: Probability and Non-probability sampling, Characteristics of a good sample, Sample size determination, Data types: Primary and Secondary, Methods of primary data collection: Observation, Interview, Questionnaire, Schedule, Secondary data sources Data Analysis and Interpretation: Processing and analyzing data, Statistical tools: Measures of central tendency, Dispersion, Correlation, Regression, Hypothesis testing: Null and alternative hypothesis, Type I and II errors, Use of software tools (e.g., Excel/SPSS/MATLAB for analysis), Interpretation of results Technical Writing, Research Ethics: Publication ethics and responsibilities of researchers, Structure and components of research report, Types of technical reports and papers, Writing thesis and dissertations, Referencing and citation styles (APA, IEEE, etc.), Ethical considerations in engineering research., Plagiarism and research ethics.		
Total Lecture Hours		30 Hours

Text books	
1	H. S. Fogler and S. E. LeBlanc, Strategies for Creative Problem Solving, 2nd edition, Pearson, Upper Saddle River, NJ, 2008.
2	Garg, B.L., Karadia, R., Agarwal, F. and Agarwal, U.K., 2002. An introduction to Research Methodology, RBSA Publishers.
3	Levine, Effective Problem Solving, 2nd edition, Prentice Hall, Upper Saddle River, NJ, 1994
Reference Books	
1	Activities for Teaching creativity and Problem Solving - By Arthur B Vangundy - Pfeiffer
2	Whimbey and J. Lochhead, Problem Solving & Comprehension, 6th edition, Lawrence Erlbaum, Mahwah, NJ, 1999.
3	Kothari, C.R., 1990. Research Methodology: Methods and Techniques. New Age International.
4	Sinha, S.C. and Dhiman, A.K., 2002. Research Methodology, Ess Ess Publications. 2 volumes.
5	Trochim, W.M.K., 2005. Research Methods: the concise knowledge base, Atomic Dog Publishing.
6	Wadehra, B.L. 2000. Law relating to patents, trademarks, copyright designs and geographical indications. Universal Law Publishing
7	Yousef Haik and Tamer M. Shahin, "Engineering Design Process", Cengage Learning, Second Edition, 2011.
8	Jeanne Liedtka (Author), Andrew King (Author), Kevin Bennett, "Solving Problems with Design

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

SoE No.
23VLSI-101

B.Tech in V.L.S.I.

	Thinking - Ten Stories of What Works” (Columbia Business School Publishing) Hardcover 2013
9	H. S. Fogler and S.E. LeBlanc, Strategies for Creative Problem Solving, Prentice Hall
10	E. Lumsdaine and M. Lumsdaine, Creative Problem Solving, McGraw Hill
11	J. Goldenberg and D. Mazursky, Creativity in product innovation. Cambridge University Press, 2002.
YCCE e- library book links [ACCESSIBLE FROM COLLEGE CAMPUS]	
1	http://103.152.199.179/YCCE/yccelibrary.html
MOOCs Links and additional reading, learning, video material	
1	www.nptelvideos.in
2	www.coursera.com
3	www.udemy.com
4	swayam.gov.in

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

B.Tech in V.L.S.I.

SoE No.
23VLSI-101

VI SEMESTER

23VLS1621 : PE-II : CMOS Subsystem Design

Course Outcomes:

Upon successful completion of the course the students will be able to

1. Understand VLSI circuit timing using Logical Effort analysis.
2. Analyze and calculate the signal delay introduced by the resistive and capacitive nature of interconnects in VLSI circuits.
3. Analyse and compute the power consumption of a VLSI circuit. .
4. Design fundamental digital VLSI subsystems like adders, memory structures

Unit:1	Wires and Interconnect: Resistance, Capacitance, RC delay analysis, Crosstalk delay and noise effects, Repeaters, Logical Effort, Crosstalk control, reliability.	8 Hours
---------------	--	----------------

Unit:2	Synchronizers; Arbiters; Clock Synthesis; PLLs; Clock generation; Clock distribution; Synchronous Vs Asynchronous design, introduction to pipelined system/ALU.	8 Hours
---------------	---	----------------

Unit:3	Datapath Subsystems : Adders: Full Adder using a variety of Logics styles, bit-serial Adder, Ripple Carry Adder, Carry-skip Adder, Carry Look-ahead Adder, Brent-Kung Adder, Kogge-Stone Adder, Carry-Save Adder (multi-operand addition), etc. with power and speed trade-off	7 Hours
---------------	---	----------------

Unit:4	Datapath Subsystems : Multipliers: Unsigned Array Multiplier, Booth Encoded Multiplier, Baugh-Wooley Multiplier, Wallace tree multiplier, etc. , comparators, shifter-registers, random number generator based on Linear Feedback Shift-Registers (LFSR).	8 Hours
---------------	--	----------------

Unit:5	Memory Array Subsystems : Register-file, Content-addressable memory, LIFO and FIFO DRAM,ROM,SRAM design, Reliability; Power dissipation in Memories	8 Hours
---------------	--	----------------

Unit :6	Special-purpose Subsystems: Packaging; power distribution; I/O pads, Emerging topics in VLSI.	7 Hours
----------------	--	----------------

Total Lecture Hours	45 Hours
----------------------------	-----------------

			July,2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

B.Tech in V.L.S.I.

SoE No.
23VLSI-101

Text books

- | | |
|---|---|
| 1 | Neil H. E. WesteHarris, Principle of CMOS VLSI Design, 4th Edition, Addison Wesley VLSI Series. |
|---|---|

Reference Books




- | | |
|---|--|
| 1 | John P. Uyemura, Introduction to VLSI Circuits and Systems, Students Edition, Wiley Publication. |
| 2 | Sung-Mo Kang, Yusuf leblebici, CMOS VLSI Design, Third edition, 2008, TataMcGraw Hill. |

YCCE e- library book links [ACCESSIBLE FROM COLLEGE CAMPUS]

- | | |
|---|---|
| 1 | http://103.152.199.179/YCCE/yccelibrary.html |
|---|---|

MOOCs Links and additional reading, learning, video material

- | | |
|---|---|
| 1 | https://nptel.ac.in/courses/108107129 |
| 2 | https://nptel.ac.in/courses/106103116 |
| 3 | https://nptel.ac.in/courses/117106092 |

			July,2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

B.Tech in V.L.S.I.

SoE No.
23VLSI-101

VI SEMESTER

23VLS1622 : PE-II : Lab. CMOS Subsystem Design

Course Outcomes:

Upon successful completion of the course the students will be able to

1. Understand VLSI circuit timing using Logical Effort analysis.
2. Design elementary data path subsystems like adder and subtractors.
3. Design elementary data path subsystems like Multiplier and comparators
4. Analyse and compute the power consumption of a VLSI circuit.
5. Analyse and compute hands-on experience with industry-standard CAD tools for simulation, and verification of CMOS circuits

Sr. No.	Experiments based on
1	Design 3 bit oscillator using CMOS inverter
2	Implement $f = \text{not}((a+b)(c+d))$ using nand gate
3	Design and simulate a CMOS Ripple Carry Adder .
4	Design and simulate a CMOS Carry-skip Adder
5	Design and simulate a CMOS Carry Look-ahead Adder
6	Design 2 bit comparator using basic cmos gates
7	Design and simulate 8 to 1 Multiplexer using 2 to 1 Mux
8	Design Binary multiplier using basic gates
9	Design and simulate Ring counter
10	Mini Project

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

SoE No.
23VLSI-101

B.Tech in V.L.S.I.

VI SEMESTER

23VLS1623 : PE II: Synthesis & Optimisation of VLSI Circuits

Course Outcomes:

Upon successful completion of the course the students will be able to

1. Understand the concept of microelectronics, its designs and graph theory.
2. Understand and apply the Boolean algebra concepts with the help of hardware descriptive language.
3. Apply and analyse two level logic optimization techniques, multilevel logic optimization, and sequential logic optimization.
4. Understand and apply the concepts of scheduling.
5. Apply optimization techniques on the digital concepts.

Unit:1	Introduction to Microelectronics	7 Hours
Microelectronics, Semiconductor technologies and circuit taxonomy, Microelectronic design styles, Design of Microelectronic circuits, Computer aided synthesis and optimization. Graphs Notation, Undirected graphs, Directed graphs.		
Unit:2	Hardware Modelling	8 Hours
Boolean algebra and Applications, Hardware Modelling Languages, Distinctive features, Structural hardware language, Behavioral hardware language, HDLs used in synthesis, Abstract models, Structures logic networks, State diagrams, Data flow and sequencing graphs, Compilation and optimization techniques.		
Unit:3	Scheduling Algorithms	7 Hours
A model for scheduling problems, Scheduling without resources constraints, Scheduling with resources constraint, Scheduling algorithms for extended sequencing models, Scheduling pipelined circuits.		
Unit:4	Logic level synthesis and optimization	8 Hours
Logic optimization principles, Operation on two level logic covers, Algorithms for logic minimization, Symbolic minimization and encoding problems, Minimization of Boolean relations.		
Unit:5	Multiple-level combinational logic optimization	8 Hours
Multiple level combinational logic optimizations, Models and transformations Combinational networks, Algebraic model, Synthesis of testable network, Algorithm for delay evaluation and optimization.		
Unit :6	Sequential Logic optimization	7 Hours
Introduction, Sequential circuit optimization using state-based models, Sequential circuit optimization using network models, Cell library binding, Specific problems and algorithms for library binding (lookup table F.P.G.As and Antifuse based F.P.G.As)		
Total Lecture Hours		45 Hours

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

B.Tech in V.L.S.I.

SoE No.
23VLSI-101

Text books

- | | |
|---|---|
| 1 | "Synthesis and Optimization of Digital Circuits", Giovanni De Micheli, 1st Edition, Tata McGraw-Hill, 2003. |
|---|---|

Reference Books




- | | |
|---|---|
| 1 | "Logic Synthesis" SrinivasDevadas, AbhijitGhosh, and Kurt Keutzer, 1st Edition, McGraw-Hill, USA, 1994. |
| 2 | "VHDL for Programmable Logic," Kevin Skahill, 1st Edition, Pearson Education, 2000. |

YCCE e- library book links [ACCESSIBLE FROM COLLEGE CAMPUS]

- | | |
|---|---|
| 1 | http://103.152.199.179/YCCE/yccelibrary.html |
|---|---|

MOOCs Links and additional reading, learning, video material

- | | |
|---|---|
| 1 | https://nptel.ac.in/courses/108103108 |
| 2 | https://archive.nptel.ac.in/noc/courses/noc18/SEM1/noc18-ec06/ |
| 3 | https://archive.nptel.ac.in/courses/108/103/108103108/ |
| 4 | https://onlinecourses.nptel.ac.in/noc22_cs109/preview |

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

B.Tech in V.L.S.I.

SoE No.
23VLSI-101

VI SEMESTER

23VLS1624 : PE II: Lab. Synthesis & Optimisation of VLSI Circuits

Course Outcomes:

Upon successful completion of the course the students will be able to

1. Understand the concept of microelectronics, its designs and graph theory.
2. Understand and apply the Boolean algebra concepts with the help of hardware descriptive language.
3. Apply and analyse two level logic optimization techniques, multilevel logic optimization, and sequential logic optimization.
4. Understand and apply the concepts of scheduling.
5. Apply optimization techniques on the digital concepts.

Sr. No.	Experiments based on
1	Write HDL Codes of basic gates.
2	Write HDL Codes of half adder and full adder.
3	Write HDL Codes of half and full subtractor.
4	Implementation and synthesis of multiplexers.
5	Implementation and synthesis of demultiplexers.
6	Implementation and synthesis of decoders.
7	Implementation and synthesis of Flip-flops.
8	Implementation and synthesis of latches.
9	Implementation and synthesis of registers.
10	Implementation and synthesis of flip flops.

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

SoE No.
23VLSI-101

B.Tech in V.L.S.I.

VI SEMESTER

23VLS1625 : PEII: Quantum Computing

Course Outcomes:

Upon successful completion of the course the students will be able to

1. Understand the basic concepts of Quantum Mechanics
2. Understand and analyze logic gates with Quantum mechanism
3. Understand and analyze Quantum Computing Algorithms
4. Understand and analyze Quantum Computing Applications

Unit:1	Introduction to Quantum Mechanics:	8 Hours
Basic principles of quantum mechanics, Wave-particle duality, Superposition and measurement, Quantum gates and operators		
Unit:2	Qubits and Quantum Gates:	8 Hours
Quantum bit (qubit) representation, Quantum gates (e.g., Pauli gates, Hadamard gate, CNOT gate), Quantum circuits and circuit diagrams, Single-qubit and multi-qubit operations		
Unit:3	Quantum Algorithms:	7 Hours
Quantum parallelism and superposition, Quantum Fourier transform, Quantum search algorithms (e.g., Grover's algorithm), Shor's algorithm for prime factorization		
Unit:4	Quantum Error Correction and Noise:	8 Hours
Sources of noise and errors in quantum systems, Quantum error correction codes, Error mitigation techniques		
Unit:5	Quantum Applications:	8 Hours
Quantum simulation, Quantum cryptography, Quantum machine learning Quantum optimization		
Unit :6	Quantum Hardware:	7 Hours
Physical implementation of qubits (e.g., superconducting qubits, trapped ions, topological qubits), Quantum circuit design and optimization, Challenges and advancements in quantum hardware development.		
Total Lecture Hours		45 Hours

Text books

1	"Quantum Computation and Quantum Information" by Michael Nielsen and Isaac Chuang
2	"Quantum Computing for Computer Scientists" by Noson S. Yanofsky and Mirco A. Mannucci
3	"Quantum Computing: A Gentle Introduction" by Eleanor Rieffel and Wolfgang Polak

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

B.Tech in V.L.S.I.

SoE No.
23VLSI-101

Reference Books

1 "Quantum Computing since Democritus" by Scott Aaronson

YCCE e- library book links [ACCESSIBLE FROM COLLEGE CAMPUS]

1 <http://103.152.199.179/YCCE/yccelibrary.html>

MOOCs Links and additional reading, learning, video material

1 "Quantum Computing for Everyone" by Chris Bernhardt and "Quantum Mechanics for Scientists and Engineers" by Stanford University.

2 "Quantum Mechanics and Quantum Computation" by MIT, and "Quantum Cryptography" by Delft University of Technology.

3 "Introduction to Quantum Computing" IBM Quantum.

4 "Quantum Computing for Business" and "Discovering Quantum Mechanics and Quantum Computing" by the University of Glasgow.

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's
Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

B.Tech in V.L.S.I.

SoE No.
23VLSI-101

VI SEMESTER

23VLS1626 : PEII: Lab. Quantum Computing

Course Outcomes:

Upon successful completion of the course the students will be able to

1. Understand the basic concepts of Quantum Mechanics
2. Understand and analyze logic gates with Quantum mechanism
3. Understand and analyze Quantum Computing Algorithms
4. Understand and analyze Quantum Computing Applications

Sr. No.	Experiments based on
1	To implement NOT gate with quantum bits.
2	To implement quantum basic gates using quantum bits.
3	To implement NAND gate using quantum bits.
4	To implement NOR gate using quantum bits.
5	Design Half Adder using quantum bits.
6	Design Full Adder using quantum bits.
7	Design 2:1 Multiplexer using quantum bits.
8	Design 4:1 Multiplexer using quantum bits.
9	Design 2:4 Decoder using quantum bits.
10	Design Encoder using quantum bits.

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

B.Tech in V.L.S.I.

SoE No.
23VLSI-101

VI SEMESTER **23VLS1641 : PE-III : Analog VLSI Design**

Course Outcomes:

Upon successful completion of the course the students will be able to

1. Understand and explain concepts related to MOSFET
2. Apply the knowledge of circuit analysis models in analysis of analog VLSI circuit
3. Analyze given analog VLSI circuit to arrive at a suitable conclusion
4. Design analog VLSI circuit for given application and specifications
5. Design and conduct experiment using analog VLSI circuit for given application and specifications

Unit:1	Basic MOS Device Physics:	8 Hours
Threshold voltage, Derivation of I/V characteristics, second order effects, MOS device capacitance, MOS small signal models, MOS SPICE models.		
Unit:2	Single stage amplifiers:	7 Hours
Basic concept, common source, common source stage with resistive load, CS stage with source degeneration, source follower, common gate.		
Unit:3	Differential amplifiers:	8 Hours
Single ended & differential operation, Basic differential pair, qualitative and quantitative analysis, Common mode response		
Unit:4	Passive and active current mirrors:	7 Hours
Basic current mirror, Cascode current mirror, Active current mirror, common mode properties		
Unit:5	frequency response of amplifiers:	8 Hours
Miller effect, association of poles with node, common source stage, source follower, common gate stage		
Unit :6	Operational amplifiers:	7 Hours
Performance parameters, one stage op amp, Two stage op amp, Gain boosting, Noise in op amp		
Total Lecture Hours		45 Hours

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

B.Tech in V.L.S.I.

SoE No.
23VLSI-101

Textbooks	
1	Design of Analog CMOS Integrated circuits, Behzad Razavi Mc-graw-Hill Ninteenth reprint 2010
Reference Books	
1	CMOS circuit design, layout, and Simulation' Second edition, reprint 2009. Jacob Baker WSE
2	CMOS Analog Circuit Design second edition, 2010 P.E.Allen, D.R.Holdberg Oxford univ. press
3	Analysis and Design of Analog Integrated Circuits fifth edition, reprint 2010 Paul B Gray , Hurst , Lewis, Meyer John Wiley & sons
YCCE e- library book links [ACCESSIBLE FROM COLLEGE CAMPUS]	
1	http://103.152.199.179/YCCE/yccelibrary.html
MOOCs Links and additional reading, learning, video material	
1	https://archive.nptel.ac.in/courses/108/105/108105158/

			July,2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

B.Tech in V.L.S.I.

SoE No.
23VLSI-101

VI SEMESTER

23VLS1642 : PE-III Lab:- Analog VLSI Design

Course Outcomes:

Upon successful completion of the course the students will be able to

1. Understand and explain concepts related to MOSFET
2. Apply the knowledge of circuit analysis models in analysis of analog VLSI circuit
3. Analyze given analog VLSI circuit to arrive at a suitable conclusion
4. Design analog VLSI circuit for given application and specifications
5. Design and conduct experiment using analog VLSI circuit for given application and specifications

Sr. No.	Experiments based on
1	NMOS characteristic :- V_{ds} Vs I_D for various values of V_{gs} .
2	PMOS characteristic :- V_{ds} Vs I_D for various values of V_{gs} .
3	Current source using current mirror :- DC analysis
4	Common Source amplifier:- AC analysis Transient analysis
5	Common Drain amplifier:- AC analysis Transient analysis
6	Differential Amplifier :- AC analysis Transfer curve (V_{in} Vs V_{out} , DC condition)
7	Op-Amp Design: AC analysis Transient analysis DC analysis
8	Basic CMOS Comparator Design
9	Source Coupled Pair Differential Amplifier
10	Mini Project

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

B.Tech in V.L.S.I.

SoE No.
23VLSI-101

VI SEMESTER

23VLS1643 : PE-III : FPGA-Based System Design

Course Outcomes:

Upon successful completion of the course the students will be able to

CO1:Analyze the architecture of Field-Programmable Gate Arrays (FPGAs)

CO2:Demonstrate proficiency in the FPGA design flow

CO3:Design and implement combinational and sequential digital circuits

CO4:Apply FPGA design principles to develop solutions for specific application domains

Unit:1	Overview of FPGA Architectures	7 Hours
--------	--------------------------------	---------

Introduction to programmable logic devices (PLDs, CPLDs, FPGAs), FPGA architecture (CLBs, interconnects, I/O blocks), FPGA design flow, Overview of FPGA development tools.

Unit:2	FPGA Design and Implementation	8 Hours
--------	--------------------------------	---------

FPGA design methodologies, Synthesis, place and route, and bitstream generation, Timing analysis and optimization, Resource utilization and power consumption, Memory interfacing (SRAM, DRAM), High-speed I/O interfaces (e.g., PCIe, Ethernet), Embedded processors on FPGAs (e.g., MicroBlaze, NIOS II).

Unit:3	Verilog Modelling of Combinational Circuits	7 Hours
--------	---	---------

Behavioral, Data Flow, Structural Realization of Adders, High Speed Adders, Carry look-ahead adder, Carry save adders, Multipliers, Sequential and Parallel Multipliers, Comparators, code converters

Unit:4	Verilog Modelling of Sequential Circuits	8 Hours
--------	--	---------

Flip Flops, Realization of Shift Register, Realization of a Counter- Synchronous and Asynchronous, FIFO, Single port and Dual port RAM, LFSR

Unit:5	Synchronous Sequential Circuit	7 Hours
--------	--------------------------------	---------

Mealy and Moore state machines, Design of serial adder using Mealy and Moore state machines, Sequence detection, Design examples




Unit :6	FPGA System Design Project and Advanced Topics	8 Hours
---------	--	---------

System Specification, Architecture, Implementation and Testing, Design Methodologies Design Example for Large Scale Systems, Advanced FPGA Topics.

Total Lecture Hours	45 Hours
---------------------	----------

Text books

1	Wayne Wolf, "FPGA-Based System Design," with CD-ROM, 2004, Prentice Hall, ISBN: 0131424610.
---	---

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

SoE No.
23VLSI-101

B.Tech in V.L.S.I.

Reference Books




1	Samir Palnitkar, "Verilog HDL," Second Edition, 2003, Prentice Hall, ISBN: 0130449113
2	Pong P. Chu, "FPGA Prototyping by Verilog Examples: Xilinx Spartan-3," Wiley-Interscience, 1st Edition, 2008, ISBN-10: 0470185325.
	Steven Kilts, "Advanced FPGA Design: Architecture, Implementation and Optimization" Wiley-IEEE Press, 1st Edition, 2007, ISBN:0470054379

YCCE e- library book links [ACCESSIBLE FROM COLLEGE CAMPUS]

1	http://103.152.199.179/YCCE/yccelibrary.html
---	---

MOOCs Links and additional reading, learning, video material

1	https://archive.nptel.ac.in/courses/117/108/117108040/
2	https://elearn.nptel.ac.in/shop/nptel/workshop-on-fpga-architecture-and-programming-using-verilog-hdl/?v=c86ee0d9d7ed

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

B.Tech in V.L.S.I.

SoE No.
23VLSI-101

VI SEMESTER

23VLS1644 : PE-III : Lab. FPGA-Based System Design

Course Outcomes:

Upon successful completion of the course the students will be able to

CO1: Design and implement combinational and sequential digital circuits using Hardware Description Languages (HDL) using industry-standard tools such as Vivado and Quartus Prime

CO2: Develop and optimize digital systems using FPGA design tools and workflows, including synthesis, placement, routing, and timing analysis

CO3: Design and test FPGA-based systems for real-world applications, ensuring functionality and performance.

CO4: Demonstrate proficiency in debugging and verifying FPGA designs using simulation and hardware debugging techniques.

Sr. No.	Experiments based on
1	FPGA Tools & Simulation: Setup, basic HDL simulation.
2	Design and Implementation of High Speed Adders
3	Design and Implementation of Multipliers
4	Design and Implementation of Comparators
5	Design and Implementation of Code Converters
6	Design and Implementation of Parity Checkers
7	Design and Implementation of Flip Flops
8	Design and Implementation of Counters
9	Design and Implementation of Shift Register
10	Design and Implementation of State Machines
11	Mini project

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

B.Tech in V.L.S.I.

SoE No.
23VLSI-101

VI SEMESTER 23VLSI645 : PE-III : System C

Course Outcomes:

Upon successful completion of the course the students will be able to

1. Understand the fundamentals of SystemC
2. Design and analyze transaction-level models
3. Simulate and debug SystemC designs
4. Apply SystemC in system design problems
5. Evaluate and optimize performance of SystemC models

Unit:1	Introduction	8 Hours
What is System C, Why System C, Design Methodology, Capabilities, System C RTL		
Unit:2	Data Types	8 Hours
Value Holders, Summary of Types, Bit Types, Arbitrary Width Bit Type, Logic Type, Arbitrary Width Logic Type, Signed and Unsigned Integer type, User Defined Data Type, Recommended Data Type.		
Unit:3	Modelling Combinational Logic	7 Hours
File Structure, Reading and writing ports and signals, Logic Operators, Arithmetic Operators (Unsigned and signed), Relational Operators, Vectors and Ranges, If Statements, Switch Statements, Loops, Methods, Structures, Multiple Processes and delta Delays.		
Unit:4	Modelling Synchronous Logics	8 Hours
Modelling Flip-Flops, Multiple Processes, Flip-flop with Asynchronous Preset and clear, Flip-flop with Synchronous Preset and clear, Multiple and Multi-phase Clocks, Modeling Latches.		
Unit:5	Miscellaneous Logic	8 Hours
Three state Drivers, Multiple Drivers, handling Don't Cares, hierarchy, Parameterizing Modules, Variable and Signal Assignments.		
Unit :6	Modeling Examples	7 Hours
A memory Model, Modeling and FSM, Universal Shift Register, Counters, A factorial Model.		
Total Lecture Hours		46 Hours

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

B.Tech in V.L.S.I.

SoE No.
23VLSI-101

Textbooks

1 System C Primer, J. Bhasker, 2nd Edition (Updated with TLM concepts)

Reference Books

1 **SystemC: System Design with SystemC, Frank Ghenassia**

2 The SystemC Language Reference Manual (IEEE 1666)

3 Modeling Embedded Systems and SoC's with SystemC and TLM 2.0, Francky Catthoor, Dirk Verkest

YCCE e- library book links [ACCESSIBLE FROM COLLEGE CAMPUS]

1 <http://103.152.199.179/YCCE/yccelibrary.html>

MOOCs Links and additional reading, learning, video material

1 <https://archive.nptel.ac.in/courses/117/106/117106112/>

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

B.Tech in V.L.S.I.

SoE No.
23VLSI-101

VI SEMESTER **23VLSI1646 : PE-III : Lab. System C**

Course Outcomes:

Upon successful completion of the course the students will be able to

1. Develop and simulate basic digital components using SystemC.
2. Design structural and behavioral models of digital systems using SystemC modules and processes.
3. Implement and simulate synchronous and asynchronous circuits using SystemC constructs.
4. Build and verify simple hardware subsystems using transaction-level modeling

Sr. No.	Experiments based on
1	Lab 1: SystemC Installation and Setup “Install and configure SystemC on Linux/Windows.”
2	Lab 2: Basic Module and Process Modeling “Understand SC_MODULE, SC_METHOD, SC_THREAD.”
3	Lab 3: Data Types and Ports “Use SystemC-specific data types and ports.”
4	Lab 4: Clock and Reset Implementation “Generate and use clock/reset signals in SystemC.”
5	Lab 5: ALU Design in SystemC “Implement a 4-bit ALU using SystemC.”
6	Lab 6: FSM (Finite State Machine) Modeling “Design and simulate a FSM (e.g., traffic light controller).”
7	Lab 7: Memory Modeling “Simulate a RAM/ROM block in SystemC.”
8	Lab 8: Testbench Creation “Design a basic testbench for verification.”
9	Lab 9: Counter Design (Synchronous/Asynchronous) “Implement 4-bit up/down counters.”
10	Lab 10: Transaction-Level Modeling (TLM) Introduction “Understand TLM 2.0 basics.”

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Yeshwantrao Chavan College of Engineering

Nagar Yuwak Shikshan Sanstha's
(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

SoE No.
23VLSI-101

B.Tech in V.L.S.I.

VI SEMESTER MDM4VLSI04 : Digital System Design

Course Outcomes:

Upon successful completion of the course the students will be able to

1. **Understand** hardware description language and able to design and simulate digital systems using different abstraction levels.
2. **Apply and design** combinational and sequential logic circuits.
3. **Apply and design** the basics of synchronous sequential logic and finite state machines.
4. **Analyze** building blocks in digital system and explain the programmable devices and able to design digital systems using modern design tools.

Unit:1	Introduction to Verilog	8 hrs
HDL Based Design flow, Requirements of HDL, Design Methodologies, Different Modelling styles, Introduction to Verilog, Elements of Verilog, Verilog Module definition, Elements of Module, Basic Concepts in Verilog, Reserved Keywords, Syntax & Semantics, Comments, Identifiers, Number Representation, System Representation, Verilog Ports, Verilog Data Types, Wire & Variables, Physical & Abstract, Constants, Parameter, Verilog Data Operators.		
Unit:2	Data Flow Modelling	7hrs
Data Flow Modelling, Delay, Continuous Assignment, Delayed Continuous assignment Design entry in Verilog & Test bench, Combinational blocks design, Compilation and synthesis, Timing analysis resolving signal values		
Unit:3	Structural Modelling	8 hrs
Structural Modelling Feature, Module Instantiation, Gate level Primitives, Gate Delays, Switch Level Primitives, User Defined Primitives.		
Unit:4	Behavioural Modelling	7hrs
Behavioural Modelling, Initial, Always, Procedural Assignment, Blocking and Non- Blocking assignments, Sequential & Parallel Blocks, Race around Condition, Timing Control, Procedural Statements, Conditional Statements if case loop repeat forever etc, Zero Delay Control, Event Based Timing Control, Compiler Directives, Assign Design, Force Release, Latch Models, FF Models, State Machine Coding, Moore and Mealy Machines.		
Unit:5	Combinational & sequential system Design	8 hrs
Combinational & sequential system Design examples like Shift Registers, Counters, LFSR, Stacks and Queues, Multi bit Adders & Multiplier, Huffman Coding, Processor and Memory Model, CPU, System Tasks and Functions, Design Verification.		

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

B.Tech in V.L.S.I.

SoE No.
23VLSI-101

Unit :6	Digital Design Fundamentals	7 hrs
Digital Design Fundamentals, Combinational & Sequential design issues, Introduction to finite state machines, Moore & Mealy Machine, Introduction to programmable devices, PLA, PAL, PROM, Structure of CPLDs, Introduction to FPGA, Architecture, CLB, IOB, Programmable Interconnect Points, Different type of programmable switches used in PLDs.		
Total Lecture Hours		45 hrs

Textbooks	
1	Samir Palnitkar , Verilog HDL: A Guide to Digital Design and Synthesis, 2 nd Edition,2003,Prentice Hall
Reference Books	
1	Zainalabedin Navabi , Verilog Digital System Design, Second Edition ,Tata McGraw Hill,2009.
YCCE e- library book links [ACCESSIBLE FROM COLLEGE CAMPUS]	
1	http://103.152.199.179/YCCE/yccelibrary.html .
MOOCs Links and additional reading, learning, video material	
1	https://onlinecourses.nptel.ac.in/noc20_cs63/
2	

			July,2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)

B.Tech in V.L.S.I.

SoE No.
23VLSI-101

VI SEMESTER

23VLS1605 : Lab:- Electronics Design Automation

Course Outcomes:

Upon successful completion of the course the students will be able to

1. Implement finite state machine-based logic for traffic control using LEDs and microcontroller programming.
2. Develop a real-time monitoring system integrating multiple sensors and actuators
3. Design and implement a multi-component embedded system capable of real-time data acquisition, processing, and actuator control.
4. Innovate and prototype a domain-specific embedded solution using the STM32 Blue Pill to solve real-world problems.

MSPA-1 Activity

Traffic Light Control Logic:

- Implement a state machine to control Red, Yellow, and Green LEDs for four lanes.
- Typical cycle for each lane:
 - Green: 10 seconds
 - Yellow: 3 seconds
 - Red: 10 seconds
- Only one lane should have a Green light at any given time.

MSPA-2 Activity

Design and implement a real-time monitoring system using the STM32 Blue Pill that interfaces with at least two sensors, controls three LEDs, and optionally displays sensor data on an LCD or OLED display.

MSPA-3 Activity

Design and develop an embedded system using the **STM32 Bluepill board** that integrates a **display, two sensors, and an actuator**. The system should demonstrate real-time data acquisition, processing, and control, ensuring efficient communication between components.

MSPA-4 Activity

Conceptualize and design an innovative embedded system project using the **STM32 Blue Pill** microcontroller. The project should address a real-world problem in any of the following domains:

- IoT (Internet of Things)
- Automation & Control
- Wearable Technology
- Smart Agriculture
- Health Monitoring
- Security & Surveillance
- Communication Systems

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	



Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

B. Tech SoE and Syllabus 2023
(Scheme of Examination w.e.f. 2023-24 onward)
(Department of Electronics Engineering)




B.Tech in V.L.S.I.

SoE No.
23VLSI-101

VI SEMESTER

Mandatory Learning Course (MLC)

MLC2126 : YCAP6

			July, 2023	1.00	Applicable for AY 2023-24 Onwards
Chairperson	Dean (Acad. Matters)	Dean OBE	Date of Release	Version	