Engineering Notebook

VOLUME 1

EE2201 Electronic Devices

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Unit 1
Energy Bands and charge carriers in semiconductors

Que: 1 *Calculate the intrinsic carrier concentration in silicon at T = 300 K.*

Answer: For silicon at T = 300 K, we can write

$$n_i = BT^{3/2}e^{\left(\frac{-E_g}{2kT}\right)}$$

$$= (5.23 \times 10^{15})(300)^{3/2}e^{\left(\frac{-1.1}{2(86\times10^{-6})(300)}\right)}$$

$$n_i = 1.5 \times 10^{10}\text{cm}^{-3}$$

An intrinsic electron concentration of 1.5×10^{10} cm^{-3} may appear to be large, but it is relatively small compared to the concentration of silicon atoms, which is 5×10^{22} cm^{-3}.

Que: 2*- Calculate the thermal equilibrium electron and hole concentrations.*

(a) *Consider silicon at T = 300 K doped with phosphorus at a concentration of $N_d = 10^{16}$ cm^{-3}, $n_i = 1.5 \times 10^{10}$ cm^{-3} .*

Answer: Since Nd >>ni , the electron concentration is

$$n_o \cong N_d = 10^{16}\,\text{cm}^{-3}$$

and the hole concentration is

$$p_o = \frac{n_i^2}{N_d} = \frac{(1.5 \times 10^{10})^2}{10^{16}} = 2.25 \times 10^4\,\text{cm}^{-3}$$

Que: 2- (b) *Consider silicon at T = 300 K doped with boron at a concentration of Na = 5×10^{16} cm^{-3}.*

Answer: Since Na >>ni , the hole concentration is

$$p_o \cong N_a = 5 \times 10^{16}\,\text{cm}^{-3}$$

and the electron concentration is

$$n_o = \frac{n_i^2}{N_a} = \frac{(1.5 \times 10^{10})^2}{5 \times 10^{16}} = 4.5 \times 10^3\,\text{cm}^{-3}$$

Que: 3*- Calculate the drift current density for a given semiconductor. Consider silicon at T = 300 K doped with arsenic atoms at a concentration of Nd = 8×10^{15} cm^{-3}. Assume mobility values of μn = 1350 cm^2/V–s and μp = 480 cm^2/V–s. Assume the applied electric field is 100 V/cm.*

Solution: The electron and hole concentrations are

$$n \cong N_d = 8 \times 10^{15}\,\text{cm}^{-3}$$

And

$$p = \frac{n_i^2}{N_d} = \frac{(1.5 \times 10^{10})^2}{8 \times 10^{15}} = 2.81 \times 10^4\,\text{cm}^{-3}$$

Because of the difference in magnitudes between the two concentrations, the conductivity
is given by

$$\sigma = e\mu_n n + e\mu_p p \cong e\mu_n n$$

or

$$\sigma = (1.6 \times 10^{-19})(1350)(8 \times 10^{15}) = 1.73(\Omega\text{–cm})^{-1}$$

The drift current density is then

$$J = \sigma E = (1.73)(100) = 173\,\text{A/cm}^2$$

Que: 4*- Calculate the diffusion current density for a given semiconductor. Consider silicon at T = 300 K. Assume the electron concentration varies linearly from n = 10^{12} cm^{-3} to n = 10^{16} cm^{-3} over the distance from x = 0 to x = 3 μm. Assume Dn = 35 cm^2/s.*

Solution: We have

$$J_n = eD_n\frac{dn}{dx} = eD_n\frac{\Delta n}{\Delta x} = (1.6 \times 10^{-19})(35)\left(\frac{10^{12} - 10^{16}}{0 - 3 \times 10^{-4}}\right)$$

or

Jn = 187 A/cm2

Unsolved 1: *Consider n-type GaAs at T = 300 K doped to a concentration of Nd = 2 × 10^{16} cm^{-3} . Assume mobility values of μn = 6800 $cm^2/V–s$ and μp = 300 $cm^2/V–s$. (a) Determine the resistivity of the material. (b) Determine the applied electric field that will induce a drift current density of 175 A/cm2.*
(**Ans**. (a) 0.0460 Ω–cm, (b) 8.04 V/cm).

Unsolved 2: *Consider silicon at T = 300 K. Assume the hole concentration is given by p = 1016e−x/Lp (cm−3), where Lp = 10−3 cm. Calculate the hole diffusion current density at (a) x = 0 and (b) x = 10−3cm. Assume Dp = 10 cm2/s.*
(**Ans.** (a) 16 A/cm2, (b) 5.89 A/cm2)

Unsolved 3: *The electron and hole diffusion coefficients in silicon are Dn = 35 cm2/s and Dp = 12.5 cm2/s, respectively. Calculate the electron and hole*

diffusion current densities (a) if an electron concentration varies linearly from n = 1015 cm−3 to n = 1016 cm−3 over the distance from x = 0 to x = 2.5 μm and (b) if a hole concentration varies linearly from p = 10^{14} cm−3 to p = 5 × 10^{15} cm−3 over the distance from x = 0 to x = 4.0 μm.
(**Ans**. (a) Jn = 202 A/cm^2, (b) Jp = −24.5 A/cm^2)

Unsolved 4: *A sample of silicon at T = 300 K is doped to N_d = 8 × 10^{15} cm^{-3}. (a) Calculate no and po. (b) If excess holes and electrons are generated such that their respective concentrations are _n = _p = 10^{14} cm^{-3} , determine the total concentrations of holes and electrons.*
(**Ans**. (a) no = 8 × 10^{15} cm^{-3} , po = 2.81 × 10^4 cm−3 ; (b) n = 8.1 × 10^{15} cm^{-3} , p = 10^{14} cm^{-3})

Que: 5 *Describe the concepts of drift current and diffusion current in a semiconductor material.*

Answer: Drift and Diffusion Currents

The creation of negatively charged electrons and positively charged holes in the semiconductor. If these charged particles move, a current is generated. These charged electrons and holes are simply referred to as **carriers.**

The two basic processes which cause electrons and holes to move in a semiconductor
are:

(a) **drift,** which is the movement caused by electric fields, and

(b) **diffusion,** which is the flow caused by variations in the concentration, that is, concentration gradients.
Such gradients can be caused by a non homogeneous doping distribution, or by the injection of a quantity of electrons or holes into a region.

Drift Current Density

Assume an electric field is applied to a semiconductor. The field produces a force that acts on free electrons and holes, which then experience a net drift velocity and net movement. Consider an n-type semiconductor with a large number of free electrons shown in figure. An electric field *E* applied in one direction produces a force on the electrons in the *opposite* direction, because of the electrons' negative charge. The electrons acquire a drift velocity v*dn* (in cm/s) which can be written as

$$v_{dn} = -\mu_n E$$

where μ*n* is a constant called the **electron mobility** and has units of cm2/V–s. For low-doped silicon, the value of μ*n* is typically 1350 cm2/V–s. The mobility can be thought of as a parameter indicating how well an electron can move in a semiconductor. The negative sign in above equation indicates that the electron drift velocity is opposite to that of the applied electric field as shown in Figure The electron drift produces a drift current density *Jn* (A/cm2) given by

$$J_n = -env_{dn} = -en(-\mu_n E) = +en\mu_n E$$

where *n* is the electron concentration (#/cm3) and *e*, in this context, is the magnitude of the electronic charge. The conventional drift current is in the opposite direction from the flow of negative charge, which means that the drift current in an n-type semiconductor is in the same direction as the applied electric field.

Next consider a p-type semiconductor with a large number of holes. An electric field *E* applied in one direction produces a force on the holes in the *same* direction, because of the positive charge on the holes. The holes acquire a drift velocity v*dp* (in cm/s), which can be written as

$$v_{dp} = +\mu_p E$$

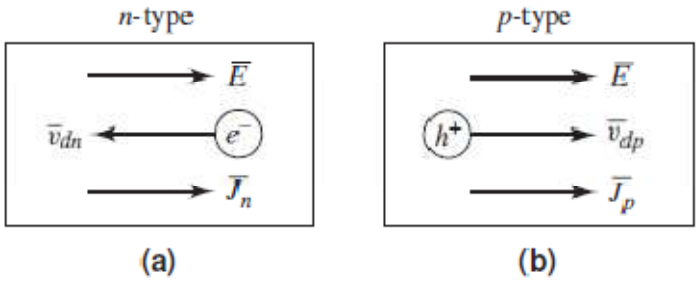


Figure Directions of applied electric field and resulting carrier drift velocity and drift current density in (a) an n-type semiconductor and (b) a p-type semiconductor where μ*p* is a constant called the **hole mobility,** and again has units of cm2/V–s. For low-doped silicon, the value of μ*p* is typically 480 cm2/V–s, which is less than half the value of the electron mobility. The positive sign in Equation indicates that the hole drift velocity is in the same direction as the applied electric field as shown in Figure. The hole drift produces a drift current density *Jp* (A/cm2) given by

$$J_p = +epv_{dp} = +ep(+\mu_p E) = +ep\mu_p E$$

where *p* is the hole concentration (#/cm3) and *e* is again the magnitude of the electronic charge. The conventional drift current is in the same direction as the flow of positive charge, which means that the drift current in a p-type material is also in the same direction as the applied electric field.

Since a semiconductor contains both electrons and holes, the total drift current density is the sum of the electron and hole components. The total drift current density is then written as

$$J = en\mu_n E + ep\mu_p E = \sigma E = \frac{1}{\rho} E$$

Where

$$\sigma = en\mu_n + ep\mu_p$$

and where ρ is the **conductivity** of the semiconductor in (Ω–cm)−1 and where ρ= 1/σ is the **resistivity** of the semiconductor in (Ω–cm). The conductivity is related to the concentration of electrons and holes. If the electric field is the result of applying a voltage to the semiconductor, then Equation becomes a

linear relationship between current and voltage and is one form of Ohm's law. From Equation,we see that the conductivity can be changed from strongly n-type, $n >> p$, by donor impurity doping to strongly p-type, $p >> n$, by acceptor impurity doping. **Being able to control the conductivity of a semiconductor by selective doping is what enables us to fabricate the variety of electronic devices that are available.**

Que: 6 *Derive the continuity equation.*

Answer: Derivation

The continuity equation describes a basic concept, namely that a change in carrier density over time is due to the difference between the incoming and outgoing flux of carriers plus the generation and minus the recombination. The flow of carriers and recombination and generation rates are illustrated with Figure

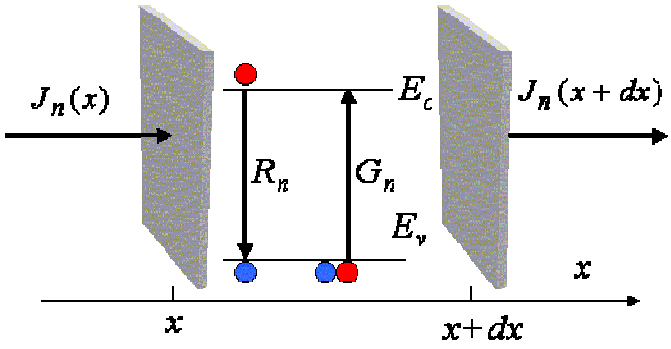


Figure: Electron currents and possible recombination and generation processes

The rate of change of the carriers between x and x + dx equals the difference between the incoming flux and the outgoing flux plus the generation and minus the recombination:

$$\frac{\partial n(x,t)}{\partial t} A\,dx = \left(\frac{J_n(x)}{-q} - \frac{J_n(x+dx)}{-q}\right) A + \left(G_n(x,t) - R_n(x,t)\right) A\,dx$$

where $n(x,t)$ is the carrier density, A is the area, $G_n(x,t)$ is the generation rate and $R_n(x,t)$ is the recombination rate. Using a Taylor series expansion,

$$J_n(x+dx) = J_n(x) + \frac{d\,J_n(x)}{dx} dx$$

this equation can be formulated as a function of the derivative of the current:

$$\frac{\partial n(x,t)}{\partial t} = \frac{1}{q} \frac{\partial J_n(x,t)}{\partial x} + G_n(x,t) - R_n(x,t)$$

and similarly for holes one finds:

$$\frac{\partial p(x,t)}{\partial t} = -\frac{1}{q} \frac{\partial J_p(x,t)}{\partial x} + G_p(x,t) - R_p(x,t)$$

A solution to these equations can be obtained by substituting the expression for the electron and hole current, (2.7.31) and (2.7.32). This then yields two partial differential equations as a function of the electron density, the hole density and the electric field. The electric field itself is obtained from Gauss's law.

$$\frac{dn(x,t)}{dt} = \mu_n n \frac{\partial \mathcal{E}(x,t)}{\partial x} + \mu_n \mathcal{E} \frac{\partial n(x,t)}{\partial x} + D_n \frac{\partial^2 n(x,t)}{\partial x^2} + G_n(x,t) - R_n(x,t)$$

$$\frac{dp(x,t)}{dt} = -\mu_p p \frac{\partial \mathcal{E}(x,t)}{\partial x} - \mu_p \mathcal{E} \frac{\partial p(x,t)}{\partial x} + D_p \frac{\partial^2 p(x,t)}{\partial x^2} + G_p(x,t) - R_p(x,t)$$

$$\frac{dp(x,t)}{dt}$$

A generalization in three dimensions yields the following continuity equations for electrons and holes:

$$\frac{\partial n(x,y,z,t)}{dt} = \frac{1}{q}\vec{\nabla}\vec{J}_n(x,y,z,t) + G_n(x,y,z,t) - R_n(x,y,z,t)$$

$$\frac{\partial p(x,y,z,t)}{\partial t} = -\frac{1}{q}\vec{\nabla}\vec{J}_p(x,y,z,t) + G_p(x,y,z,t) - R_p(x,y,z,t)$$

Que: 7 *Write notes on generation and recombination of charge carriers in semiconductor.*

Answer: An **Electron** is defined as a negative charge or negative polarity atomic particle. The electrons are free or attached to the nucleus of any atom. They exist in the various energy level or energy band of any atomic particle or atom. Movement of electrons generates an electric current in the semiconductor material. The charge on an electron is termed as the **unit electric charge.**

When energy is supplied to a semiconductor, a valence electron is lifted to a higher energy level, the departing electron leaves a vacancy in the valence band. This vacancy is known as **Hole**. Thus, in other words, we can define hole as a vacancy left in the valence band because of the lifting of an electron from the valence band to a conduction band is called as a Hole.

Electron-Hole Pairs

Whenever, some external energy in the form of heat energy is supplied to a semiconductor the valence electrons are lifted up to the conduction band one after the other leaving behind a vacancy in the valence band called the Hole.

The number of electrons to be lifted from the valence band to the conduction band depends upon the quantity of external energy supplied to the semiconductor.

If only one electron is lifted to the conduction band, then one hole is created in the valence band. Thus, each time an electron-hole pair is formed. The vacancy created by the electron in the valence band known as hole acts as a positive charge. It has a strong tendency to attract the electrons from the nearby covalent bonds.

Recombination of Electron and Hole

When some external energy is supplied to a semiconductor, the electron of the valence band is lifted to the conduction band and become free leaving behind the holes in the valence band. The orbit of the conduction band in which free electrons are moving is larger as compared to the orbit of the valence band in which the holes are formed.

The one atom of the conduction band orbit may intersect with the hole orbit of another atom. As a result of this intersection, the conduction band electron falls into a hole. This merging of the free electron and a hole is called **Recombination of Electron and Hole**. When the recombination takes place, the hole does not move anywhere, it just disappears.

This **recombination process** takes place continuously in a semiconductor and fills every hole. However, the incoming heat energy keeps producing new holes by lifting valence electrons up to the conduction band forming electron-hole pair. The creation of electron-hole pairs and their recombination goes on continuously.

The average timing between the creation and the disappearing of an electron-hole pair is termed as Lifetime. The lifetime varies from nanoseconds to several microseconds depending upon the various factors such as shape, size, crystal structure of the semiconductor material.

Que: 7 State and explain the Difference Between p Type and n Type Semiconductor

Answer: The various factors like doping element, nature of doping element, the majority and minority carriers in the p-type and n-type semiconductor. The density of electrons and holes, energy level and Fermi level, the direction of

movement of majority carriers, etc. are considered in explaining the difference between p-type and n-type semiconductors.

The difference between a p-type semiconductor and n-type semiconductor are given below in tabulated form.

Basis of difference	**p-type semiconductor**	**n-type semiconductor**
Group of Doping Element	In P type semiconductor III group element is added as doping element.	In n type semiconductor V group element is added as doping element.
Nature of Doping Element	Impurity added creates vacancy of electrons (holes) called as Acceptor Atom.	Impurity added provides extra electrons and is known as Donor Atom.
Type of impurity added	Trivalent impurity like Al, Ga, In etc. are added.	Pentavalent impurity like P, As, Sb, Bi etc. are added.
Majority Carriers	Holes are majority carriers	Electrons are majority carriers
Minority Carriers	Electrons are minority carriers	Holes are minority carriers
Density of Electrons and Holes	The hole density is much greater than the electron density. nh >> ne	The electron density is much greater than the hole density. ne >> nh
Energy level	The acceptor energy level is close to the valence band and away from the conduction band.	The donor energy level is close to the conduction band and away from the valence band.
Fermi level	Fermi level lies between acceptor energy level and the valence band.	Fermi level lies between donor energy level and the conduction band.

Basis of difference	p-type semiconductor	n-type semiconductor
Movement of Majority carriers	Majority carriers move from higher to lower potential.	Majority carriers move from lower to higher potential.

The p-type semiconductor is formed when the Trivalent impurity is added to the pure semiconductor. Similarly, when a Pentavalent impurity is added to the pure semiconductor n-type semiconductor is obtained.

Difference Between p-Type and n-Type Semiconductor

- In a p-type semiconductor, the III group element of the periodic table is added as a doping element, whereas in n-type the V group element is the doping element.
- Trivalent impurity like Aluminum, Gallium and Indium is added in the p-type semiconductor, while in n-type semiconductor Pentavalent impurity like Arsenic, Antimony, Phosphorus, Bismuth, etc. are added.
- The impurity added in p-type semiconductor provides extra holes known as Acceptor atom, whereas in n-type semiconductor impurity provides extra electrons and termed as Donor atom.
- In a p-type semiconductor, the majority carriers are holes, and minority carriers are electrons. In the n-type semiconductor, electrons are majority carriers, and holes are minority carriers.
- The electron density is much greater than the hole density in the n-type semiconductor denoted as $\mathbf{n_e >> n_h}$ whereas, in p-type semiconductor the hole density is much greater than the electron density $\mathbf{n_h >> n_e}$.
- In a n-type semiconductor, the donor energy level is close to the conduction band and away from the valence band. In the p-type semiconductor, the acceptor energy level is close to the valence band and away from the conduction band.

The Fermi level of the n-type semiconductor lies between donor energy level and the conduction band while the Fermi level of the p-type semiconductor lies between the acceptor energy level and the valence band.

Majority carriers move from higher to lower potential in p-type whereas, in n-type, the majority carriers move from lower to the higher potential.

Unit 2
Diode and its applications

Que: 1 Calculate the built-in potential barrier of a pn junction. Consider a silicon pn junction at T = 300 K, doped at Na = 10^{16} cm^{-3} in the p-region and Nd = $10^{17}cm^{-3}$ in the n-region.

Answer:

we have ni = $1.5 \times 10^{10}cm^{-3}$ for silicon at room temperature. We then find

$$V_{bi} = V_T \ln\left(\frac{N_a N_d}{n_i^2}\right) = (0.026)\ln\left[\frac{(10^{16})(10^{17})}{(1.5 \times 10^{10})^2}\right] = 0.757\,\text{V}$$

Unsolved:1 (a) Calculate V_{bi} for a GaAs pn junction at T = 300 K for Na = 10^{16} cm^{-3} and Nd = 10^{17} cm^{-3} (b) Repeat part (a) for a Germanium pn junction with the same doping concentrations.
(Ans. (a) Vbi = 1.23 V, (b) Vbi = 0.374 V).

Que: 2 Calculate the junction capacitance of a pn junction. Consider a silicon pn junction at T = 300 K, with doping concentrations of Na = 10^{16} cm^{-3} and Nd = 10^{15} cm^{-3}. Assume that ni = 1.5×10^{10} cm^{-3} and let Cjo = 0.5 pF. Calculate the junction capacitance at VR = 1V and VR = 5V.

Solution: The built-in potential is determined by

$$V_{bi} = V_T \ln\left(\frac{N_a N_d}{n_i^2}\right) = (0.026)\ln\left[\frac{(10^{16})(10^{15})}{(1.5 \times 10^{10})^2}\right] = 0.637\,\text{V}$$

The junction capacitance for VR = 1 V is then found to be

$$C_j = C_{jo}\left(1 + \frac{V_R}{V_{bi}}\right)^{-1/2} = (0.5)\left(1 + \frac{1}{0.637}\right)^{-1/2} = 0.312\,\text{pF}$$

For VR = 5 V

$$C_j = (0.5)\left(1 + \frac{5}{0.637}\right)^{-1/2} = 0.168\,\text{pF}$$

Unsolved:2 A silicon pn junction at T = 300 K is doped at Nd = 10^{16} cm^{-3} and Na = 10^{17} cm^{-3}. The junction capacitance is to be Cj = 0.8pF when a reverse bias voltage of VR = 5V is applied. Find the zero-biased junction capacitance Cjo.
(Ans. Cjo = 2.21 pF)

Que: 3 Determine the current in a pn junction diode. Consider a pn junction at T = 300 K in which $I_S = 10^{-14}$ A and n = 1. Find the diode current for v_D = +0.70 V and v_D = −0.70 V.

Solution: For v_D = +0.70 V, the pn junction is forward-biased and we find

$$i_D = I_S\left[e^{\left(\frac{v_D}{V_T}\right)} - 1\right] = (10^{-14})\left[e^{\left(\frac{0.70}{0.026}\right)} - 1\right] \Rightarrow 4.93\,\text{mA}$$

For v_D = −0.70V, the pn junction is reverse-biased and we find

$$i_D = I_S\left[e^{\left(\frac{v_D}{V_T}\right)} - 1\right] = (10^{-14})\left[e^{\left(\frac{-0.70}{0.026}\right)} - 1\right] \cong -10^{-14}\,\text{A}$$

Unsolved:3 (**a**) A silicon pn junction at T = 300 K has a reverse-saturation current of $IS = 2 \times 10^{-14}$ A. Determine the required forward-bias voltage to produce a current of (i) I_D = 50 μA and (ii) I_D = 1 mA.

(**b**) Repeat part (a) for $I_S = 2 \times 10^{-12}$ A.

(Ans. (a) (i) 0.563 V, (ii) 0.641 V; (b) (i) 0.443 V, (ii) 0.521 V).

Que: 4 Determine diode voltages. The reverse saturation currents of a pn junction diode and a Schottky diode are $I_S = 10^{-12}$ A and 10^{-8} A, respectively. Determine the forward-bias voltages
required to produce 1 mA in each diode.

Solution: The diode current-voltage relationship is given by

Solving for the diode voltage, we obtain

$$V_D = V_T \ln\left(\frac{I_D}{I_S}\right)$$

We then find, for the pn junction diode

$$V_D = (0.026)\ln\left(\frac{1 \times 10^{-3}}{10^{-12}}\right) = 0.539\ \text{V}$$

and, for the Schottky diode

$$V_D = (0.026)\ln\left(\frac{1 \times 10^{-3}}{10^{-8}}\right) = 0.299\ \text{V}$$

Unsolved:4 A pn junction diode and a Schottky diode both have forward-bias currents of 1.2mA. The reverse-saturation current of the pn junction diode is $I_S = 4 \times 10^{-15}$ A. The difference in forward-bias voltages is 0.265 V. Determine the reverse-saturation current of the Schottky diode.
(**Ans**. $I_S = 1.07 \times 10^{-10}$ A)

Que: 5 How is a pn junction formed? What is meant by a built-in potential barrier, and
how is it formed?

Solution: In the preceding sections, we looked at characteristics of semiconductor materials.
The real power of semiconductor electronics occurs when p- and n-regions are directly adjacent to each other, forming a **pn junction.** One important concept to remember is that in most integrated circuit applications, the entire semiconductor material is a single crystal, with one region doped to be p-type and the adjacent region doped to be n-type.
The Equilibrium pn Junction Figure 1.10(a) is a simplified block diagram of a pn junction. Figure 1.10(b) shows the respective p-type and n-type doping concentrations, assuming uniform doping in each region, as well as the minority carrier concentrations in each region, assuming thermal equilibrium. Figure 1.10(c) is a three-dimensional diagram of the pn junction showing the cross-sectional area of the device.
The interface at $x = 0$ is called the **metallurgical junction.** A large density gradient in both the hole and electron concentrations occurs across this junction. Initially, then, there is a diffusion of holes from the p-region into the n-region, and a diffusion of electrons from the n-region into the p-region (Figure 1.11). The flow of holes from the p-region uncovers negatively charged acceptor ions, and the flow of

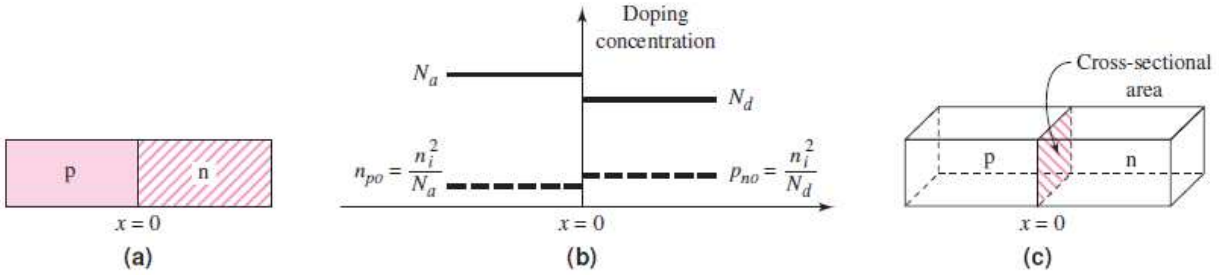


Figure 1.10 (a) The pn junction: (a) simplified one-dimensional geometry, (b) doping profile of an ideal uniformly doped pn junction, and (c) three-dimensional representation showing the cross-sectional area

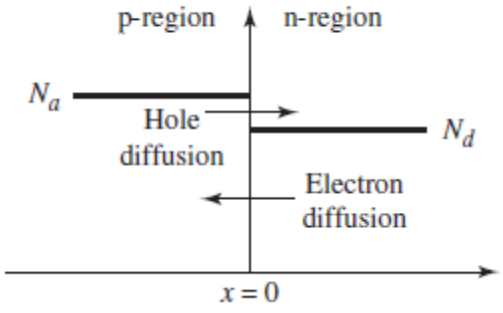


Figure 1.11 Initial diffusion of electrons and holes across the metallurgical junction at the "instant in time" that the p- and n-regions are joined together

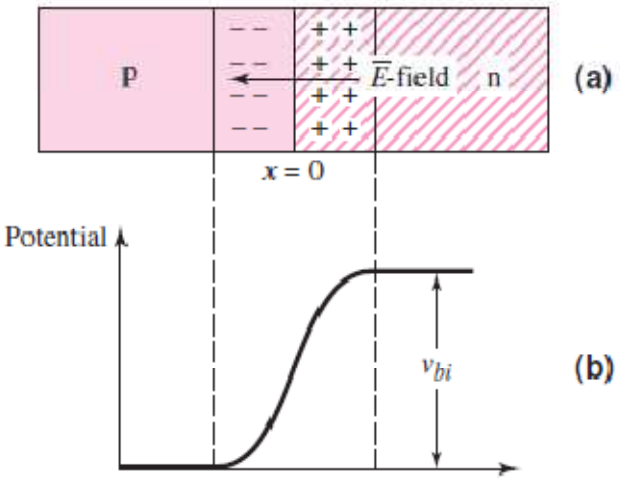


Figure 1.12 The pn junction in thermal equilibrium. (a) The space charge region with negatively charged acceptor ions in the p-region and positively charged donor ions in the n-region; the resulting electric field from the n- to the p-region. (b) The potential through the junction and the built-in potential barrier *Vbi* across the junction.

Electrons from the n-region uncovers positively charged donor ions. This action creates a charge separation (Figure 1.12(a)), which sets up an electric field oriented in the direction from the positive charge to the negative charge. If no voltage is applied to the pn junction, the diffusion of holes and electrons must eventually cease. The direction of the induced electric field will cause the resulting force to repel the diffusion of holes from the p-region and the diffusion of electrons from the n-region. Thermal equilibrium occurs when the force produced by the electric field and the "force" produced by the density gradient exactly balance.

The positively charged region and the negatively charged region comprise the **space-charge** region, or **depletion region,** of the pn junction, in which there are essentially no mobile electrons or holes. Because of the electric field in the spacecharge region, there is a potential difference across that region (Figure 1.12(b)). This potential difference is called the **built-in potential barrier,** or built-in voltage, and is given by

$$V_{bi} = \frac{kT}{e}\ln\left(\frac{N_a N_d}{n_i^2}\right) = V_T \ln\left(\frac{N_a N_d}{n_i^2}\right)$$

where $V_T = kT/e$, k = Boltzmann's constant, T = absolute temperature, e = the magnitude of the electronic charge, and N_a and N_d are the net acceptor and donor concentrations in the p- and n-regions, respectively. The parameter *VT* is called the **thermal voltage** and is approximately V_T = 0.026 V at room temperature, T = 300 K.

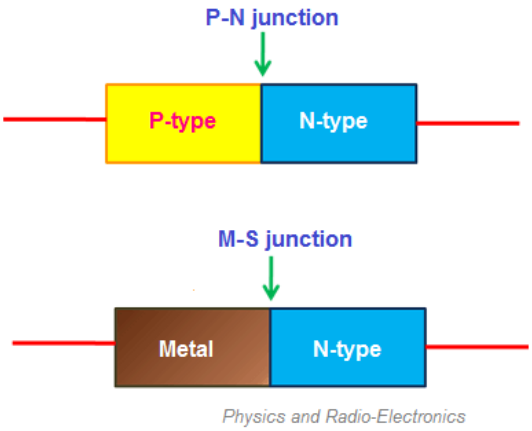
Que: 6. What is a schottky diode? Also explain schottky barrier.

Answer: Schottky diode is a metal-semiconductor junction diode that has less forward voltage drop than the P-N junction diode and can be used in high-speed switching applications.

In a normal p-n junction diode, a p-type semiconductor and an n-type semiconductor are used to form the p-n junction. When a p-type semiconductor is joined with an n-type semiconductor, a junction is formed between the P-type and N-type semiconductor. This junction is known as P-N junction.

In schottky diode, metals such as aluminum or platinum replace the P-type semiconductor. The schottky diode is named after German physicist Walter H. Schottky.

Schottky diode is also known as schottky barrier diode, surface barrier diode, majority carrier device, hot-electron diode, or hot carrier diode. Schottky diodes are widely used in radio frequency (RF) applications.



When aluminum or platinum metal is joined with N-type semiconductor, a junction is formed between the metal and N-type semiconductor. This junction is known as a metal-semiconductor junction or M-S junction. A metal-semiconductor junction formed between a metal and n-type semiconductor creates a barrier or depletion layer known as a schottky barrier.

Schottky diode can switch on and off much faster than the p-n junction diode. Also, the schottky diode produces less unwanted noise than p-n junction diode. These two characteristics of the schottky diode make it very useful in high-speed switching power circuits.

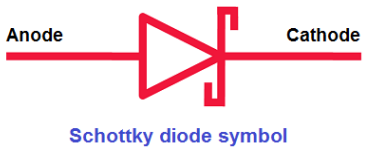
When sufficient voltage is applied to the schottky diode, current starts flowing in the forward direction. Because of this current flow, a small voltage loss occurs across the terminals of the schottky diode. This voltage loss is known as voltage drop.

A silicon diode has a voltage drop of 0.6 to 0.7 volts, while a schottky diode has a voltage drop of 0.2 to 0.3 volts. Voltage loss or voltage drop is the amount of voltage wasted to turn on a diode.

The voltage needed to turn on the schottky diode is same as that of a germanium diode. But germanium diodes are rarely used because the switching speed of germanium diodes is very low as compared to the schottky diodes.

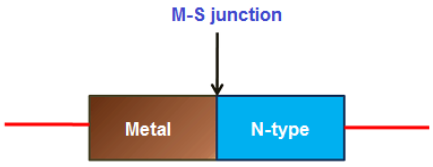
Symbol of schottky diode

The symbol of schottky diode is shown in the below figure. In schottky diode, the metal acts as the anode and n-type semiconductor acts as the cathode.



Metal-semiconductor (M-S) junction

Metal-semiconductor (M-S) junction is a type of junction formed between a metal and an n-type semiconductor when the metal is joined with the n-type semiconductor. Metal-semiconductor junction is also sometimes referred to as M-S junction.



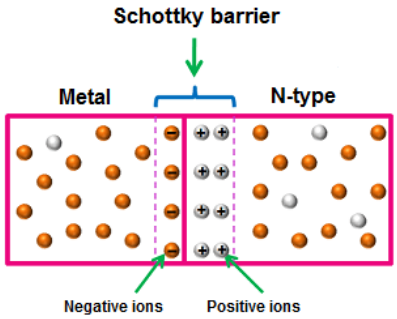
The metal-semiconductor junction can be either non-rectifying or rectifying. The non-rectifying metal-semiconductor junction is called ohmic contact. The rectifying metal-semiconductor junction is called non-ohmic contact.

Que: 7. How schottky diode works?

Answer: Schottky barrier is a depletion layer formed at the junction of a metal and n-type semiconductor. In simple words, schottky barrier is the potential

energy barrier formed at the metal-semiconductor junction. The electrons have to overcome this potential energy barrier to flow across the diode.

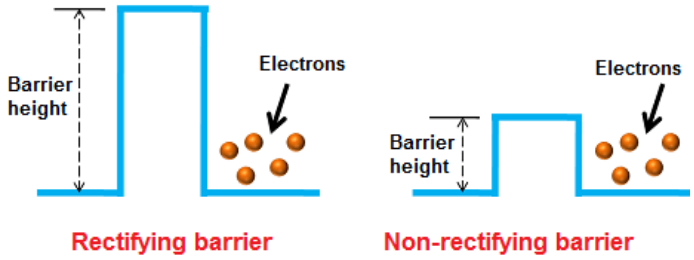
The rectifying metal-semiconductor junction forms a rectifying schottky barrier. This rectifying schottky barrier is used for making a device known as schottky diode. The non-rectifying metal-semiconductor junction forms a non-rectifying schottky barrier.



One of the most important characteristics of a schottky barrier is the schottky barrier height. The value of this barrier height depends on the combination of semiconductor and metal.

The schottky barrier height of ohmic contact (non-rectifying barrier) is very low whereas the schottky barrier height of non-ohmic contact (rectifying barrier) is high.

In non-rectifying schottky barrier, the barrier height is not high enough to form a depletion region. So depletion region is negligible or absent in the ohmic contact diode.



On the other hand, in rectifying schottky barrier, the barrier height is high enough to form a depletion region. So the depletion region is present in the non-ohmic contact diode.

The non-rectifying metal-semiconductor junction (ohmic contact) offers very low resistance to the electric current whereas the rectifying metal-

semiconductor junction offers high resistance to the electric current as compared to the ohmic contact.

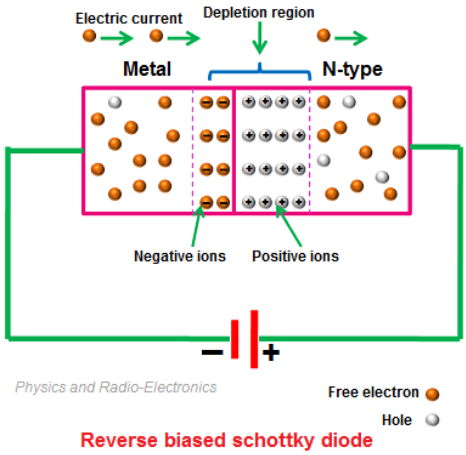
The rectifying schottky barrier is formed when a metal is in contact with the lightly doped semiconductor, whereas the non-rectifying barrier is formed when a metal is in contact with the heavily doped semiconductor.

The ohmic contact has a linear current-voltage (I-V) curve whereas the non-ohmic contact has a non-linear current-voltage (I-V) curve.

Reverse bias schottky diode :

If the negative terminal of the battery is connected to the metal and the positive terminal of the battery is connected to the n-type semiconductor, the schottky diode is said to be reverse biased.

When a reverse bias voltage is applied to the schottky diode, the depletion width increases. As a result, the electric current stops flowing. However, a small leakage current flows due to the thermally excited electrons in the metal.



Reverse biased schottky diode

If the reverse bias voltage is continuously increased, the electric current gradually increases due to the weak barrier.

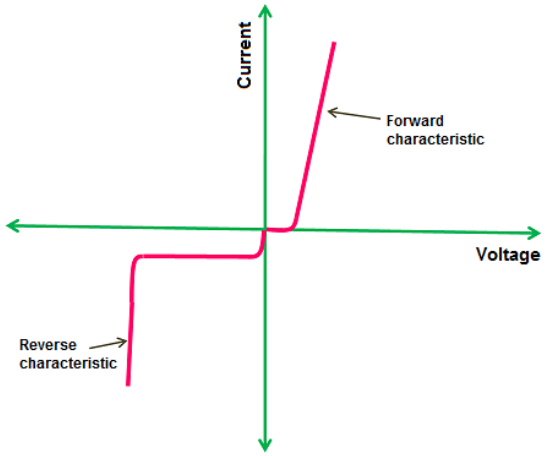
If the reverse bias voltage is largely increased, a sudden rise in electric current takes place. This sudden rise in electric current causes depletion region to break down which may permanently damage the device.

V-I characteristics of schottky diode

The V-I (Voltage-Current) characteristics of schottky diode is shown in the below figure. The vertical line in the below figure represents the current flow in

the schottky diode and the horizontal line represents the voltage applied across the schottky diode.

The V-I characteristics of schottky diode is almost similar to the P-N junction diode. However, the forward voltage drop of schottky diode is very low as compared to the P-N junction diode.



V-I characteristics of schottky diode

The forward voltage drop of schottky diode is 0.2 to 0.3 volts whereas the forward voltage drop of silicon P-N junction diode is 0.6 to 0.7 volts.

If the forward bias voltage is greater than 0.2 or 0.3 volts, electric current starts flowing through the schottky diode.

In schottky diode, the reverse saturation current occurs at a very low voltage as compared to the silicon diode.

Que: 8. Differentiate between schottky diode and P-N junction diode

Answer: The main difference between schottky diode and p-n junction diode is as follows:

In schottky diode, the free electrons carry most of the electric current. Holes carry negligible electric current. So schottky diode is a unipolar device. In P-N junction diode, both free electrons and holes carry electric current. So P-N junction diode is a bipolar device.

The reverse breakdown voltage of a schottky diode is very small as compared to the p-n junction diode.

In schottky diode, the depletion region is absent or negligible, whereas in p-n junction diode the depletion region is present.

The turn-on voltage for a schottky diode is very low as compared to the p-n junction diode.

In schottky diode, electrons are the majority carriers in both metal and semiconductor. In P-N junction diode, electrons are the majority carriers in n-region and holes are the majority carriers in p-region.

Que: 9. State and explain the advantages, disadvantages and applications of schottky diode

Answer: Advantages of schottky diode

- Low junction capacitance

We know that capacitance is the ability to store an electric charge. In a P-N junction diode, the depletion region consists of stored charges. So there exists a capacitance. This capacitance is present at the junction of the diode. So it is known as junction capacitance.

In schottky diode, stored charges or depletion region is negligible. So a schottky diode has a very low capacitance.

- Fast reverse recovery time

The amount of time it takes for a diode to switch from ON state to OFF state is called reverse recovery time.

In order to switch from ON (conducting) state to OFF (non-conducting) state, the stored charges in the depletion region must be first discharged or removed before the diode switch to OFF (non-conducting) state.

The P-N junction diode do not immediately switch from ON state to OFF state because it takes some time to discharge or remove stored charges at the depletion region. However, in schottky diode, the depletion region is negligible. So the schottky diode will immediately switch from ON to OFF state.

- High current density

We know that the depletion region is negligible in schottky diode. So applying is small voltage is enough to produce large current.

- Low forward voltage drop or low turn on voltage

The turn on voltage for schottky diode is very small as compared to the P-N junction diode. The turn on voltage for schottky diode is 0.2 to 0.3 volts

whereas for P-N junction diode is 0.6 to 0.7 volts. So applying a small voltage is enough to produce electric current in the schottky diode.

- High efficiency
- Schottky diodes operate at high frequencies.
- Schottky diode produces less unwanted noise than P-N junction diode.

Disadvantages of schottky diode

- Large reverse saturation current

Schottky diode produces large reverse saturation current than the p-n junction diode.

Applications of schottky diodes

- Schottky diodes are used as general-purpose rectifiers.
- Schottky diodes are used in radio frequency (RF) applications.
- Schottky diodes are widely used in power supplies.
- Schottky diodes are used to detect signals.
- Schottky diodes are used in logic circuits.

Que: 10. Write notes on varactor diode

Answer: The varactor diode was named because of the variable reactor or variable reactance or variable capacitor or variable capacitance property of these diodes. A varactor diode is considered as a special type of diode that is widely used in the electronics industry and is used in various electronics applications. Varactor diode is also a semiconductor microwave solid-state device, it is frequently used in applications where variable capacitance is desired which can be achieved by controlling voltage.

Varactor Diode Basics

Varactor diodes are also termed as varicap diodes, in fact, these days they are usually termed as varactor diodes. Even though the variable capacitance effect can be exhibited by the normal diodes (P-N junction diodes), but, varactor diodes are preferred for giving the desired capacitance changes as they are special types of diodes. These diodes are specially manufactured and optimized

such that they enables a very high range of changes in capacitance. Varactor diodes are again classified into various types based on the varactor diode junction properties. And, these are termed as abrupt varactor diodes, gallium-arsenide varactor diodes, and hyper abrupt varactor diodes.

Varactor Diode Symbol

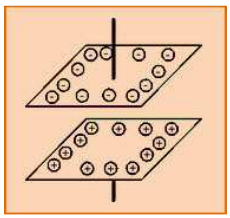
The symbol of varactor diode is shown in the figure. The varactor diode symbol consists of the capacitor symbol at one end of the diode that represents the variable capacitor characteristics of the varactor diodes.

Varactor Diode Symbol

In general, it looks like a normal PN- junction diode in which one terminal is termed as the cathode and the other terminal is termed as anode. Here, varactor diode consists of two lines at one end (cathode end of normal diode) that indicates the capacitor symbol.

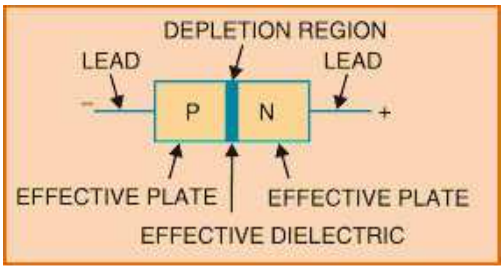
Varactor Diode Working

To understand the working principle of the varactor diode, we must know what is a capacitor and how can we change the capacitance. Let us consider the capacitor that consists of two plates separated by an insulating dielectric as shown in the figure.



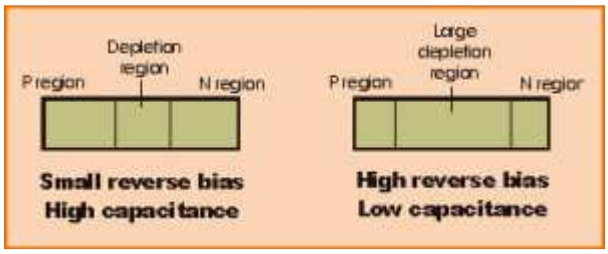
Capacitor

We know that the capacitance of an electrical capacitor is directly proportional to the area of the plates, as the area of the plates increases the capacitance of the capacitor increases. Consider the reverse biased mode of the diode, in which P-type region and N-type region are able to conduct and thus can be treated as two plates. The depletion region between the P-type and N-type regions can be considered as insulating dielectric. Thus, it is exactly similar to the capacitor shown above.



Varactor Diode with P-N Junctoin and Depletion Region

The size of the depletion region of diode changes with change in reverse bias. If the varactor diode reverse voltage is increased, then the depletion region size increases. Similarly, if the varactor diode reverse voltage is decreased, then the depletion region size decreases or narrows.



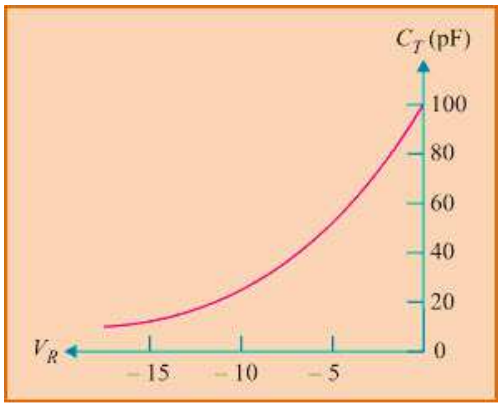
Variation of Capacitance with Variation in Depletion Region of Varactor Diode

Hence, by varying the reverse bias of the varactor diode the capacitance can be varied.

Varactor Diode Characteristics

The varactor diodes have the following significant characteristics:

- Varactor diodes produces considerably less noise compared to other conventional diodes.
- These diodes are available at low costs.
- Varactor diodes are more reliable.
- The varactor diodes are small in size and hence, they are very light weight.
- There is no useful purpose of varactor diode operated when it is operated in forward bias.
- Increase in reverse bias of varactor diode increases the capacitance as shown in the figure below.



Characteristics of Varactor Diode

Varactor Diode Applications

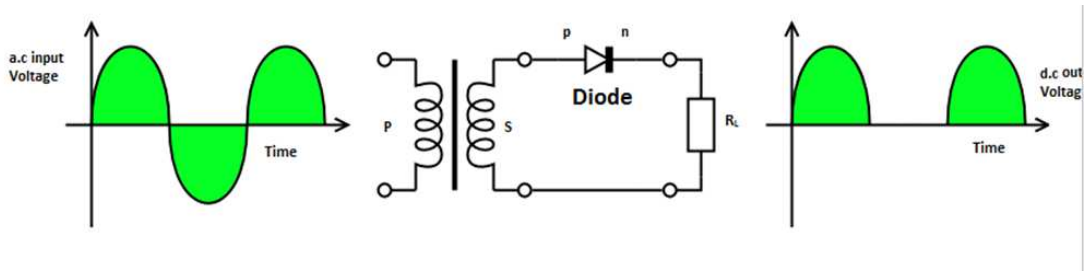
Varactor diodes finds large number of applications within the RF design arena and it is difficult to discuss about all the applications of varactor diodes or varicap diodes. However, in this article, we are discussing about the worth providing (couple of applications) applications of varactor diodes, to show how the varactor diodes can be used in a practical circuit. The capacitor in a circuit can be replaced with the varactor diode, but it is essential to ensure the tune voltage, i.e. the voltage required to set the varactor diode capacitance. And ensure that varactor diode is not affected by the bias voltage or any other voltages in the circuit. By using voltage control technique in the varactor diode circuit, varying capacitance can be provided.

Que: 11 What is Half Wave Rectifier?

Answer: In a half-wave rectifier, one half of each a.c input cycle is rectified. When the p-n junction diode is forward biased, it gives little resistance and when it is reversing biased it provides high resistance. During one-half cycles, the diode is forward biased when the input voltage is applied and in the opposite half cycle, it is reverse biased. During alternate half cycles, the optimum result can be obtained.

Working of Half Wave Rectifier

The half wave rectifier has both positive and negative cycles. During the positive half of the input, the current will flow from positive to negative which will generate only positive half cycle of the a.c supply. When a.c supply is applied to the transformer, the voltage will be decreasing at the secondary winding of the diode. All the variations in the a.c supply will reduce and we will get the pulsating d.c voltage to the load resistor.



In the second half cycle, current will flow from negative to positive and the diode will be reverse biased. Thus, at the output side, there will be no current generated and we cannot get power at the load resistance. A small amount of reverse current will flow during reverse bias due to minority carriers.

Characteristics of Half Wave Rectifier

Following are the characteristics of half wave rectifier:

Ripple Factor

Ripples are the oscillations that are obtained in the DC which is corrected by using filters such as inductors and capacitors. These ripples are measured with the help of ripple factor and is denoted by γ. Ripple factor tells us the amount of ripples present in the output DC. Higher the ripple factor, more is the oscillation at the output DC and lower is the ripple factor, less is the oscillation at the output DC.

Ripple factor is the ratio of rms value of AC component of output voltage to the DC component of the output voltage.

$$\gamma = \sqrt{(\frac{V_{rms}}{V_{DC}})^2 - 1}$$

DC Current

DC current is given as:

$$I_{DC} = \frac{I_{max}}{\pi}$$

Where I_{max} is the maximum DC load current

DC Output Voltage

The output DC voltage appears at the load resistor R_L which is obtained by multiplying output DC voltage with the load resistor R_L. The output DC voltage is given as:

$$V_{DC} = \frac{V_{Smax}}{\pi}$$

Where V_{Smax} is the maximum secondary voltage

Form Factor

Form factor is the ratio of rms value to the DC value. ***For a half wave rectifier form factor is 1.57.***

Rectifier Efficiency

Rectifier efficiency is the ratio of output DC power to the input AC power. ***For a half wave rectifier, rectifier efficiency is 40.6%.***

Advantages of Half Wave Rectifier

- Affordable
- Simple connections
- Easy to use as the connections are simple
- Number of components used are less

Disadvantages of Half Wave Rectifier

- Ripple production is more
- Harmonics are generated
- Utilization of transformer is very low
- Efficiency of rectification is low

Applications of Half Wave Rectifier

Following are the uses of half wave rectification:

- **Power rectification:** Half wave rectifier is used along with transformer for power rectification as a powering equipment.
- **Signal demodulation:** Half wave rectifiers are used for demodulating the AM signals.

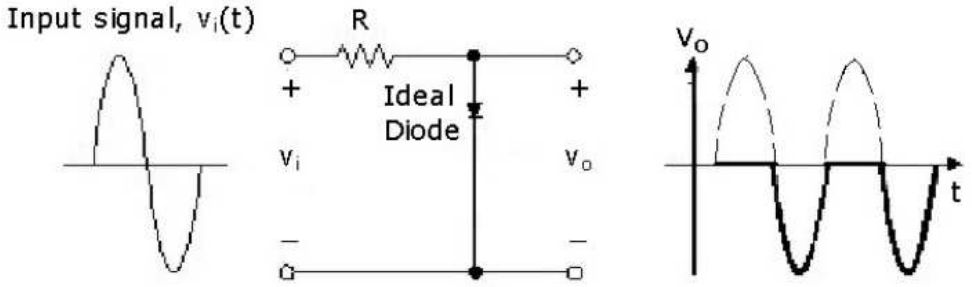
- **Signal peak detector:** Half wave rectifier is used for detecting the peak of the incoming waveform.

Que: 12 Explain clipper circuit.

Answer: Clippers Clipping circuits (also known as limiters, amplitude selectors, or slicers), are used to remove the part of a signal that is above or below some defined reference level. We've already seen an example of a clipper in the half-wave rectifier – that circuit basically cut off everything at the reference level of zero and let only the positive-going (or negative-going) portion of the input waveform through.

To clip to a reference level other than zero, a dc source (shown as a battery in your text) is put in series with the diode. Depending on the direction of the diode and the polarity of the battery, the circuit will either clip the input waveform above or below the reference level (the battery voltage for an ideal diode; i.e., for Von=0). This process is illustrated in the four parts of Figure

Without the battery, the output of the circuit below would be the negative portion of the input wave (assuming the bottom node is grounded). When vi > 0, the diode is on (short-circuited), vi is dropped across R and vo=0. When vi <0, the diode is off (open-circuited), the voltage across R is zero and vo=vi. (Don't worry; we won't be doing this for all the circuits!) Anyway, the reference level would be zero



With the battery in the orientation shown in Figure (and below), the diode doesn't turn on until vi > VB (If this looks strange, revisit the definition of forward bias). This shifts the reference level up and clips the input at +VB and passes everything for vi < VB.

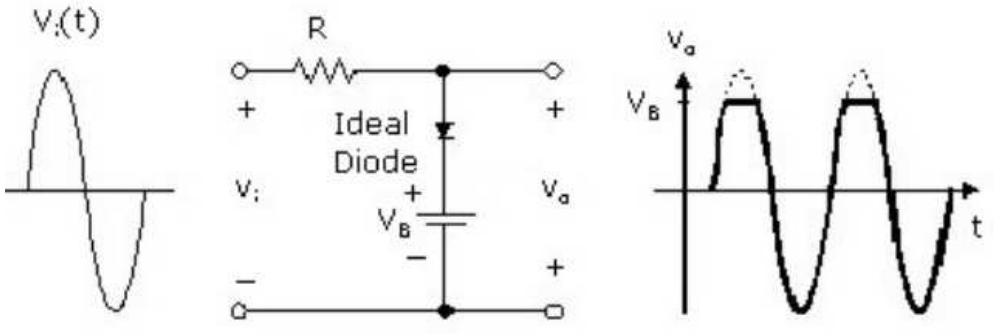
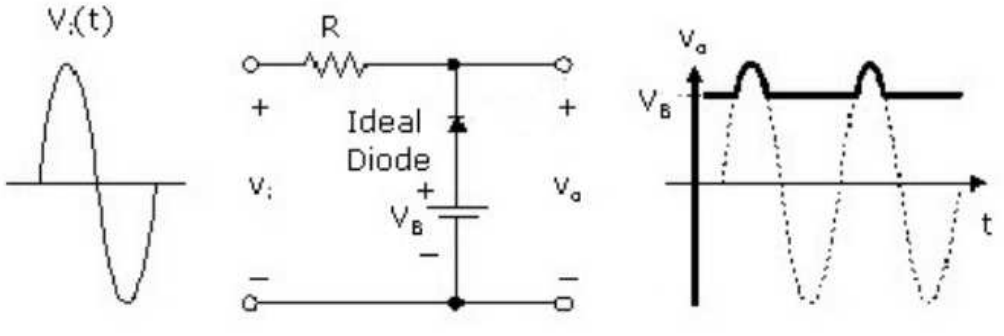
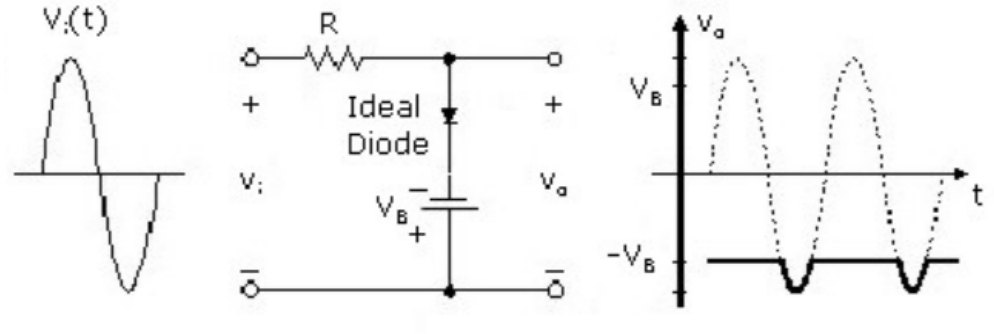


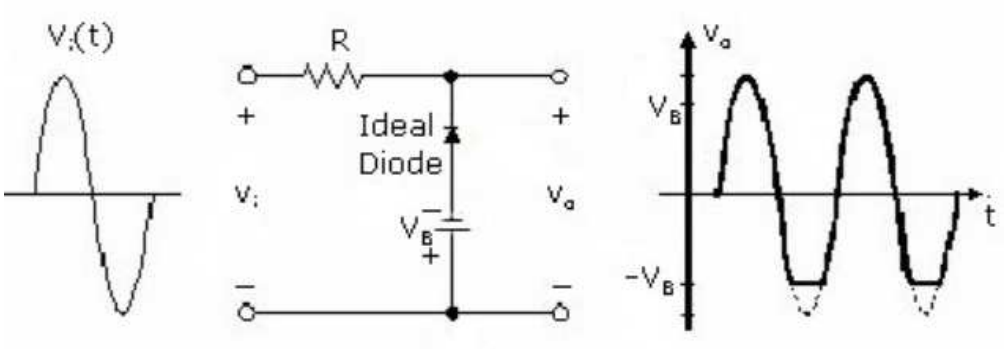
Figure 3.43b has the battery with the same orientation as in part (a), but the diode has been flipped. Without the battery, the positive portion of the input waveform would be passed (i.e., a reference level of zero).With the battery, the diode conducts for vi < VB. This means that the reference level is shifted to +VB and only vi > VB appears at the output



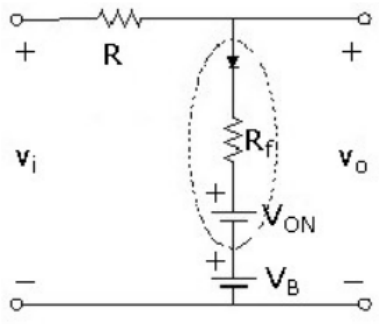
Again referencing part (a), the diode is in the original position but the polarities on the battery have been switched in Figure 3.43c. The discussion follows the same logic as earlier, but now the reference level has been shifted to –VB. The final result is that vo = vi for vi < -VB.



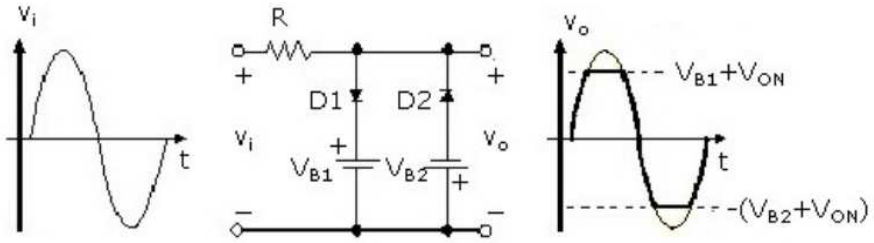
Finally, Figure 3.43d behaves the same as part (b), but the polarity on the battery has been switched, shifting the reference level to -VB. The signal that appears as the output is vi as long as vi > - VB.



To accommodate a practical diode, the turn-on voltage (VON=0.7V for silicon) and forward resistance (Rf) are included, along with the ideal diode, in the model (as shown in Figure 3.44a, reproduced to the right). The effective reference level will either have a magnitude of VB+VON or VB-VON, depending on the relative polarities of the two sources (review combining voltage sources in series if necessary). Including Rf in the diode path creates a voltage divider when the diode is forward biased. The result of this slight drop across Rf (remember that the forward resistance is generally pretty small), is a slight distortion in the output waveform – it is no longer strictly "limited" or "clipped" to the reference level, as is illustrated in Figure in your text. The four possible configurations of Figure are still valid, with the effective reference level ranging in magnitude from 0.7V (if VB=0) on up.



A parallel-biased clipper is a circuit that clips the positive and negative-going portions of the input signal simultaneously. This is designed by using two parallel diodes oriented in opposite directions – note that it is very important that the diodes are oppositely oriented (think voltage sources in parallel – a big no-no!). Just as in our previous discussion, the path containing diode D1 will provide the upper limit with reference level VB1+VON(with the VB1 polarity shown) and the path containing D2 will provide the lower limit with reference level VB2+VON (with the VB2 polarity shown). An example of this type of clipper, with the resulting output waveform is shown below (Figure 3.45 of your text, where it looks like they assumed Rf was negligible):



A series-biased clipper involves placing a battery in series with the input. The result of this modification is that the input signal is no longer symmetric about the zero axis, but instead shifts by an amount defined by the magnitude and polarity of VB. In Figure , the four possible permutations and the resulting output waveforms are shown for an ideal diode. When you look at this figure, keep in mind that the input signal is swinging between +2 and –2 volts and the battery magnitude VB is 1 volt. This may avoid some confusion when looking at the output waveforms – the (2V+VB) is just 3 volts and the –(2V-VB) may be replaced by –1 volt. The series placement of the battery is not changing the input waveform in any way, it is simply affecting when the diode turns on. To include the effects of a practical diode, include VON and RF in the diode path and crunch the math...

Unit 3
Device Fabrication Process

Que: 1 Explain the Steps of CMOS Fabrication Process

Answer: The CMOS can be fabricated using different processes such as:

- n-well process for CMOS fabrication
- P-well process
- Twin tub-CMOS-fabrication process

N The fabrication of CMOS can be done by following the below shown twenty steps, by which CMOS can be obtained by integrating both the NMOS and PMOS transistors on the same chip substrate. For integrating these NMOS and PMOS devices on the same chip, special regions called as wells or tubs are required in which semiconductor type and substrate type are opposite to each other.

A P-well has to be created on a N-substrate or N-well has to be created on a P-substrate. In this article, the fabrication of CMOS is described using the P-substrate, in which the NMOS transistor is fabricated on a P-type substrate and the PMOS transistor is fabricated in N-well.

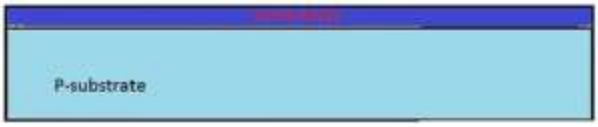
- The fabrication process involves twenty steps, which are as follows:

Step1: Substrate

Primarily, start the process with a P-substrate.

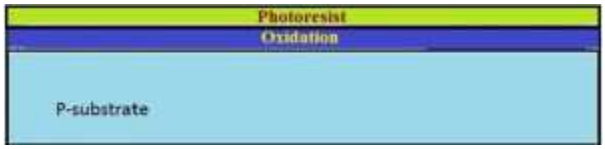
Step2: Oxidation

The oxidation process is done by using high-purity oxygen and hydrogen, which are exposed in an oxidation furnace approximately at 1000 degree centigrade.



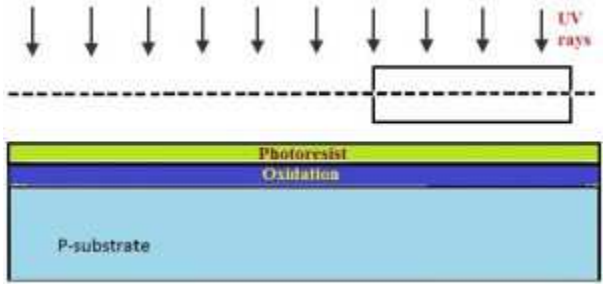
Step3: Photoresist

A light-sensitive polymer that softens whenever exposed to light is called as Photoresist layer. It is formed.



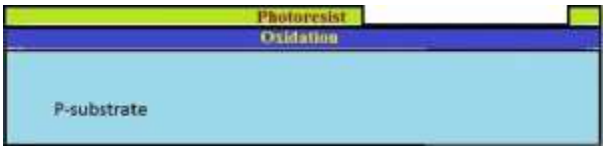
Step4: Masking

The photoresist is exposed to UV rays through the N-well mask



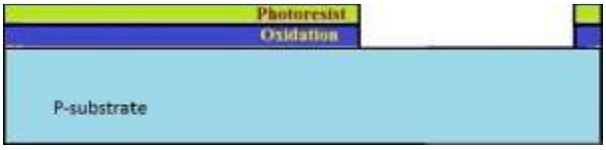
Step5: Photoresist removal

A part of the photoresist layer is removed by treating the wafer with the basic or acidic solution.



Step6: Removal of SiO2 using acid etching

The SiO2 oxidation layer is removed through the open area made by the removal of photoresist using hydrofluoric acid.

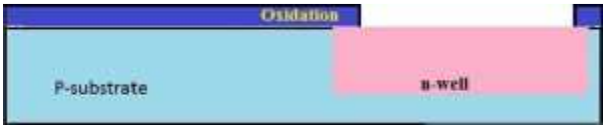


Step7: Removal of photoresist

The entire photoresist layer is stripped off, as shown in the below figure.

Step8: Formation of the N-well

By using ion implantation or diffusion process N-well is formed.

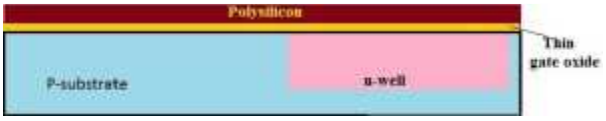


Step9: Removal of SiO2

Using the hydrofluoric acid, the remaining SiO2 is removed.

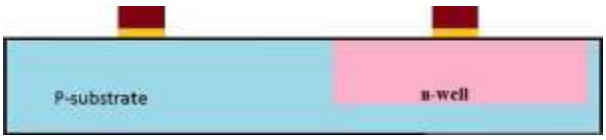
Step10: Deposition of polysilicon

Chemical Vapor Deposition (CVD) process is used to deposit a very thin layer of gate oxide.



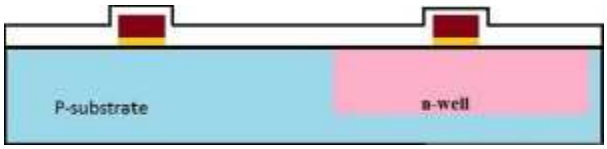
Step11: Removing the layer barring a small area for the Gates

Except the two small regions required for forming the Gates of NMOS and PMOS, the remaining layer is stripped off.



Step12: Oxidation process

Next, an oxidation layer is formed on this layer with two small regions for the formation of the gate terminals of NMOS and PMOS.



Step13: Masking and N-diffusion

By using the masking process small gaps are made for the purpose of N-diffusion.

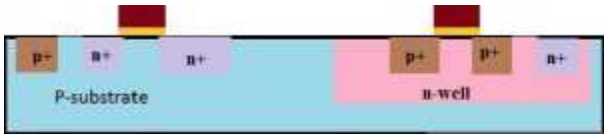
The n-type (n+) dopants are diffused or ion implanted, and the three n+ are formed for the formation of the terminals of NMOS.

Step14: Oxide stripping

The remaining oxidation layer is stripped off

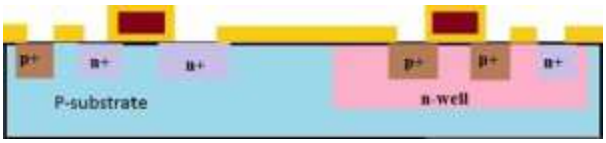
Step15: P-diffusion

Similar to the above N-diffusion process, the P-diffusion regions are diffused to form the terminals of the PMOS.



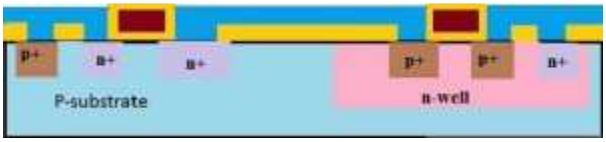
Step16: Thick field oxide

A thick-field oxide is formed in all regions except the terminals of the PMOS and NMOS.



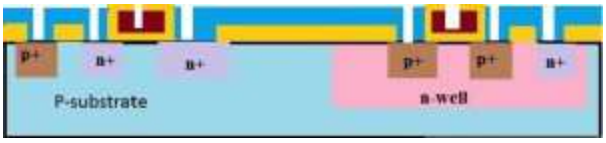
Step17: Metallization

Aluminum is sputtered on the whole wafer.



Step18: Removal of excess metal

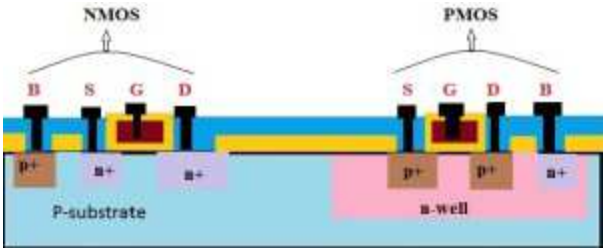
The excess metal is removed from the wafer layer.



Step19: Terminals

The terminals of the PMOS and NMOS are made from respective gaps.

Step20: Assigning the names of the terminals of the NMOS and PMOS

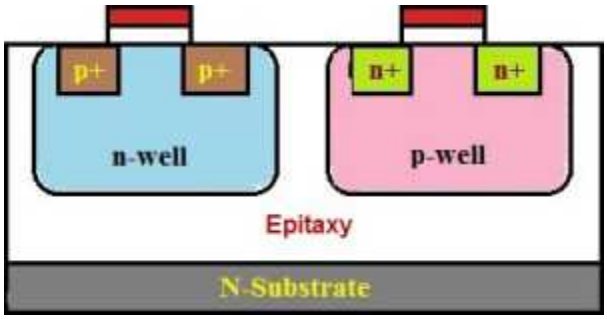


Fabircation of CMOS using P-well process

Among all the fabrication processes of the CMOS, N-well process is mostly used for the fabrication of the CMOS. P-well process is almost similar to the N-well.

But the only difference in p-well process is that it consists of a main N-substrate and, thus, P-wells itself acts as substrate for the N-devices.

Twin tub-CMOS Fabrication Process



In this process, separate optimization of the n-type and p-type transistors will be provided. The independent optimization of Vt, body effect and gain of the P-devices, N-devices can be made possible with this process.

Different steps of the fabrication of the CMOS using the twintub process are as follows:

- Lightly doped n+ or p+ substrate is taken and, to protect the latch up, epitaxial layer is used.
- The high-purity controlled thickness of the layers of silicon are grown with exact dopant concentrations.
- The dopant and its concentration in Silicon are used to determine electrical properties.
- Formation of the tub
- Thin oxide construction
- Implantation of the source and drain
- Cuts for making contacts
- Metallization

By using the above steps we can fabricate CMOS using twin tub process method.

Que 2: What is Oxidation in IC manufacturing process?

Answer: Oxidation is a process which converts silicon on the wafer into silicon dioxide. The chemical reaction of silicon and oxygen already starts at room temperature but stops after a very thin native oxide film. For an effective oxidation rate the wafer must be settled to a furnace with oxygen or water vapor at elevated temperatures. Silicon dioxide layers are used as high-quality

insulators or masks for ion implantation. The ability of silicon to form high quality silicon dioxide is an important reason, why silicon is still the dominating material in IC fabrication.

Oxidation refers to the conversion of the silicon wafer to silicon oxide (SiO_2or more generally SiOx). The ability of Si to form an oxide layer is very important since this is one of the reasons for choosing Si over Ge. The Horni transistor design, which was used in the first integrated circuit by Robert Noyce, was made of Si and the formation of SiOx helped in fabricating a planar device. Si exposed to ambient conditions has a native oxide on its surface. The native oxide is approximately 3nmthick at room temperature. But this is too thin for most applications and hence a thicker oxide needs to be grown. This is done by consuming the underlying Si to form SiOx. This is a grown layer. It is also possible to grow SiOx by a chemical vapor deposition process using Si and O precursor molecules. In this case, the underlying Si in the wafer is not consumed. This is called a deposited layer. SiOx helps in protecting the wafer from contamination, both physical and chemical. Thus, it acts as a passivating layer. The oxide layer protects the wafer surface from scratches and it also prevents dust from interacting with the wafer surface, and thus minimizes contamination. The oxide layer also protects the wafer from chemical impurities, mainly electrically active contaminants. SiOx acts as a hard mask for doping and as an etch stop during patterning. The original gate oxide in MOSFET was made of SiOx. SiOx was also used as the inter-layer dielectric separating different metallization layers, though this is usually a deposited layer. SiO2is also used to prevent induced charge due to the metal layers, this is called afield oxide. In all of these forms, different thickness of the oxide layer are required.

Que 3: State and explain the types of oxidation.

Answer: In the case of grown oxide layers, there are two main growth mechanisms1.Dry oxidation– Si reacts with O2to form SiO2.Si(s) +O2(g)→SiO2(s)(1)2.Wet oxidation– Si reacts with water (steam) to form SiO2.Si(s) + 2H2O(g)→SiO2(s) + 2H2(g)(2)In both cases, Si is supplied by the underlying wafer. Dry and wet oxidation need high temperature (900 - 1200◦C) for growth, though the kinetics are different, which is why this process is called thermal oxidation. Since the underlying Si is consumed, the Si/SiO2interface moves deeper into the wafer. The movement of the interface is shown in figure 1.There is also a volume expansion since the densities of the oxide layer and silicon are different. Thus, the final thickness is higher than the initial Si thickness. Consider the oxide layer silicon interface as shown in figure 2. Here,

d is the thickness of the original Si layer that has been consumed informing the oxide layer of thickness d′. Si has a density of 2.33gcm−3 (ρSi)and an atomic weight of 28.08gmol−1(ZSi) while SiO2has a density of 2.65gcm−3(ρSiO2) and a molecular weight of 60.08gmol−1(ZSiO2). Given that

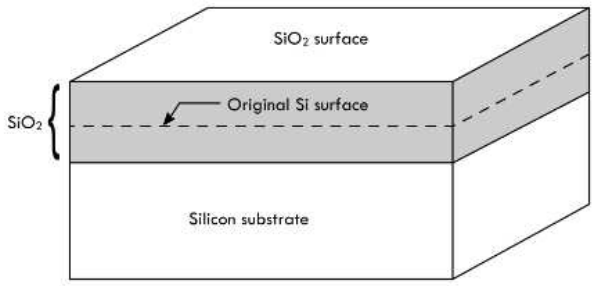


Figure 1: Movement of the silicon-oxide interface as oxide thickness grows. The original thickness of the wafer is marked by dotted lines. The oxide has a higher density, which is why the overall thickness is higher. Adapted from Fundamentals of semiconductor manufacturing and process control -May and Spanos.

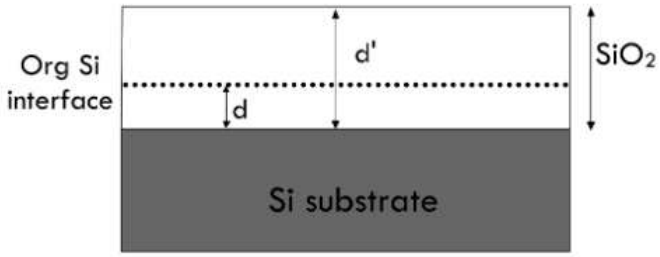


Figure 2: Schematic cross section of the Si oxide interface showing the oxide thickness, d′, and the thickness of Si consumed, d, to form the oxide. The ratio of the thicknesses is inversely proportional to the densities and directly proportional to the atomic/molecular weights.

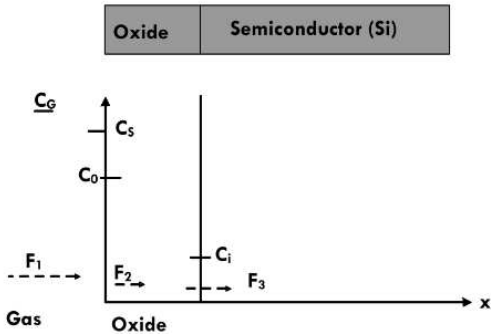


Figure 3: A one dimensional growth model for oxide formation with the fluxes and concentrations marked. There is a certain concentration of the diffusing species, oxygen or steam, in the gas phase, and it is in equilibrium with the concentration in the oxide layer and the oxide-silicon interface.

the cross section area, A, is the same it is possible to use the law of molar conservancy to derive the relation between d and d′. This is given by dAρ Si Z Si=d′AρSiO2ZSiO2(3)Substituting the values in equation 3 gives the relation d′= 1.88d(4)Hence, the thickness of the oxide layer is larger than the thickness of the Si that is consumed to form that oxide. To grow 100nmof oxide, per equation3, 53.2nmof Si needs to be consumed.

Que 4: What is diffusion in fabrication process?

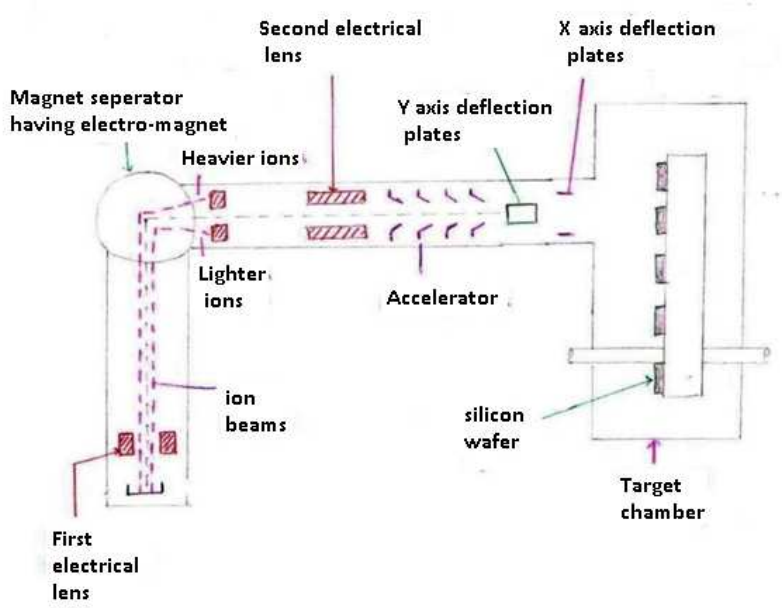
Answer: Diffusion is the movement of impurity atoms in a semiconductor material at high temperatures. The driving force of diffusion is the concentration gradient. There is a wide range of diffusivities for the various dopant species, which depend on how easy the respective dopant impurity can move through the material. Diffusion is applied to anneal the crystal defects after ion implantation or to introduce dopant atoms into silicon from a chemical vapor source. In the last case the diffusion time and temperature determine the depth of dopant penetration. Diffusion is used to form the source, drain, and channel regions in a MOS transistor. But diffusion can also be an unwanted parasitic effect, because it takes place during all high temperature process steps.

Que 5: What is ion implantation?

Answer: Ion implantation is the dominant technique to introduce dopant impurities into crystalline silicon. This is performed with an electric field which accelerates the ionized atoms or molecules so that these particles penetrate into the target material until they come to rest because of interactions with the silicon atoms. Ion implantation is able to control exactly the distribution and dose of the dopants in silicon, because the penetration depth depends on the kinetic energy of the ions which is proportional to the electric field. The dopant dose can be controlled by varying the ion source. Unfortunately, after ion implantation the crystal structure is damaged which implies worse electrical properties. Another problem is that the implanted dopants are electrically

inactive, because they are situated on interstitial sites. Therefore after ion implantation a thermal process step is necessary which repairs the crystal damage and activates the dopants.

Ion implantation is a low-temperature **process** by which **ions** of one element are accelerated into a solid target, thereby changing the physical, chemical, or electrical properties of the target. **Ion implantation** is used in **semiconductor** device **fabrication** and in metal finishing, as well as in materials science research.



- It is defined as the process by which impurity ions are accelerated to high velocity and physically lodged into the target material.
- It is a process by which energetic impurity atoms can be introduced into a single crystal substrate in order to change its electronic properties.
- Dopant atoms are vapourized , accelerated , and directed at silicon substrate.
- They enter the crystal lattice , collide with silicon atoms , and gradually loose energy , finally coming to rest at some depth within the lattice.
- The gas containing the desired impurity is ionized within the ion source.
- The ions are generated and repelled from their source in a diverging beam that is focused by the 1st electrical lens before it passes through a mass separator.
- The 2nd electrical lens focuses this resolved beam which then passes through an accelerator.
- Accelerator brings the ions to their required energy before they strike the target and become implanted in the exposed areas of the silicon wafers.

Advantages:

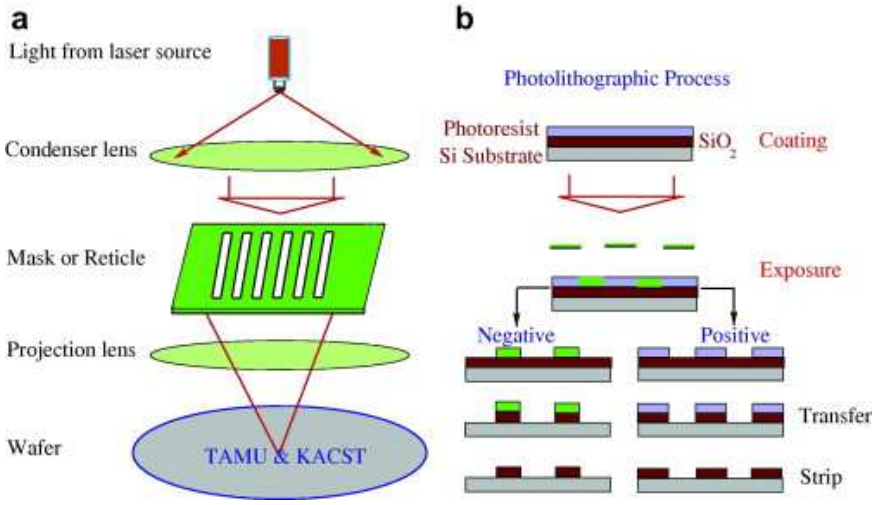
- Mass separation techniques can be used to obtain highly pure form of impurity atoms
- Wide range of dopant doses
- It can be carried out at room temperature
- Provides independent control of dose and penetration depth

Disadvantages:

- Equipments are highly sophisticated and expensive
- Results in damage to conductor
- At high temp , annealing is needed

Que: 6: explain photolithography.

Answer: Lithography is used to transfer a pattern from a photomask to the surface of the wafer. For example the gate area of a MOS transistor is defined by a specific pattern. The pattern information is recorded on a layer of photoresist which is applied on the top of the wafer. The photoresist changes its physical properties when exposed to light (often ultraviolet) or another source of illumination (e.g. X-ray). The photoresist is either developed by (wet or dry) etching or by conversion to volatile compounds through the exposure itself. The pattern defined by the mask is either removed or remained after development, depending if the type of resist is positive or negative. For example the developed photoresist can act as an etching mask for the underlying layers.



Unit 4

Bipolar Junction Transistor and its Configuration

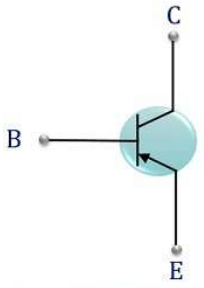
Q1. Explain in detail the construction of pnp transistor.

Solution:
A PNP transistor is an acronym used for a **positive-negative-positive** transistor. It a mainly a classification of bipolar junction transistor and is a three terminal device consisting of the emitter, base and collector.Here, majority charge carriers are holes and hence they are responsible for the flow of current through the device.

In PNP transistor, an n-type semiconductor is fixed between 2 p-type semiconductor material in order to generate a PNP transistor. It is almost similar to another type of BJT i.e., NPN transistor. However, carriers for current conduction and biasing arrangement generates the difference.

PNP transistor is a **current controlled device**. As a small amount of base current is responsible for controlling a large emitter-collector voltage. It is to be noted here that like NPN transistor here also the emitter region is highly doped than the base and collector region.

Symbol of PNP Transistor
The figure below shows the symbolic representation of the PNP transistor:



Symbol of PNP Transistor

Construction of PNP Transistor

A PNP transistor is formed when 2 p-type semiconductors are connected with an n-type semiconductor material. The semiconductor material can be **silicon or germanium**.
The figure below shows the structural arrangement of the PNP transistor having 3 regions:
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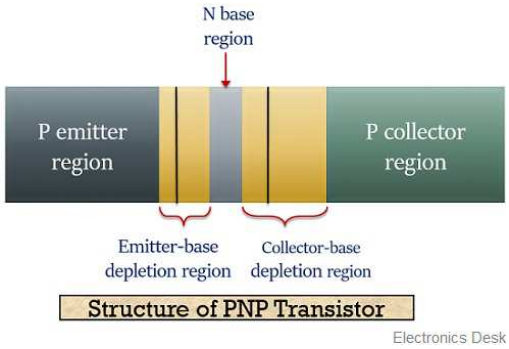
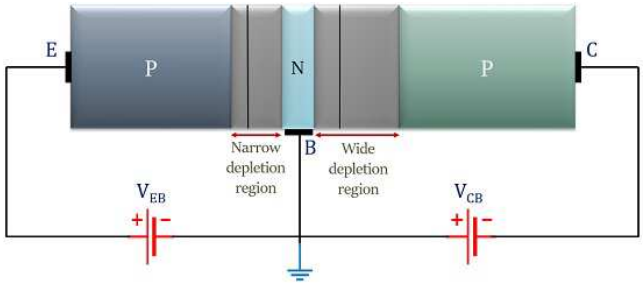


The three regions can be formed by either gaseous diffusion of p-type and n-type impurities on a semiconductor wafer or by an epitaxial method, in which an intrinsic region is grown on the heavily doped substrate of similar material.

Here, the p region is heavily doped than the base and collector region. But the size of the emitter region is greater than the base but comparatively smaller than the collector.

The base region is the thinnest among all and hence least doped. The collector region has the largest area among all but is not doped as high as the emitter.

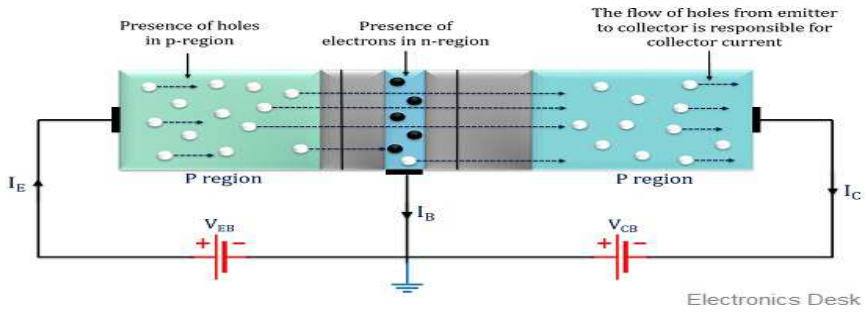
Q2. Explain in detail the working of pnp transistor.



The above figure clearly indicates the emitter-base junction is provided with forward voltage as p region is connected with positive and n region is connected with the negative terminal of the battery.

While the collector-base junction is biased with reverse potential as the p region showing collector is connected with the negative terminal of the battery. This biasing arrangement is necessary so as ensure the operation of the device in the active region.

The biasing arrangement allows current conduction in pnp transistor configuration as shown in figure below:



As the emitter region is highly doped so the majority carriers of the p region i.e., holes get repelled by the forward emitter-base voltage. This positive side of the battery applies a repulsive force to the holes and they get sufficient energy and drift across the emitter-base junction and reaches the base region.

As the base region is not highly doped and consists of electrons as the region majority carriers. Thus, only some of the holes reaching the base region combine with the electrons of the base region. Rest, move towards the collector region.

Also, there exists a depletion region due to the base-collector junction of the transistor. The holes moving with high velocity due to the repulsive force of battery V_{BE} drift across the collector region.

At the same time, the negative terminal of the battery V_{CB} also attracts the positively charged holes. The movement of holes in this way generates a large collector current through the device.

It is to be noted here that the emitter current I_E is a combination of collector current, I_C and base current, I_B. This is so because the combination of some of the holes with the electrons of the base region also gives rise to small base current.

Hence, the current equation is written as:
$I_E = I_B + I_C$

As the base current is very small thus we can say that
$I_E \approx I_C$

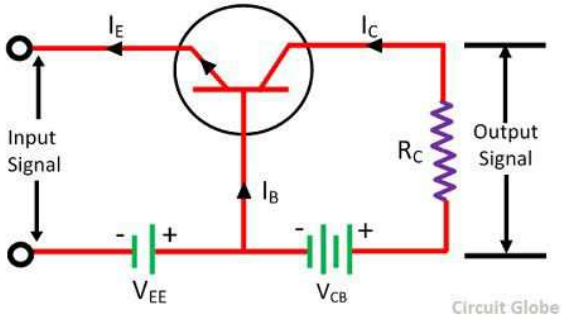
In this way, current is generated by the movement of holes in a PNP transistor. In the operation of the transistor, the efficiency of the emitter and the transport factor plays a vital role.

Q3. Explain how a transistor can used as an amplifier.

Solution:

Transistor as an amplifier:

The transistor raises the strength of a weak signal and hence acts an amplifier. The transistor amplifier circuit is shown in the figure below. The transistor has three terminals namely emitter, base and collector. The emitter and base of the transistor are connected in forward biased and the collector base region is in reverse bias. The forward bias means the P-region of the transistor is connected to the positive terminal of the supply and the negative region is connected to the N-terminal and in reverse bias just opposite of it has occurred.



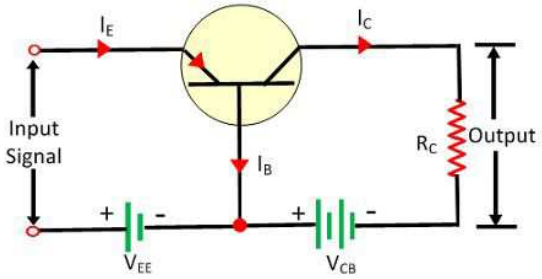
The input signal or weak signal is applied across the emitter base and the output is obtained to the load resistor R_C which is connected in the collector circuit. The DC voltage V_{EE} is applied to the input circuit along with the input signal to achieve the amplification. The DC voltage V_{EE} keeps the emitter-base junction under the forward biased condition regardless of the polarity of the input signal and is known as a bias voltage.

When a weak signal is applied to the input, a small change in signal voltage causes a change in emitter current (or we can say a change of 0.1V in signal voltage causes a change of 1mA in the emitter current) because the input circuit has very low resistance. This change is almost the same in collector current because of the transmitter action.

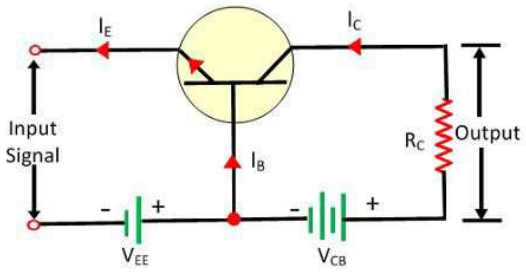
In the collector circuit, a load resistor R_C of high value is connected. When collector current flows through such a high resistance, it produces a large voltage drop across it. Thus, a weak signal (0.1V) applied to the input circuit appears in the amplified form (10V) in the collector circuit.

Q4. Explain the working of transistor in Common Base Configuration with the help of input and output characteristics.

Solution:
The configuration in which the base of the transistor is common between emitter and collector circuit is called a **common base configuration**. The common base circuit arrangement for NPN and PNP transistor is shown in the figure below. In common base-emitter connection, the input is connected between emitter and base while the output is taken across collector and base.



Common Base Connection of PNP Transistor



Common Base Conection of NPN Transistor

Current Amplification factor (α)

The ratio of output current to input current is known as a **current amplification factor**. In the common base configuration, the collector current I_C is the output current, and the emitter current I_E is the input current. Thus, the ratio of change in emitter current to the collector at constant collector-base voltage is known as a current amplification factor of a transistor in common base configuration. It is represented by α (alpha).

$$\alpha = \frac{\Delta I_C}{\Delta I_E}$$

Where ΔI_C is the change in the collector and ΔI_E is changed in emitter current at constant V_{CB}. Now,

$$I_E = I_C + I_B$$

$$\Delta I_E = \Delta I_C + \Delta I_B$$

$$\frac{\Delta I_E}{\Delta I_E} = \frac{\Delta I_C}{\Delta I_E} + \frac{\Delta I_B}{\Delta I_E}$$

$$1 = \alpha + \frac{\Delta I_B}{\Delta I_E}$$

$$\alpha = 1 - \frac{\Delta I_B}{\Delta I_E}$$

The value of current amplification factor is less than unity. The value of the amplification factor (α) reaches to unity when the base current reduces to zero.

The base current becomes zero only when it is thin and lightly doped. The practical value of the amplification factor varies from 0.95 to 0.99 in the commercial transistor.

Collector Current:

The base current is because of the recombination of the electrons and holes in the base region. The whole emitter current will not flow through the current. The collector current increase slightly because of the leakage current flows due to the minority charge carrier. The total collector current consists;

1. The large percentage of emitter current that reaches the collector terminal, i.e., αI_E.
2. The leakage current Ileakage. The minority charge carrier is because of the flow of minority charge carrier across the collector-base junction as the junction is heavily reversed. Its value is much smaller than αI_E.

Total collector current,

$$I_C = \alpha I_E + I_{leakage}$$

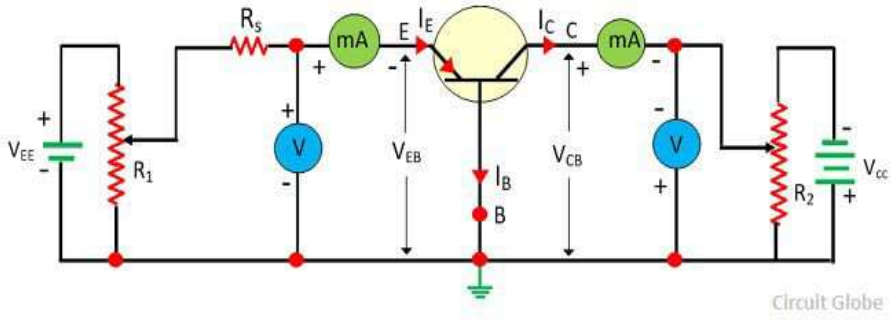
The above expression shows that if $I_E = 0$ (when the emitter circuit is open) then still a small current flow in the collector circuit called leakage current. This leakage current is represented by as I_{CBO}, i.e., collector-base current with emitter circuit is open.

$$I_C = \alpha I_E + I_{CBO}$$

The leakage current is also abbreviated as I_{CO} i.e., the collector current with emitter circuit open.

Characteristics of Common Base (CB) Configuration

The characteristic diagram of determining the common base characteristic is shown in the figure below.

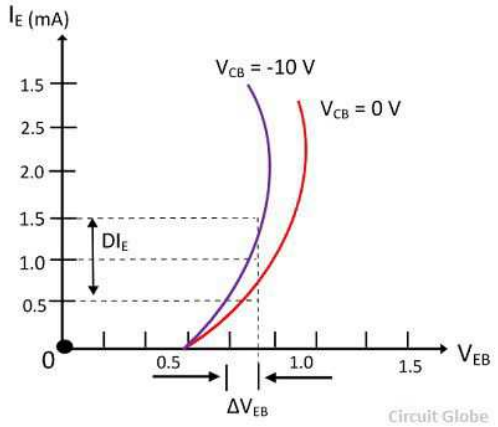


The emitter to base voltage V_{EB} can be varied by adjusting the potentiometer R_1. A series resistor R_S is inserted in the emitter circuit to limit the emitter

current I_E. The value of the emitter change to a large value even the value of a potentiometer slightly changes. The value of collector voltage changes slightly by changing the value of the potentiometer R_2. The input and output characteristic curve of the potentiometer explains below in details.

Input Characteristic:

The curve plotted between emitter current I_E and the emitter-base voltage V_{EB} at constant collector base voltage V_{CB} is called input characteristic curve. The input characteristic curve is shown in the figure below.

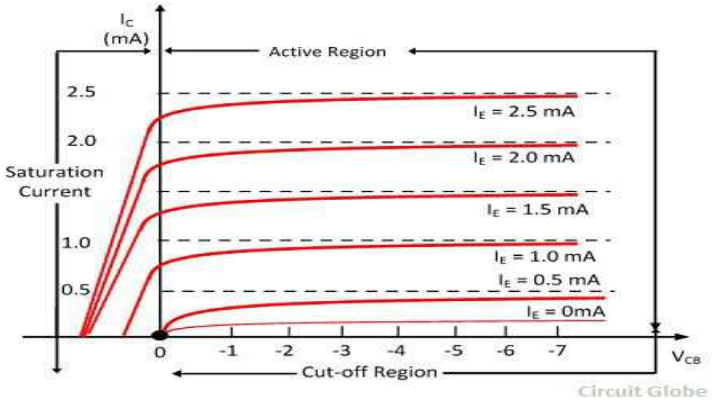


The following points are taken into consideration from the characteristic curve.

1. For a specific value of V_{CB}, the curve is a diode characteristic in the forward region. The PN emitter junction is forward biased.
2. When the value of the voltage base current increases the value of emitter current increases slightly. The junction behaves like a better diode. The emitter and collector current is independent of the collector base voltage V_{CB}.
3. The emitter current I_E increases with the small increase in emitter-base voltage V_{EB}. It shows that input resistance is small.

Output Characteristic Curve:

In common base configuration, the curve plotted between the collector current and collector base voltage V_{CB} at constant emitter current I_E is called output characteristic. The CB configuration of PNP transistor is shown in the figure below.



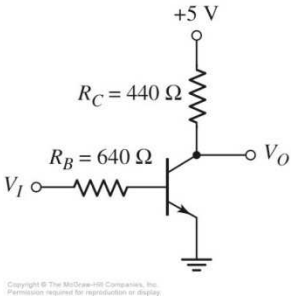
The following points from the characteristic curve are taken into consideration.

1. The active region of the collector-base junction is reverse biased, the collector current I_C is almost equal to the emitter current I_E. The transistor is always operated in this region.
2. The curve of the active regions is almost flat. The large charges in V_{CB} produce only a tiny change in I_C The circuit has very high output resistance ro.
3. When V_{CB} is positive, the collector-base junction is forward bias and the collector current decrease suddenly. This is the saturation state in which the collector current does not depend on the emitter current.
4. When the emitter current is zero, the collector current is not zero. The current which flows through the circuit is the reverse leakage current, i.e., I_{CBO}. The current is temperature depends and its value range from 0.1 to 1.0 μA for silicon transistor and 2 to 5 μA for germanium transistor.

Numerical:

1. For the circuit shown in Figure 1, assume β= 50, $V_{BE(on)}$ = 0.7 V and $V_{CE(sat)}$ = 0.2 V. Determine V_O, I_B, and $I_C$for: (a) V_I= 0.2 V, and (b) V_I= 3.6 V. Then calculate the power dissipated in the transistor for the two conditions. (c) Determine $V_I$such that V_{BC}= 0. Calculate the power dissipated in the transistor under suchcondition.

Figure 1



Solution:
(a) V_I= 0.2 V:

Since $V_I < V_{BE(on)}$ the transistor is biased in the cut-off region. Therefore I_B= I_C= 0, V_O= 5 V and the power dissipated in the transistor P = 0.

(b) V_I= 3.6V:
Assume that the transistor is initially biased in the forward-active region,

$$I_B = \frac{V_I - V_{BE(on)}}{R_B} = \frac{3.6 - 0.7}{640} = 4.53\ (\text{mA})$$

$$I_C = \beta I_B = 50(4.53) = 226.56\ (\text{mA})$$

$$V_{CE} = V_{CC} - I_C R_C = 5 - 99.69 = -94.69\ (\text{V})$$

Therefore the initial assumption is incorrect. The transistor is actually biased in the saturation region. Hence:

$$I_B = \frac{V_I - V_{BE(on)}}{R_B} = \frac{3.6 - 0.7}{640} = 4.53\ (\text{mA})$$

$$I_C = \frac{V_{CC} - V_{CE(sat)}}{R_C} = \frac{5 - 0.2}{440} = 10.91\ (\text{mA})$$

$$V_O = V_{CE(sat)} = 0.2\ (\text{V})$$

$$P = V_{CE(sat)} I_C + V_{BE(on)} I_B = 0.2(10.91) + 0.7(4.53) = 5.35\ (\text{mW})$$

(c) When V_{BC}=0,

$$V_O = V_{BE(\text{on})} = 0.7 \text{ (V)}$$

$$I_C = \frac{V_{CC} - V_O}{R_C} = \frac{5 - 0.7}{440} = 9.77 \text{ (mA)}$$

This is the boundary condition between the transistor's saturation and forward-active region. If V_{BC}> 0 the base-collector junction will be forward-biased and the transistor will enter the saturation region. Conversely, if V_{BC}< 0 the base-collector junction will be reversed biased and the transistor will enter the forward-active region. At the boundary condition, $I_C = \beta I_B$ is still valid, and the maximum V_I which can be applied to the base before the transistor is biased into saturation can be found by:

$$I_B = \frac{I_C}{\beta} = \frac{9.77}{50} = 195.45 \ (\mu\text{A})$$

$$= \frac{V_{I(\max)} - V_{BE(\text{on})}}{R_B}$$

$$\Rightarrow$$

$$V_{I(\max)} = 0.825 \text{ (V)}$$

$$P = V_{CE} I_C + V_{BE(\text{on})} I_B = 6.98 \text{ (mW)}$$

2. For the circuit shown in Figure 2, the measured value of V_C is V_C= +6.34 V. Determine I_B, I_E, I_C, V_{CE}, β, and α. Assume $V_{BE(\text{on})}$ = 0.7V.

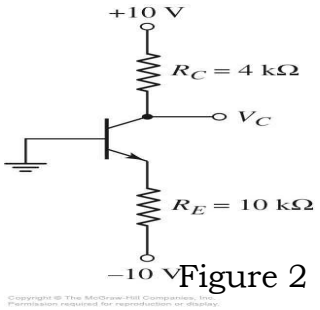


Figure 2

Solution:

Since V_{BC}= V_B-V_C= -6.34 V < 0, the transistor is biased in the forward-active mode. Other circuit parameters can be calculated as:

$$I_C = \frac{V_{CC} - V_C}{R_C} = \frac{10 - 6.34}{4000} = 0.915 \text{ (mA)}$$

$$I_E = \frac{V_B - V_{BE(on)} - (-V_{CC})}{R_E} = \frac{0 - 0.7 - (-10)}{10000} = 0.930 \text{ (mA)}$$

$$\alpha = \frac{I_C}{I_E} = \frac{0.915}{0.930} = 0.9838$$

$$\beta = \frac{\alpha}{1-\alpha} = 61$$

$$I_B = \frac{I_C}{\beta} = 15 \ (\mu A)$$

$$V_{CE} = V_C - V_E = 6.34 - (-0.7) = 7.04 \text{ (V)}$$

3. Design the common-base circuit shown in Figure 3 such that I_{EQ} = 0.50 mA and V_{ECQ} = 4.0 V. Assume transistor parameters of β = 120 and $V_{EB(on)}$ = 0.7 V.

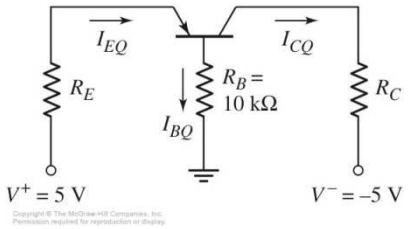


Figure 3

Solution:

From Figure 3, the following equations can be written:

$$V^+ = I_{EQ}R_E + I_{BQ}R_B + V_{EB} \qquad ...(1)$$

$$V^+ - V^- = V_{ECQ} + I_{EQ}R_E + I_{CQ}R_C \qquad ...(2)$$

From(1):

$$V^+ = I_{EQ}R_E + I_{BQ}R_B + V_{EB(on)}$$

$$= I_{EQ}R_E + \left(\frac{I_{EQ}}{1+\beta}\right) \cdot R_B + V_{EB(on)}$$

$$= \left[R_E + \frac{R_B}{1+\beta}\right] \cdot I_{EQ} + V_{EB(on)}$$

$$5 = \left(R_E + \frac{10}{121}\right) \cdot (0.5) + 0.7$$

$$\Rightarrow R_E = 8.52 \text{ (k}\Omega\text{)}$$

From(2):

$$V^+ - V^- = V_{ECQ} + I_{EQ}R_E + I_{CQ}R_C$$

$$= V_{ECQ} + I_{EQ}R_E + \left(\frac{\beta}{1+\beta}\right)\cdot I_{EQ}R_C$$

$$= V_{ECQ} + \left[R_E + \left(\frac{\beta}{1+\beta}\right)\cdot R_C\right] I_{EQ}$$

$$10 = 4 + \left[8.5174 + \left(\frac{120}{121}\right)\cdot R_C\right](0.5)$$

$$\Rightarrow R_C = 3.51\ (\text{k}\Omega)$$

4. The circuit shown in Figure 4 is to be designed such that I_{CQ} = 0.8 mA and V_{CEQ} = 2 V for the case when (a) R_E = 0 and (b) R_E = 1 kΩ. Assume β = 80 and $V_{BE(on)}$ = 0.7 V. The transistor in Figure 4 is replaced with one with a value of β = 120 and β = 150. Calculate the new Q-point values I_{CQ} and V_{CEQ} for each case. Which design (R_E = 0 or R_E = 1 kΩ) shows a smaller change in Q-point values when β changes? What can you conclude about the advantage of adding R_E?

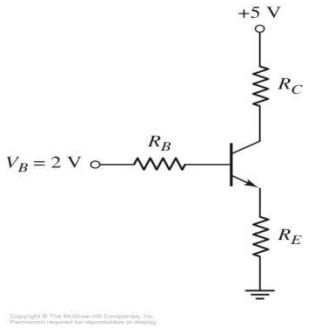


Figure 4

Solution:
The circuit is to be designed with I_{CQ}= 0.8 mA and V_{CEQ}= 2 V.
Let β= 80 and R_E= 0,

$$V_B = I_{BQ}R_B + V_{BE(on)} = \frac{I_{CQ}}{\beta}\cdot R_B + V_{BE(on)}$$

$$2 = \frac{0.8}{80}\cdot R_B + 0.7$$

$$\Rightarrow R_B = 130\ (\text{k}\Omega)$$

$$V_{CC} = I_{CQ}R_C + V_{CEQ}$$

$$5 = 0.8\cdot R_C + 2$$

$$\Rightarrow R_C = 3.75\ (\text{k}\Omega)$$

If R_E= 1 kΩ is present, R_B and R_C are re-calculated as:

$$V_B = I_{BQ}R_B + V_{BE(on)} + I_{EQ}R_E = \frac{I_{CQ}}{\beta}\cdot R_B + V_{BE(on)} + \frac{I_{CQ}}{\alpha}\cdot R_E$$

$$2 = \frac{0.8}{80}\cdot R_B + 0.7 + \left(\frac{0.8}{0.9877}\right)(1)$$

$$\Rightarrow R_B = 49\ (\text{k}\Omega)$$

$$V_{CC} = I_{CQ}R_C + V_{CEQ} + I_{EQ}R_E$$

$$5 = 0.8\cdot R_C + 2 + \left(\frac{0.8}{0.9877}\right)(1)$$

$$\Rightarrow R_C = 2.74\ (\text{k}\Omega)$$

	R_E= 0 (R_B= 130 kΩ, R_C= 3.75 kΩ)	**R_E= 1 kΩ (R_B= 49 kΩ, R_C= 2.74 kΩ)**
β= 80	**I_{CQ}= 0.8mA** **V_{CEQ}= 2.0V**	I_{CQ}= 0.8mA V_{CEQ}= 2.0V
β= 120	**I_{CQ}= 1.2mA** **V_{CEQ}= 0.5V**	I_{CQ}= 0.92mA V_{CEQ}= 1.56V
β= 150	I_{CQ}= 1.5 mA V_{CEQ}= -0.625 V	I_{CQ}= 0.98mA V_{CEQ}= 1.35V

From the tabulated results, with the addition of the emitter resistor R_E, the *Q*-point values become less sensitive to the variation in the current gain β hence a more stable dc design is achievable. Referring to the circuit with R_E,

$$V_B = I_{BQ}R_B + V_{BE(on)} + I_{EQ}R_E$$

$$= I_{BQ}R_B + V_{BE(on)} + (1+\beta)\cdot I_{BQ}R_E$$

$$\Rightarrow I_B = \frac{V_B - V_{BE(on)}}{R_B + (1+\beta)\cdot R_E}$$

$$I_C = \beta\cdot I_B = \frac{\beta\cdot(V_B - V_{BE(on)})}{R_B + (1+\beta)\cdot R_E}$$

$$\approx \frac{V_B - V_{BE(on)}}{R_E}\ \ (\text{if } R_B << (1+\beta)\cdot R_E \text{ and } \beta >> 1)$$

Therefore if R_E is chosen such that $(1 + \beta)R_E$ is much larger than R_B, e.g. $(1 + \beta)R_E = 10R_B$, the quiescent collector current I_C becomes a function of R_E only and

is not affected by the variation in β. It is a common practice to add this resistor in practical circuit design.

5. The circuit shown in Figure 5 is to be designed such that I_{CQ} = 0.5 mA and V_{CEQ} = 2.5 V. Assume β = 120 and $V_{BE(on)}$ = 0.7 V. Sketch the load line and mark the Q-point. If the resistor values vary by ± 10 %, Calculate the maximum and minimum values of R_B and R_C (four Q-point values).

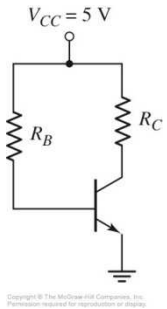


Figure 5

Solution:

The circuit is to be designed with I_{CQ} = 0.5 mA and V_{CEQ} = 2.5 V.

Let β = 120,

$$V_{CC} = I_{BQ}R_B + V_{BE(on)} = \frac{I_{cQ}}{\beta}R_B + V_{BE(on)}$$

$$5 = \frac{0.5}{120}\cdot R_B + 0.7$$

$$\Rightarrow R_B = 1.032\ (\text{M}\Omega)$$

$$V_{CC} = I_{CQ}R_C + V_{CEQ}$$

$$5 = (0.5)\cdot R_C + 2.5$$

$$\Rightarrow R_C = 5\ (\text{k}\Omega)$$

Since both resistors have a tolerance of ± 10 %, the base resistor can vary between 928.8 kΩ≤ RB ≤ 1135.2 kΩ and the collector resistor between 4.5 kΩ≤ RC ≤ 5.5 kΩ. For extreme values of R_B and R_C,the Q-point values are computed as follows:

	R_C= 4.5 kΩ	**R_C= 5.5 kΩ**
R_B= 928.8 kΩ	I_{CQ}= 0.556 mA V_{CEQ}= 2.5 V	I_{CQ}= 0.556 mA V_{CEQ}= 1.94 V
R_B= 1135.2 kΩ	I_{CQ}= 0.455 mA V_{CEQ}= 2.95 V	I_{CQ}= 0.455 mA V_{CEQ}= 2.5 V

UNIT 5:
MOSFET and its Configuration

Q1. Explain the construction of MOSFET with the help of diagram. Also give the classification of MOSFET.

Solution:

MOSFET stands for Metal Oxide Silicon Field Effect Transistor or Metal Oxide Semiconductor Field Effect Transistor. This is also called as IGFET meaning Insulated Gate Field Effect Transistor. The FET is operated in both depletion and enhancement modes of operation.

Construction of a MOSFET

The construction of a MOSFET is a bit similar to the FET. An oxide layer is deposited on the substrate to which the gate terminal is connected. This oxide layer acts as an insulator (sio_2 insulates from the substrate), and hence the MOSFET has another name as IGFET. In the construction of MOSFET, a lightly doped substrate, is diffused with a heavily doped region. Depending upon the substrate used, they are called as **P-type** and **N-type** MOSFETs.

The following figure 1 shows the construction of a MOSFET.

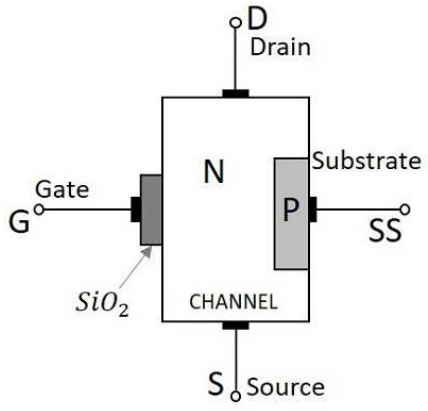


Figure 1

The voltage at gate controls the operation of the MOSFET. In this case, both positive and negative voltages can be applied on the gate as it is insulated from the channel. With negative gate bias voltage, it acts as **depletion MOSFET** while with positive gate bias voltage it acts as an **Enhancement MOSFET**.

Classification of MOSFET

MOSFET can be classified as Enhancement MOSFET and Depletion MOSFET as shown in Figure 2

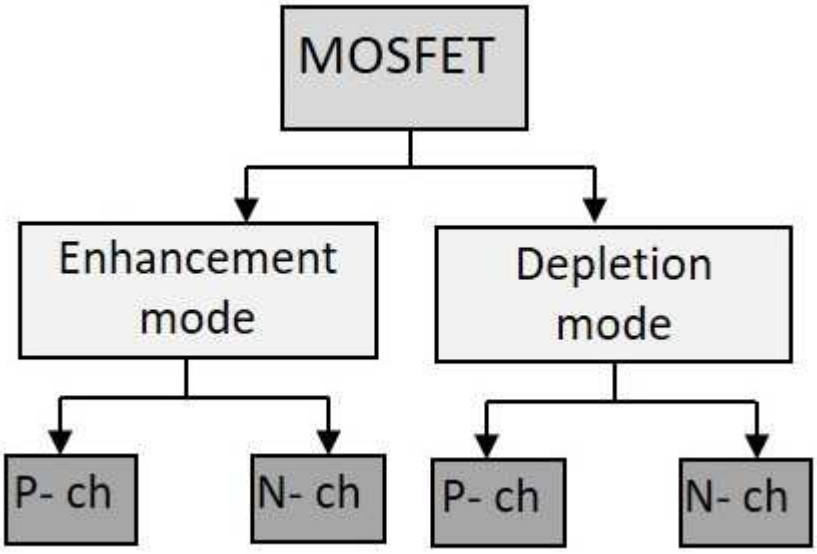
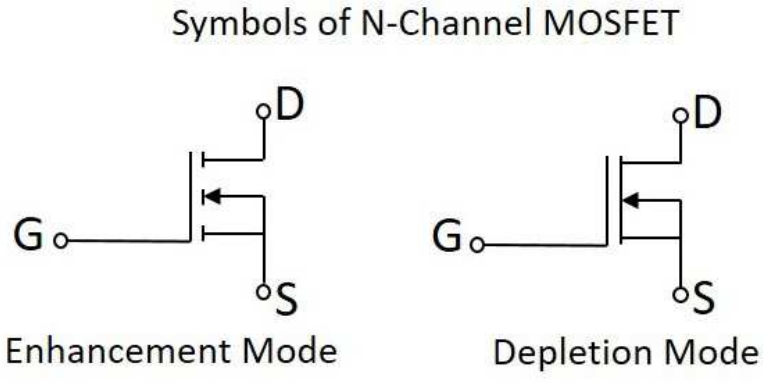


Figure 2

Q2: Explain the construction and working principle of N-Channel MOSFET in depletion mode with the help of neat diagram.

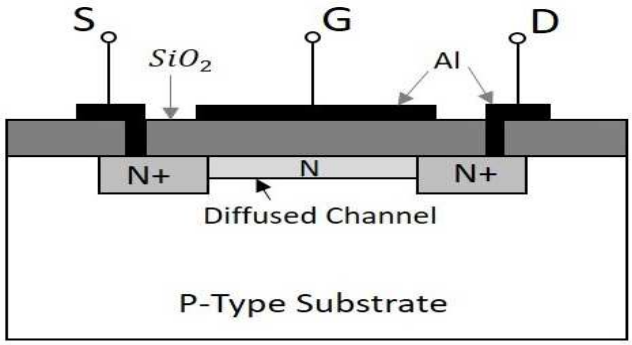
Solution:

The N-channel MOSFETs are simply called as NMOS. The symbols for N-channel MOSFET are as given below.



Construction of N- Channel MOSFET

Let us consider an N-channel MOSFET. A lightly doped P-type substrate is taken into which two heavily doped N-type regions are diffused, which act as source and drain. Between these two N+ regions, there occurs diffusion to form an N-channel, connecting drain and source. The structure of N-Channel MOSFET is as shown in figure 3 below.



Structure of N-channel MOSFET

Figure 3

A thin layer of Silicon dioxide (SiO_2) is grown over the entire surface and holes are made to draw ohmic contacts for drain and source terminals. A conducting layer of aluminum is laid over the entire channel, upon this SiO_2 layer from source to drain which constitutes the gate. The SiO_2 substrate is connected to the common or ground terminals.

Because of its construction, the MOSFET has a very less chip area than BJT, which is 5% of the occupancy when compared to bipolar junction transistor. This device can be operated in modes. They are depletion and enhancement modes.

Working of N - Channel depletionmodeMOSFET:

There is no PN junction present between gate and channel in N-Channel MOSFET, unlike a FET. The diffused channel N betweentwoN+regions, the insulating dielectric SiO_2 and the aluminum metal layer of the gate together form a parallel plate capacitor.

If the NMOS has to be worked in depletion mode, the gate terminal should be at negative potential while drain is at positive potential, as shown in the following figure 4.

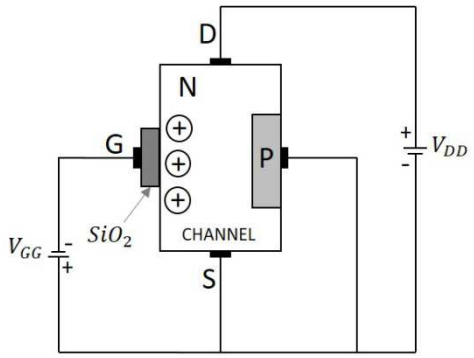


Figure 4

When no voltage is applied between gate and source, some current flows due to the voltage between drain and source. Let some negative voltage is applied at V_{GG}. Then the minority carriers i.e. holes, get attracted and settle near SiO_2 layer. But the majority carriers, i.e., electrons get repelled.

With some amount of negative potential at V_{GG} a certain amount of drain current I_D flows through source to drain. When this negative potential is further increased, the electrons get depleted and the current I_D decreases. Hence the more negative the applied V_{GG}, the lesser the value of drain current I_D will be.

The channel nearer to drain gets more depleted than at source and the current flow decreases due to this effect. Hence it is called as depletion mode MOSFET.

Q3: Explain the working principle of N-Channel MOSFET in Enhancement mode with the help of neat diagram.

Solution:

Working of N-Channel MOSFET Enhancement Mode

The same MOSFET can be worked in enhancement mode, if we can change the polarities of the voltage V_{GG}. So, let us consider the MOSFET with gate source voltage V_{GG} being positive as shown in the following figure 5.

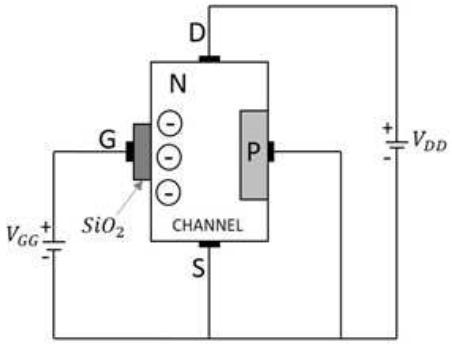


Figure 5

When no voltage is applied between gate and source, some current flows due to the voltage between drain and source. Let some positive voltage is applied at V_{GG}. Then the minority carriers i.e. holes, get repelled and the majority carriers i.e. electrons gets attracted towards the SiO_2 layer.

With some amount of positive potential at V_{GG} a certain amount of drain current I_D flows through source to drain. When this positive potential is further increased, the current I_D increases due to the flow of electrons from source and these are pushed further due to the voltage applied at V_{GG}. Hence the more positive the applied V_{GG}, the more the value of drain current I_D will be. The current flow gets enhanced due to the increase in electron flow better than in depletion mode. Hence this mode is termed as Enhanced Mode MOSFET.

Q4: Explain the construction and working principle of P-Channel MOSFET in depletion mode with the help drain and transfer characteristics.

Solution:

A lightly doped n-substrate is taken into which two heavily doped P+ regions are diffused. These two P+ regions act as source and drain. A thin layer of SiO2 is grown over the surface. Holes are cut through this layer to make contacts with P+ regions, as shown in the following figure 6.

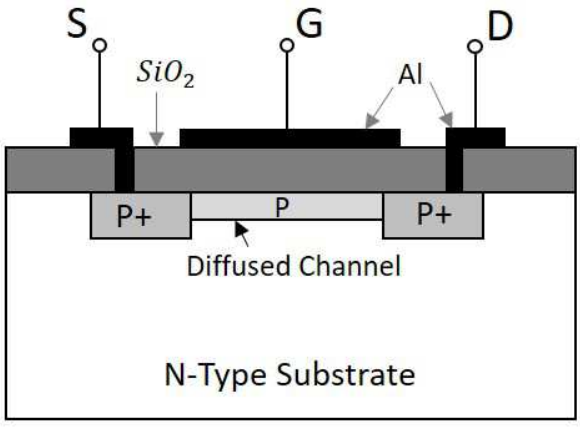


Figure 6

Working of PMOS

When the gate terminal is given a negative potential at $\mathbf{V_{GG}}$ than the drain source voltage $\mathbf{V_{DD}}$, then due to the P+ regions present, the hole current is increased through the diffused P channel and the PMOS works in **Enhancement Mode**.

When the gate terminal is given a positive potential at $\mathbf{V_{GG}}$ than the drain source voltage $\mathbf{V_{DD}}$, then due to the repulsion, the depletion occurs due to

which the flow of current reduces. Thus PMOS works in **Depletion Mode**. Though the construction differs, the working is similar in both the type of MOSFETs. Hence with the change in voltage polarity both of the types can be used in both the modes.

Drain Characteristics:

The drain characteristics of a MOSFET are drawn between the drain current ID and the drain source voltage VDS. The characteristic curve is as shown in figure 7 below for different values of inputs.

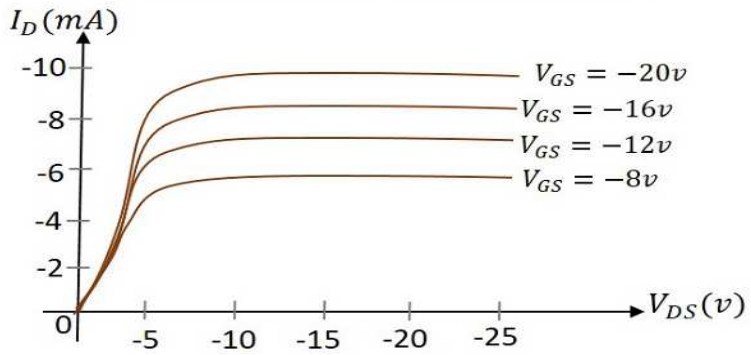


Figure 7

Actually when **V_{DS}** is increased, the drain current **I_D** should increase, but due to the applied **V_{GS}**, the drain current is controlled at certain level. Hence the gate current controls the output drain current.

Transfer Characteristics

Transfer characteristics define the change in the value of **V_{DS}** with the change in **I_D** and **V_{GS}** in both depletion and enhancement modes. The below transfer characteristic curve as shown in figure 8 is drawn for drain current versus gate to source voltage.

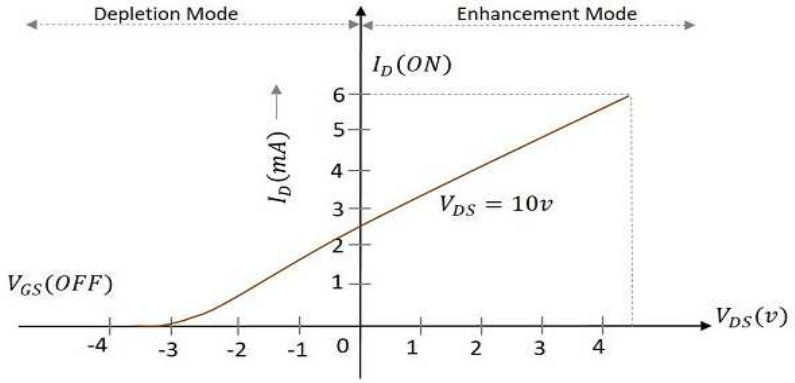


Figure 8

Q5: Explain how Common Source MOSFET can be used an amplifier.

Solution:

If we apply a small time-varying signal to the input, then under the right circumstances the MOSFET circuit can act as a linear amplifier providing the transistors Q-point is somewhere near the center of the saturation region, and the input signal is small enough for the output to remain linear. Consider the basic MOSFET amplifier circuit as shown in figure 9 below.

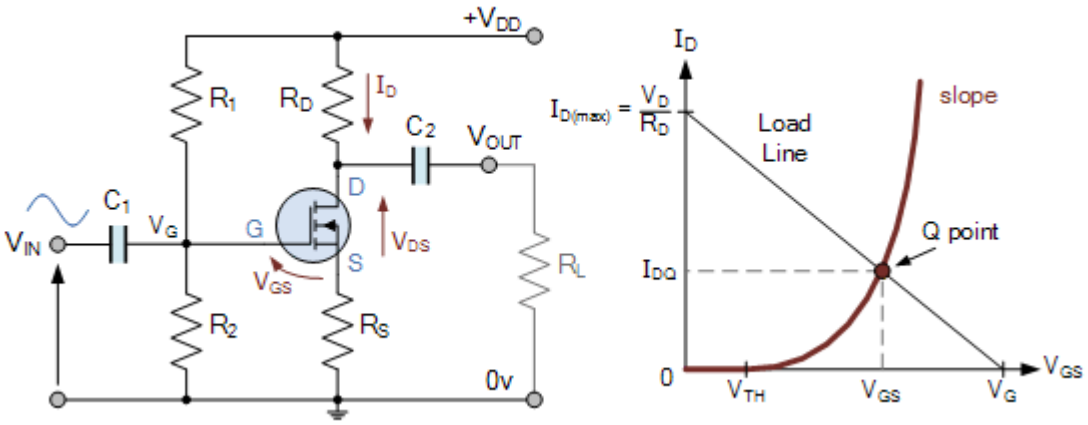


Figure 9: Basic CS MOSFET amplifier and I_DVs V_{GS} Characteristics

Following are the basic assumptions about the MOSFET amplifiers DC operating conditions.

$$V_{DD} = I_D R_D + V_{DS} + I_D R_S$$
$$= I_D(R_D+R_S) + V_{DS}$$

Therefore $$R_D + R_S = (V_{DD} – V_{DS}) / I_D$$

And the MOSFET Gate – to – Source Voltage is given as:

$$V_{GS} = V_G – I_S R_S$$
$$= V_G - I_D R_S$$

For proper operation of the MOSFET, this gate-source voltage must be greater than the threshold voltage of the MOSFET, that is $V_{GS} > V_{TH}$. Since $I_S = I_D$, the gate voltage, V_G is therefore equal too:

$$V_{GS}= V_G - I_D R_S$$

$$V_G = V_{GS}+ I_D R_S$$

$$\text{or} V_G = V_{GS} + V_S$$

To set the MOSFET amplifier gate voltage to this value we select the values of the resistors, R_1 and R_2 within the voltage divider network to the correct values. As we know from above, "no current" flows into the gate terminal of a MOSFET device so the formula for voltage division is given as:

$$V_G = V_{DD} (R_2 / (R_1+R_2))$$

Q6: Explain how an MOSFET can be used as an Switch.

Solution:
MOSFETs exhibit three regions of operation viz., Cut-off, Linear or Ohmic and Saturation. Among these, when MOSFETs are to be used as amplifiers, they are required to be operated in their Ohmic region wherein the current through the device increases with an increase in the applied voltage. On the other hand, when the MOSFETs are required to function as switches, they should be biased in such a way that they alter between cut-off and saturation states. This is because, in cut-off region, there is no current flow through the device while in saturation region there will be a constant amount of current flowing through the device, just mimicking the behavior of an open and closed switch, respectively.

Figure 10 shows a simple circuit which uses an n-channel enhancement **MOSFET as a switch**. Here the drain terminal (D) of the **MOSFET** is connected to the supply voltage V_S via the drain resistor R_D while its source terminal (S) is grounded. Further, it has an input voltageVi applied at its gate terminal (G) while the output Vo is drawn from its drain.

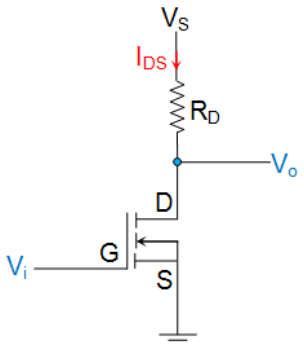


Figure 10

Consider the case where Vi applied is 0V, which means the gate terminal of the MOSFETis left unbiased. As a result, the MOSFET will be OFF and operates in its cutoff region wherein it offers a high impedance path to the flow of current which makes the I_{DS} almost equivalent to zero. As a result, even the voltage drop across R_D will become zero due to which the output voltage V_o will become almost equal to V_S.

Consider the case where the input voltage Vi applied is greater than the threshold voltage V_T of the device. Under this condition, the MOSFET will start to conduct and if the VS provided is greater than the pinch-off voltage V_P of the device (usually it will be so), then the MOSFET starts to operate in its saturation region. This further means that the device will offer low resistance path for the flow of constant I_{DS}, almost acting like a short circuit. As a result, the output voltage will be pulled towards low voltage level, which will be ideally zero.

Therefore it is clear that the output voltage alters between V_S and zero depending on whether the input provided is less than or greater than V_T, respectively. Thus, it can be concluded that MOSFETs can be made to function as electronic switches when made to operate between cut-off and saturation operating regions.

Q7: Explain the construction and working principle of P-Channel MOSFET in Enhancement mode with the help of neat diagram.

Solution:

p channel MOSFETis also popularly known as PMOS. Here, a substrate of lightly doped n-type semiconductor, usually a silicon or gallium arsenide semiconductor material, forms the main body of the device. Two heavily doped p-type regions are there in the body separated by a certain distance L. We refer this distance L as channel length and it is in order of 1 μm. The structure of P-channel MOSFET is as shown in figure 11.

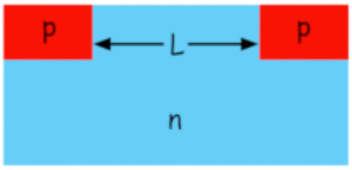


Figure 11

Now there is a thin layer of silicon dioxide (SiO2) on the top of the substrate as shown in figure 12. This layer on the substrate behaves as a dielectric. There is an aluminum plate fitted on the top of this SiO2 dielectric layer.The aluminum plate, dielectric and semiconductor substrate form a capacitor on the device.

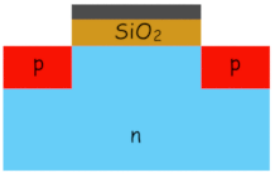


Figure 12

The terminals connected to two p-type regions are the source (S) and drain (D) of the device respectively. The terminal projected from the aluminum plate of the capacitor is gate (G) of the device as shown in figure 13.

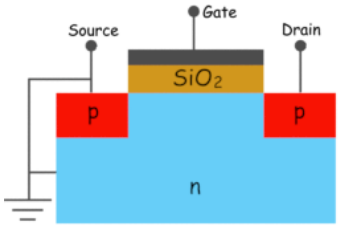


Figure 13

Apply a negative voltage at gate (G) as shown in figure 14 below. This will create negative static potential at the aluminum plate of the capacitor. Due to capacitive action, positive charge gets accumulated just below the dielectric layer.

Basically, the free electrons of that portion of the n-type substrate get shifted away due to the repulsion of negative gate plate and consequently layers of uncovered positive ions appear here. Now if we further increase the negative voltage at the gate terminal, after a certain voltage called threshold voltage, due to the electrostatic force, covalent bonds of the crystal just below the SiO_2 layer start breaking. Consequently, electron-hole pairs get generated there. The holes get attracted and free electrons get repealed due to the negativity of the gate. In this way, the concentration of holes increases there and create a channel of holes from source to drain region. Due to the concentration of holes in that channel the channel becomes conductive in nature through which electric current can pass.

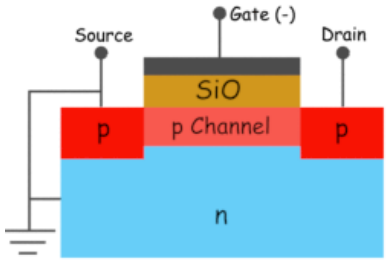


Figure 14

Apply a negative voltage at drain terminal. The negative voltage in the drain region reduces the voltage difference between gate and drain, as a result, the width of the conductive channel get reduced toward the drain region as shown in figure 15 below. At the same time, current flows from source to drain shown by arrowhead.

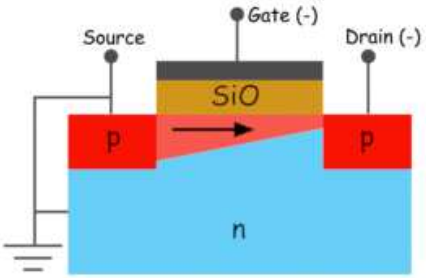


Figure 15

The channel created in the MOSFET offers a resistance to the current from source to drain. The resistance of the channel depends on the cross-section of the channel and the cross section of the channel again depends on the applied negative gate voltage. So we can control the current from the source to drain with the help of an applied gate voltage hence MOSFET is a voltage controlled electronic device. As the concentration of holes forms the channel, and the current through the channel gets enhanced due to increase in negative gate voltage, the MOSFET is called as P – Channel Enhancement MOSFET.

Q8: Draw and Explain V-I characteristics of N-Channel Enhancement MOSFET.

Solution:
Figure 16 (a) shows the transfer characteristics (drain-to-source current I_{DS} versus gate-to-source voltage V_{GS}) of **n-channel Enhancement-type MOSFETs**. From this, it is clear that the current through the device will be zero until the V_{GS} exceeds the value of threshold voltage V_T. This is because under this state, the device will be void of channel which will be connecting the drain and the source terminals. Under this condition, even an increase in V_{DS} will result in no current flow as indicated by the corresponding output characteristics (I_{DS} versus V_{DS}) shown by Figure 16 (b). As a result this state represents nothing but the cut-off region of MOSFET's operation.

Once V_{GS} crosses V_T, the current through the device increases with an increase in I_{DS} initially (Ohmic region) and then saturates to a value as determined by the V_{GS} (saturation region of operation) i.e. as V_{GS} increases, even the saturation current flowing through the device also increases. This is evident by Figure 16 (b) where I_{DSS2} is greater than I_{DSS1} as $V_{GS2} > V_{GS1}$, I_{DSS3} is greater than I_{DSS2} as $V_{GS3} > V_{GS2}$, so on and so forth. Further, Figure 16 (b) also shows the locus of pinch-off voltage (black discontinuous curve), from which V_P is seen to increase with an increase in V_{GS}.

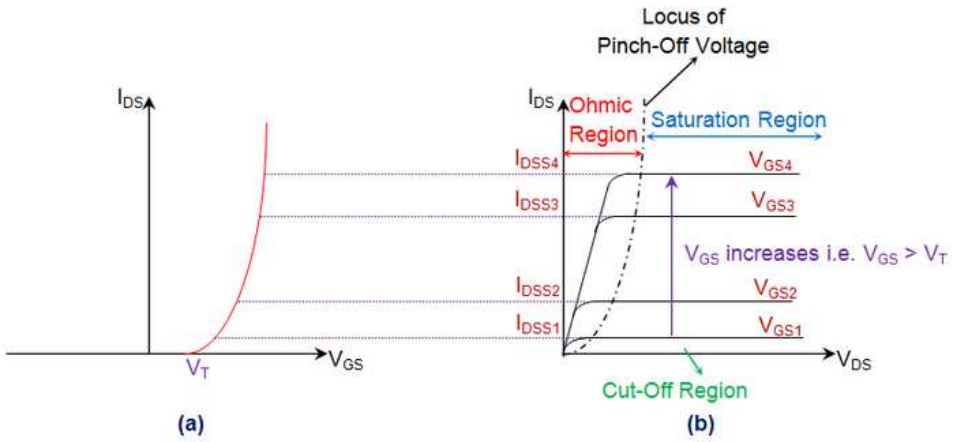


Figure 16: N- Channel Enhancement MOSFET
(a) Transfer Characteristics (b) Output Characteristics

Q9: Draw and Explain V-I characteristics of P -Channel Enhancement MOSFET.

Solution:

Figure 17(a) shows the transfer characteristics of p-type enhancement MOSFETs from which it is evident that I_{DS} remains zero (cutoff state) untill V_{GS} becomes equal to $-V_T$. This is because, only then the channel will be formed to connect the drain terminal of the device with its source terminal. After this, the I_{DS} is seen to increase in reverse direction (meaning an increase in I_{SD}, signifying an increase in the device current which will flow from source to drain) with the decrease in the value of V_{DS}. This means that the device is functioning in its ohmic region wherein the current through the device increases with an increase in the applied voltage (which will be V_{SD}).

However as V_{DS} becomes equal to $-V_P$, the device enters into saturation during which a saturated amount of current (I_{DSS}) flows through the device, as decided by the value of V_{GS}. Further it is to be noted that the value of saturation current flowing through the device is seen to increase as the V_{GS} becomes more and more negative i.e. saturation current for V_{GS3} is greater than that for V_{GS2} and that in the case of V_{GS4} is much greater than both of them as V_{GS3} is more negative than V_{GS2} while V_{GS4} is much more negative when compared to either of them (Figure 17(b)). In addition, from the locus of the pinch-off voltage it is also clear that as V_{GS} becomes more and more negative, even the negativity of V_P also increases.

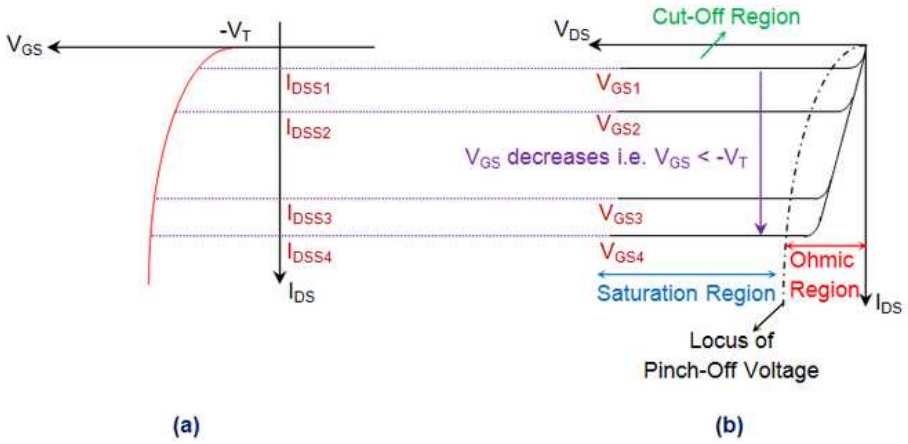


Figure 17: P- Channel Enhancement MOSFET
(a) Transfer Characteristics (b) Output Characteristics

Q10: Draw and Explain V-I characteristics of P - Channel Depletion MOSFET.

Solution:

The transfer characteristics of **p-channel depletion mode MOSFETs** (Figure 18(a)) show that these devices will be normally ON, and thus conduct even in the absence of V_{GS}. This is because they are characterized by the presence of a channel in their default state due to which they have non-zero I_{DS} for V_{GS} = 0V, as indicated by the V_{GS0} curve of Figure 18(b). Although the value of such a current increases with an increase in V_{DS} initially (ohmic region of operation), it is seen to saturate once the V_{DS} exceeds V_P (saturation region of operation). The value of this saturation current is determined by the V_{GS}, and is seen to increase in negative direction as V_{GS} becomes more and more negative. For example, the saturation current for V_{GS3} is greater than that for V_{GS2} which is however greater when compared to that for V_{GS1}. This is because V_{GS2} is more negative when compared to V_{GS1}, and V_{GS3} is much more negative when compared to either of them. Next, one can also note from the locus of pinch-off point that even V_P starts to become more and more negative as the negativity associated with the V_{GS} increases.

Lastly, it is evident from Figure 18(a) that inorder to switch these devices OFF, one needs to increase V_{GS} such that it becomes equal to or greater than that of the threshold voltage V_T. This is because, when done so, these devices will be deprived of their p-type channel, which further drives the MOSFETs into their cut-off region of operation.

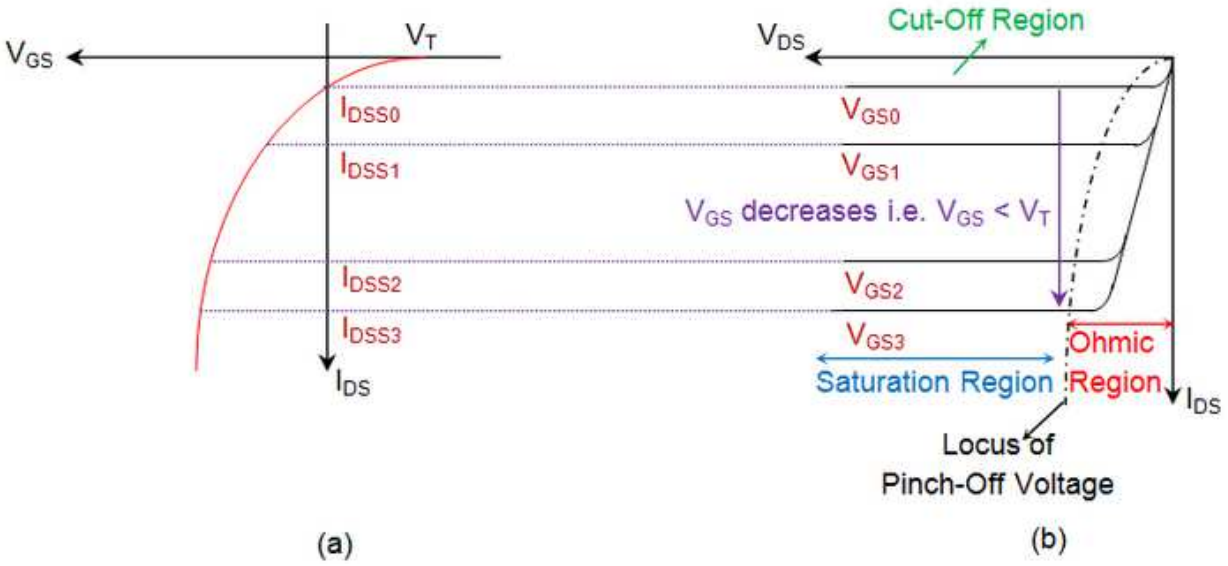
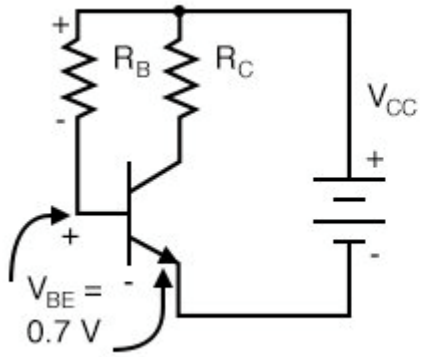


Figure 18: P- Channel Enhancement MOSFET
(a) Transfer Characteristics (b) Output Characteristics

Unit 6
BJT and MOSFET Biasing

Q1. Explain Base Bias Resistor method of biasing of transistor

The simplest biasing uses a base-bias resistor between the base and a base battery VBB. It is convenient to use the existing VCC supply instead of a new bias supply. A similar circuit is shown in the figure below. Write a KVL (Kirchhoff's voltage law) equation about the loop containing the battery, RB, and the VBE diode drop on the transistor in Figure below. Note that we use VBB for the base supply, even though it is actually VCC. If β is large we can make the approximation that IC =IE. For silicon transistors VBE≅0.7V.



$$V_{BB} - I_B R_B - V_{BE} = 0$$

$$V_{BB} - V_{BE} = I_B R_B \qquad \text{(KVL)}$$

$$I_B = \frac{V_{BB} - V_{BE}}{R_B}$$

$$I_E = (\beta + 1) I_B \approx \beta I_B$$

$$\mathbf{I_E = \frac{V_{BB} - V_{BE}}{R_B/\beta}} \qquad \text{(IE base-bias)}$$

Silicon small signal transistors typically have a β in the range of 100-300.

Example Calculations:

Assuming that we have a β=100 transistor, what value of the base-bias resistor is required to yield an emitter current of 1mA?

$$\beta = 100 \qquad V_{BB} = 10V \qquad I_C \approx I_E = 1mA$$

$$R_B = \frac{V_{BB} - V_{BE}}{I_E / \beta} = \frac{10 - 0.7}{1mA/100} = 930k$$

What is the emitter current with a 910kΩ base resistor? What is the emitter current if we randomly get a β=300 transistor?

$\beta = 100 \quad V_{BB} = 10V \quad R_B = 910k \quad V_{BE} = 0.7V$

$$I_E = \frac{V_{BB} - V_{BE}}{R_B / \beta} = \frac{10 - 0.7}{910k/100} = 1.02mA$$

$\beta = 300$

$$I_E = \frac{10 - 0.7}{910k/300} = 3.07mA$$

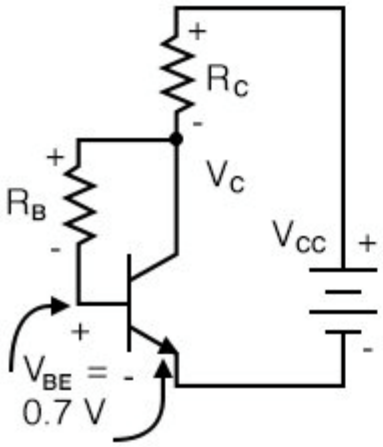
The emitter current is little changed in using the standard value 910kΩ resistor. However, with a change in β from 100 to 300, the emitter current has tripled. This is not acceptable in a power amplifier if we expect the collector voltage to swing from near V_{CC} to near ground. Base-bias is not suitable for high emitter currents, as used in power amplifiers. The base-biased emitter current is not temperature stable.

Thermal runaway is the result of high emitter current causing a temperature increase which causes an increase in emitter current, which further increases temperature.

Q2: Explain Collector-Feedback Bias (CFB) method of biasing an transistor.

Variations in bias due to temperature and β may be reduced by moving the VBB end of the base-bias resistor to the collector as shown in the figure below. If the emitter current were to increase, the voltage drop across RC increases, decreasing V_C, decreasing IB fed back to the base. This, in turn, decreases the emitter current, correcting the original increase.

Write a KVL equation about the loop containing the battery, R_C, R_B, and the V_{BE} drop. Substitute $I_C \cong I_E$ and $I_B \cong I_E/\beta$. Solving for I_E yields the I_E CFB-bias equation. Solving for I_B yields the I_B CFB-bias equation.



$$I_C = \beta I_B \qquad I_C \approx I_E \qquad I_E \approx \beta I_B$$

$$V_{CC} - I_C R_C - I_B R_B - V_{BE} = 0 \qquad \text{(KVL)}$$

$$V_{CC} - I_E R_C - (I_E/\beta) R_B - V_{BE} = 0$$

$$V_{CC} - V_{BE} = I_E R_C + (I_E/\beta) R_B$$

$$V_{CC} - V_{BE} = I_E((R_B/\beta) + R_C)$$

$$\mathbf{I_E = \frac{V_{CC} - V_{BE}}{R_B/\beta + R_C}} \qquad \text{(IE CFB-bias)}$$

$$\mathbf{R_B = \beta\left[\frac{V_{CC} - V_{BE}}{I_E} - R_C\right]} \qquad \text{(RB CFB-bias)}$$

Example Calculations:

Find the required collector feedback bias resistor for an emitter current of 1 mA, a 4.7K collector load resistor, and a transistor with β=100. Find the collector voltage V_C. It should be approximately midway between V_{CC} and ground.

$$\beta = 100 \qquad V_{CC} = 10V \qquad I_C \approx I_E = 1mA \qquad R_C = 4.7k$$

$$R_B = \beta\left[\frac{V_{CC} - V_{BE}}{I_E} - R_C\right] = 100\left[\frac{10 - 0.7}{1mA} - 4.7k\right] = 460k$$

$$V_C = V_{CC} - I_C R_C = 10 - (1mA)\cdot(4.7k) = 5.3V$$

The closest standard value to the 460kΩ collector feedback bias resistor is 470kΩ. Find the emitter current IE with the 470KΩ resistor. Recalculate the emitter current for a transistor with β=100 and β=300.

$$\beta = 100 \qquad V_{CC} = 10V \qquad R_C = 4.7k \qquad R_B = 470k$$

$$I_E = \frac{V_{CC} - V_{BE}}{R_B/\beta + R_C} = \frac{10 - 0.7}{470k/100 + 4.7k} = 0.989mA$$

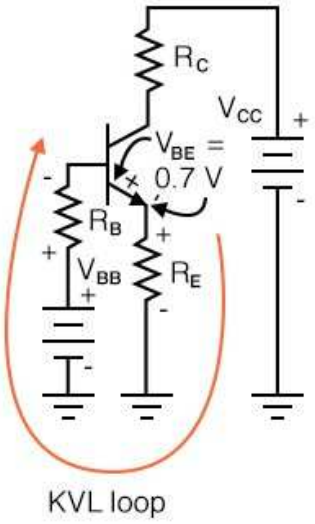
$$\beta = 300$$

$$I_E = \frac{V_{CC} - V_{BE}}{R_B/\beta + R_C} = \frac{10 - 0.7}{470k/300 + 4.7k} = 1.48mA$$

We see that as β changes from 100 to 300, the emitter current increases from 0.989mA to 1.48mA. This is an improvement over the previous base-bias circuit which had an increase from 1.02mA to 3.07mA. Collector feedback bias is twice as stable as base-bias with respect to beta variation.

Q3 : Explain Emitter-Bias method for biasing of transistor.

Inserting a resistor R_E in the emitter circuit as in figure below causes degeneration, also known as negative feedback. This opposes a change in emitter current I_E due to temperature changes, resistor tolerances, β variation, or power supply tolerance. Typical tolerances are as follows: resistor— 5%, beta— 100-300, power supply— 5%. The polarity of the voltage drop across R_E is due to the collector battery V_{CC}. The end of the resistor closest to the (-) battery terminal is (-), the end closest to the (+) terminal it (+). Note that the (-) end of R_E is connected via V_{BB} battery and R_B to the base. Any increase in current flow through R_E will increase the magnitude of negative voltage applied to the base circuit, decreasing the base current, decreasing the emitter current. This decreasing emitter current partially compensates the original increase.



$$V_{BB} - I_B R_B - V_{BE} - I_E R_E = 0$$

$$I_E = (\beta + 1) I_B \approx \beta I_B$$

$$V_{BB} - (I_E/\beta) R_B - V_{BE} - I_E R_E = 0$$

$$V_{BB} - V_{BE} = I_E((R_B/\beta) + R_E)$$

$$I_E = \frac{V_{BB} - V_{BE}}{R_B/\beta + R_E} \qquad \text{(IE emitter-bias)}$$

$$R_B/\beta + R_E = \frac{V_{BB} - V_{BE}}{I_E}$$

$$R_B = \beta \left[\frac{V_{BB} - V_{BE}}{I_E} - R_E \right] \qquad \text{(RB emitter-bias)}$$

Note that base-bias battery V_{BB} is used instead of V_{CC} to bias the base in the figure above. Later the emitter-bias is more effective with a lower base bias battery. We write a KVL equation for the loop through the base-emitter circuit, paying attention to the polarity on the components. We substitute $I_B \cong I_E/\beta$ and solve for emitter current I_E.

Example Calculations:

We calculate a value for R_C and choose a close standard value. An emitter resistor which is 10-50% of the collector load resistor usually works well.

$$\beta = 100 \qquad I_E \approx I_C = 1mA \qquad V_{CC} = V_{BB} = 10V \qquad R_E = 470\Omega$$

$$R_B = \beta \left[\frac{V_{BB} - V_{BE}}{I_E} - R_E \right] = 100 \left[\frac{10 - 0.7}{0.001} - 470 \right] = 883k$$

An 883k resistor was calculated for R_B, an 870k chosen. At β=100, I_E is 1.01mA.

$$\beta = 100 \qquad R_B = 870k$$

$$I_E = \frac{V_{BB} - V_{BE}}{R_B / \beta + R_E} = \frac{10 - 0.7}{870k/100 + 470} = 1.01mA$$

$$\beta = 300$$

$$I_E = \frac{V_{BB} - V_{BE}}{R_B / \beta + R_E} = \frac{10 - 0.7}{870k/300 + 470} = 2.76mA$$

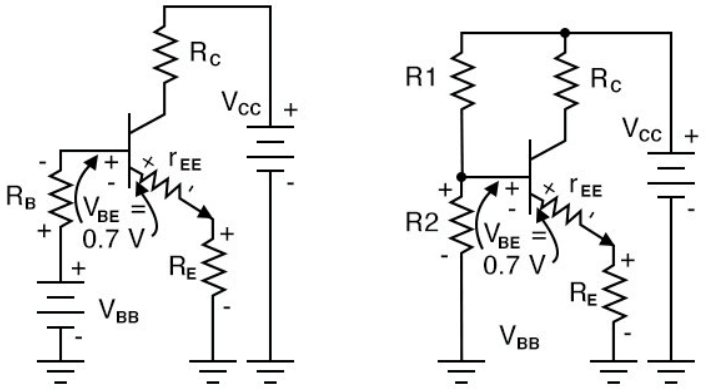
For β=300 the emitter currents are shown in Table below.

Emitter current comparison for β=100, β=300.

Bias circuit	**IC β=100**	**IC β=300**
base-bias	1.02mA	3.07mA
collector feedback bias	0.989mA	1.48mA
emitter-bias, V_{BB}=10V	1.01mA	2.76mA

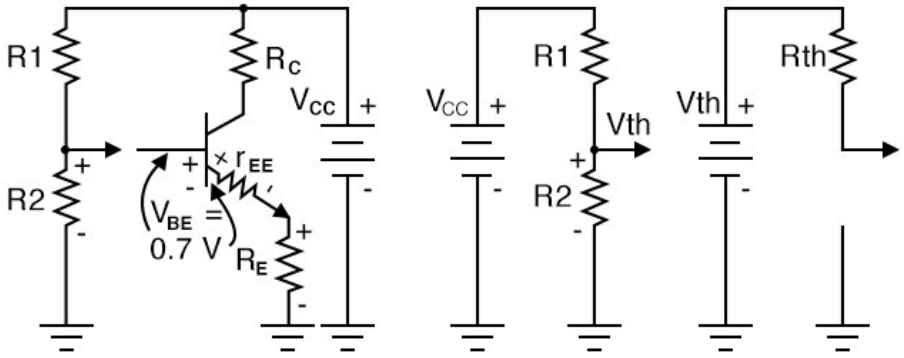
Q4: Explain Voltage Divider Bias method of biasing of transistor.

Stable emitter bias requires a low voltage base bias supply, the figure below. The alternative to a base supply VBB is a voltage divider based on the collector supply VCC.



Voltage Divider bias replaces base battery with voltage divider.

The design technique is to first work out an emitter-bias design, Then convert it to the voltage divider bias configuration by using Thevenin's Theorem. [TK1] The steps are shown graphically in the figure below. Draw the voltage divider without assigning values. Apply Thevenin's Theorem to yield a single Thevenin equivalent resistance R_{th} and voltage source V_{th}.



Thevenin's Theorem converts voltage divider to single supply V_{th} and resistance R_{th}.

The Thevenin equivalent resistance is the resistance from load point (arrow) with the battery (V_{CC}) reduced to 0 (ground). In other words, $R_1||R_2$. The Thevenin equivalent voltage is the open-circuit voltage (load removed). This

calculation is by the voltage divider ratio method. R_1 is obtained by eliminating R_2 from the pair of equations for R_{th} and V_{th}. The equation of R_1 is in terms of known quantities R_{th}, V_{th}, V_{CC}. Note that R_{th} is R_B, the bias resistor from the emitter-bias design. The equation for R_2 is in terms of R_1 and R_{th}.

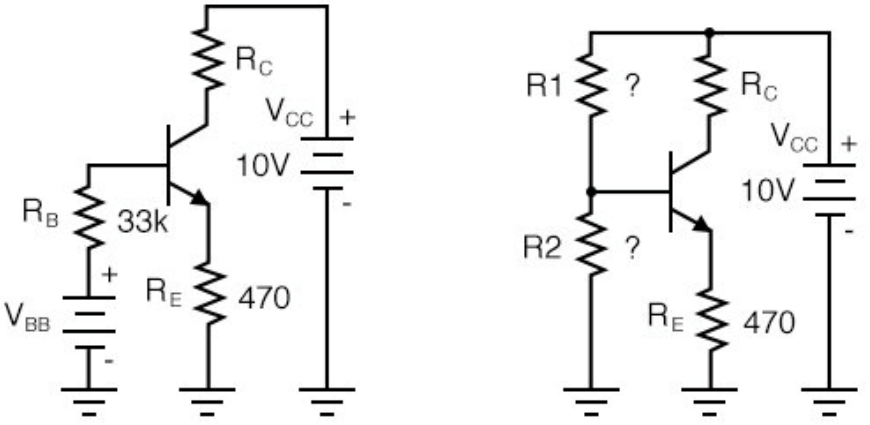
$$Rth = R1 \parallel R2 \qquad Vth = V_{CC}\left[\frac{R2}{R1 + R2}\right]$$

$$\frac{1}{Rth} = \frac{1}{Rth} + \frac{1}{Rth} \qquad f = \frac{Vth}{V_{CC}} = \left[\frac{R2}{R1 + R2}\right]$$

$$\frac{1}{Rth} = \frac{R2 + R1}{R1 \cdot R2} = \frac{1}{R1}\left[\frac{R2 + R1}{R2}\right] = \frac{1}{R1} \cdot \frac{1}{f}$$

$$R1 = \frac{Rth}{f} = R1\frac{V_{CC}}{Vth} \qquad \frac{1}{R2} = \frac{1}{Rth} - \frac{1}{R1}$$

Convert this previous emitter-bias example to voltage divider bias.



Emitter-bias example converted to voltage divider bias.

These values were previously selected or calculated for an emitter-bias example

$$\beta = 100 \qquad I_E \approx I_C = 1mA \qquad V_{CC} = 10V \qquad V_{BB} = 1.5V \qquad R_E = 470\Omega$$

$$R_B = \beta\left[\frac{V_{BB} - V_{BE}}{I_E} - R_E\right] = 100\left[\frac{1.5 - 0.7}{0.001} - 470\right] = 33k$$

Substituting V_{CC}, V_{BB}, R_B yields R_1 and R_2 for the voltage divider bias configuration.

$$V_{BB} = Vth = 1.5V$$

$$R_B = Rth = 33k$$

$$R1 = Rth \frac{V_{CC}}{Vth}$$

$$R1 = 33k \frac{10}{1.5} = 220k$$

$$\frac{1}{R2} = \frac{1}{Rth} - \frac{1}{R1}$$

$$\frac{1}{R2} = \frac{1}{33k} - \frac{1}{220k}$$

$$R2 = 38.8k$$

R_1 is a standard value of 220K. The closest standard value for R2 corresponding to 38.8k is 39k. This does not change I_E enough for us to calculate it.

Q 5 : Draw and explain voltage divider Biasing of N-Channel MOSFET

*N-channel enhancement mode MOSFET circuit shows the source terminal at ground potential and is common to both the input and output sides of the circuit.

*The coupling capacitor acts as an open circuit to d.c. but it allows the signal voltage to be coupled to the gate of the MOSFET

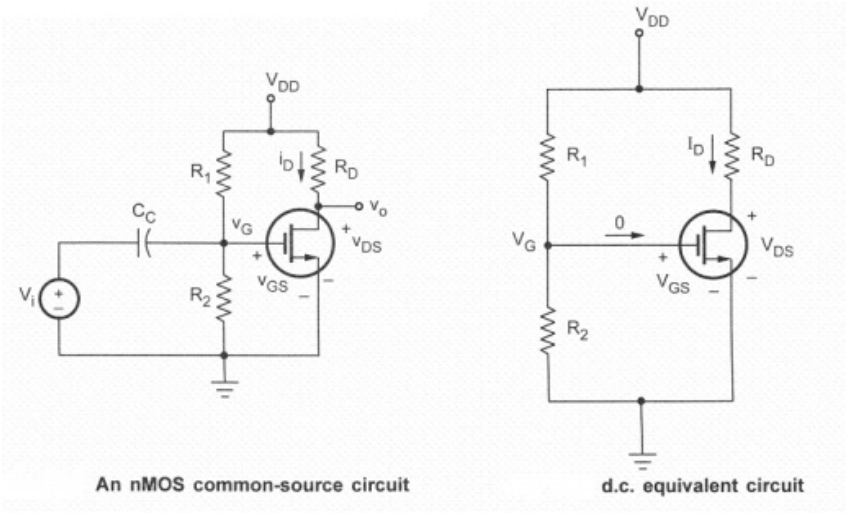


Figure 1

As $I_g = 0$ in V_G is given as,

$V_G = V_{GS} = (R_2 / R_1 + R_2) V_{DD}$

Assume $V_G > V_T$, MOSFET is biased in the saturation region, the drain current is,
$I_D = K (V_{GS} – V_T)^2$

Applying KVL to drain circuit,
$V_{DS} = V_{DD} – I_D R_D$
$= V_{GS} - V_T$

If $V_{DS} > V_{DS(sat)}$ then MOSFET is biased in saturation region

If $V_{DS} < V_{DS(sat)}$, then MOSFET is biased in non-saturation region and the drain current is given by I_D.

Q6: Example 1: For the circuit shown in figure Ex.1, assume that R_1 = 30 KΩ, R_2 = 10 KΩ, R_D = 40 KΩ, V_{DD} = 10 V, V_T = 1V, V_{GS} = 2 V and K = 0.1mA/V^2. Find I_D and V_{DS}.

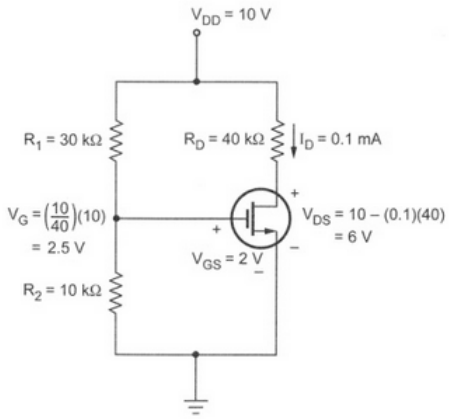


Figure Ex.1

Solution:

$V_G = V_{GS} = (R_2 / R_1 + R_2) V_{DD} = 2.5V$

Assuming the MOSFET is biased in saturation region, the drain current is

$I_D = K (V_{GS} – V_T)^2$
$= 0.1mA/V^2(2 – 1)^2$
$= 0.1$ mA

Applying KVL to drain circuit,

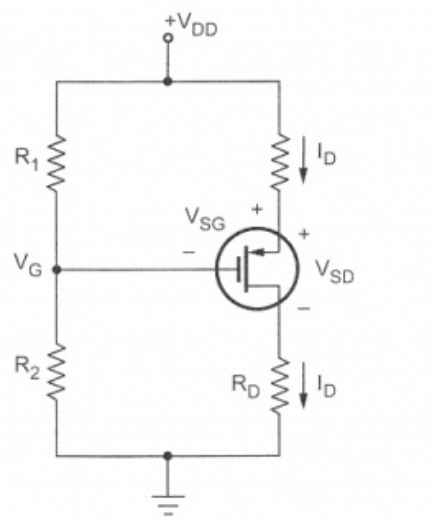
$V_{DS} = V_{DD} – I_D R_D$

= 10 – 0.1mA * 40KΩ
= 6V

Since $V_{DS} > V_{DS(sat)}$ then MOSFET is biased in saturation region, therefore our assumption is correct.

Q 7 : Draw and explain voltage divider Biasing of P-Channel MOSFET

Here, the source is tied to +VDD, Which become signal ground in the a.c. equivalent circuit. Thus it is also a common-source circuit.



A pMOS common-source circuit

Figure 2

The d.c. analysis for this circuit is essentially the same as for the n-channel MOSFET circuit. The gate voltage is given by,

$V_G = (R_2 / R_1 + R_2) V_{DD}$

The gate to source voltage is given by

$V_{SG} = V_{DD} - V_G$

Assuming that $V_{GS} < V_T$, or $V_{SG} > |V_T|$ and the device is biased in saturation region, the drain current is given by

$I_D = K (V_{SG} + V_T)^2$

And the source to drain voltage is given by

$V_{SD} = V_{DD} – I_D R_D$

If $V_{SD} > V_{SD(sat)} = V_{SG} + V_T$, then the MOSFET is biased in saturation region. However if $V_{SD} < V_{SD(sat)}$, then the MOSFET is biased in non-saturation region

Q8: Example 2: For the circuit shown in figure Ex.2 of p-channel common source MOSFET, assume that R_1 = 20 KΩ, R_2 = 60 KΩ, R_D = 15 KΩ, V_{DD} = 10 V, V_T = -0.8V, and K = 0.2mA/V^2. Find I_D and V_{SD}.

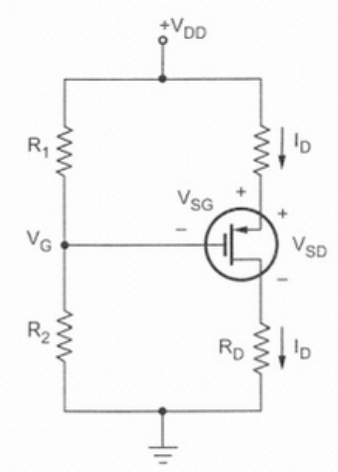


Figure : Ex. 2

Figure shows p-channel common source MSOFET

The Gate voltage is given by

$V_G = (R_2 / R_1 + R_2) V_{DD}$

And the gate to source voltage is given by

$V_{SG} = V_{DD} - V_G$

Assuming that $V_{GS} < V_T$, or $V_{SG} > |V_T|$ and the device is biased in saturation region, the drain current is given by

$I_D = K (V_{SG} + V_T)^2$

And the source to drain voltage is given by

$V_{SD} = V_{DD} – I_D R_D$

Therefore after substituting the values

The gate voltage is

$V_G = (R_2 / R_1+R_2) V_{DD} = 7.5V$

The gate to source voltage is given by

$V_{SG} = V_{DD} - V_G = 2.5$ V
Assuming that the MOSFET is biased in saturation region, the drain current is given by,

$I_D = K (V_{SG} + V_T)^2 = 0.578$ mA

And the source to drain voltage is given by

$V_{SD} = V_{DD} – I_D R_D = 1.33V$

$V_{SD(sat)} = V_{SG} + V_T = 2.5 – 0.8 = 1.7$ V

Therefore the MOSFET is not biased in saturation region.

So for the non-saturation region, the drain current is given by

$I_D = K [2(V_{SG} + V_T) V_{SD} – V^2_{SD}]$

And the source to drain voltage is given by

$V_{SD} = V_{DD} – I_D R_D$

Combining the above two equation,

$I_D = K [2(V_{SG} + V_T) V_{SD} – (V_{DD} – I_D R_D)^2]$

Simplifying the above equation and solving the quadratic equation we get

$I_D = 0.568$ mA or 0.5163 mA

Also

$V_{SD} = V_{DD} – I_D R_D = 1.48$ V or 2.2555V (using both values of I_D)

To bias MOSFET in non-saturation region, $V_{SD}<V_{SD(sat)}$, the $V_{SD} = 1.48V$

This satisfies the condition and hence the MOSFET is biased in non-saturation region.

Therefore $I_D = 0.568$ mA and $V_{SD} = 1.48$ V

Q9: Explain the Load Line concept and Modes of Operation of n-channel MOSFET.

The load line gives a graphical picture showing the region in which the MOSFET is biased. Consider the common-source circuit shown in Fig. 3

Writing Kirchhoff's voltage law around the drain-source loop results $V_{Ds} = V_{DD} - I_{DRD}$, which is the load line equation. It shows a linear relationship between the drain current and drain-to-source voltage. Fig. 4 shows the $V_{DS(sat)}$ characteristic for the MOSFET

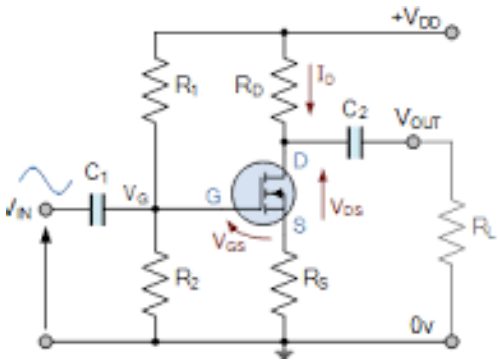


Figure 3

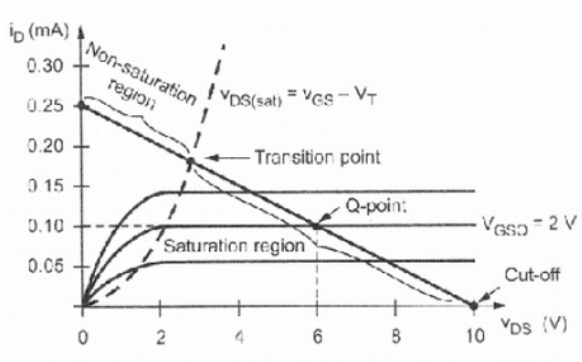


Figure 4

The load line is given by

$$V_{DS} = V_{DD} - I_D R_D$$

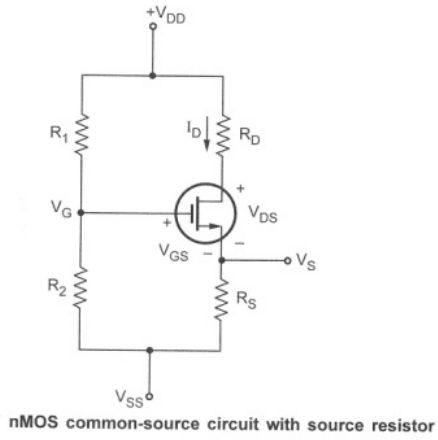
The two end points of the load line are determine in the usual manner. If the drain current = 0, then V_{DS}= 10 v; if V_{DS} = 0, then drain current = 10/40 = 0.25 mA. The Q-point of the MOSFET is given by the d.c. drain current (I_D) and drain-to-source voltage (V_{DS}) and it is always on the load line, as shown in the Fig. 4).

If the gate-to-source voltage is less than V1, the drain current is zero and the MOSFET is in cut-off. As the gate-to- source voltage becomes just greater than the threshold voltage, the MOSFET turns ON and is biased in the saturation region. As V_{GS} increases, the Q-point moves up the load line. The transition point is the boundary between the saturation and non-saturation regions. It is the point where,

$$VDS = VDS(sat) = VGS - VT.$$

As VGS increases, the MOSFET operates in non-saturation region.

Q10: Derive the expression of V_G, V_{GS} and V_{DS} for voltage divider biasing of Common Source circuit for n-channel EMOSFET with source resistor



nMOS common-source circuit with source resistor

Figure 5

The circuit as shown in Figure 5 shows Voltage divider biasing of EMOSFET with source resistor.

Since $I_G = 0$

$V_G = (R_2 / R_1+R_2) V_{DD}$

Applying KVL to input circuit

$V_{GS} – V_S = 0$

$V_{GS} = V_G – I_SR_S$

$= V_G – I_DR_S$ (since $I_D=I_S$)

$= V_G - I_DR_S$

Applying KVL to output circuit

$V_{DD} = I_DR_D – V_{DS} – I_SR_S = 0$

$V_{DS} = V_{DD} –I_DR_D – I_SR_S$

$= V_{DD} - I_DR_D – I_DR_S$ (since $I_D=I_S$)