Engineering Notebook

VOLUME 1

EE1403
Digital CMOS Circuits

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ACKNOWLEDGMENTS

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Message from Principal

The paradigm shift in the domain of teaching learning approach and process has to be in terms of the entire modality getting altered to be 'learner centric' rather of this desired shift, it is desirable nay imperative that the entire learning turns out to be not only pleasure some but also has to be joyous. It must result in learner not only getting into the mode of understanding what is taught to him but also is capable of grasping and articulating it in a handy and free flowing manner without any hindrances of any type. This is feasible only if teaching learning is facilitated not only by a conducive ambience but a conscious effort is entailed in enriching the learner with well meaning, effectively designed learning resource material commensurate with prescribed curriculum, unitization thereto, allocation of differential deserving weightage in the domain of curriculum design and the templated question paper totally in tandem with the operationally structured curriculum. In order to achieve this vital target which ultimately turns out to be the soul of the entire desired process totally conducive to the learner in facilitating his optimal learning, the important and core parts of the targeted syllabus has to be furnished appropriately in the form of facilitated learning resource material. This aspect to my understanding would stand accomplish in the form of 'targeted subject-wise Notebook mode of learning so vital to add to the understanding, decipherance and grasping capacity of the learner in unison. An opinion would go a long way in catering to the larger cause of not only the facilitating the learning process for the credible manner. I deem it my duty to record my appreciation for all those who have rendered their shoulders towards catering to improvisations would stand added to it in order to make it still more poignantly useful and of worth along with substance as a whole.

Yours Sincerely,

UNIT No 1 : Introduction of MOSFET's

Q1.*What are the design abstraction levels?*

Answer:

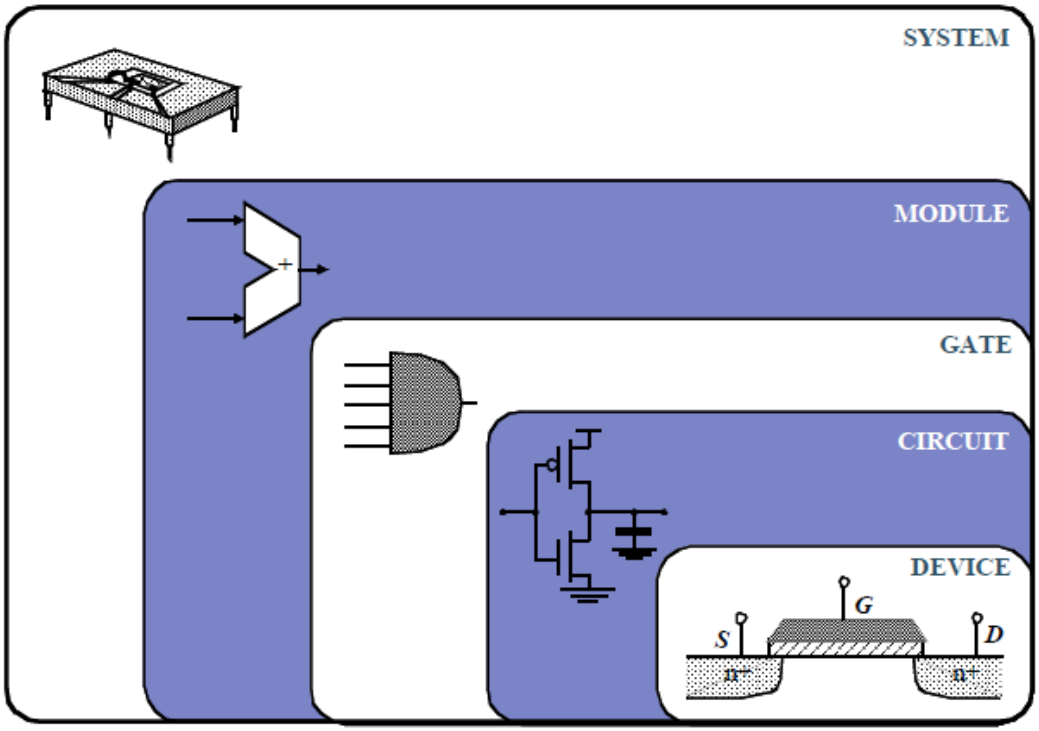


Figure 1.1: Abstraction Level

Q2.*What are the Integrated Circuit Technologies?*

Answer:

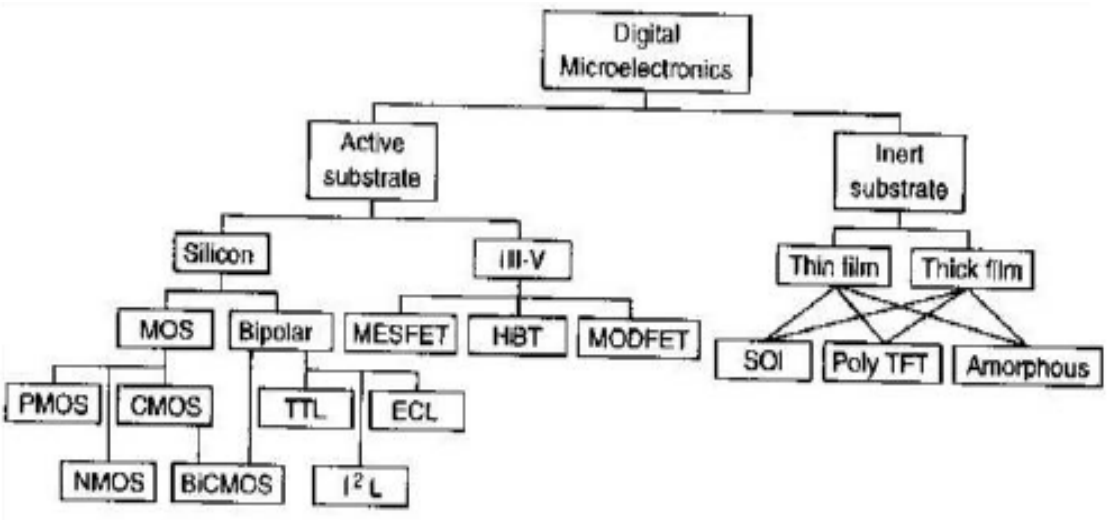


Figure 1.2: Integrated Circuit Technologies

"Technologies" for digital ICs

- passive (inert) circuits:
  - resistors and capacitors only, no transistors
- active circuits; with transistors
  - III-V devices (compound semic.)

• MOS and Bipolar devices (silicon)

• **CMOS dominates the semiconductor/IC industry**

- Silicon is cheaper -> preferred over other materials
- Physics of CMOS is easier to understand

- CMOS is easier to implement/fabricate
- CMOS provides lower power-delay product
- CMOS is lowest power
- Density: can get more CMOS transistors/functions in same chip area

•BUT! CMOS is not the fastest technology!

–BJT and III-V devices are faster

Q3. *What is MOSFET?*

Answer:

Symbols:

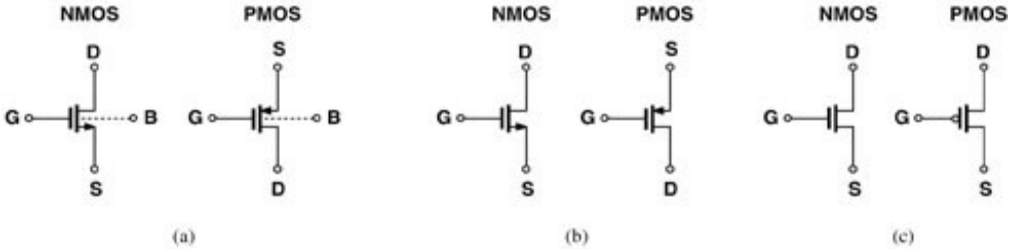
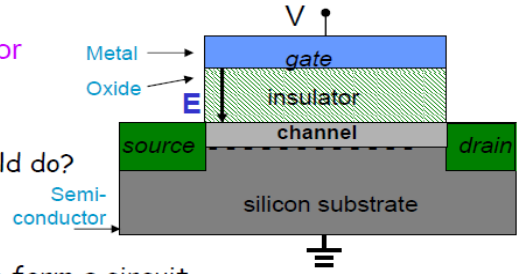


Figure 1.3: Symbols

- Digital integrated circuits rely on transistor switches
  - most common device for digital and mixed signal: MOSFET
- Definitions
  - MOS = Metal Oxide Semiconductor
    - physical layers of the device
  - FET = Field Effect Transistor
    - What field? What does the field do?
    - Are other fields important?
  - CMOS = Complementary MOS
    - use of both nMOS and pMOS to form a circuit



- Primary Features
  - gate
  - gate oxide (insulator)
  - source and drain
  - bulk/substrate
  - channel

NOTE: "metal" is replaced by polysilicon in modern MOSFETs

Cross Sectional View:

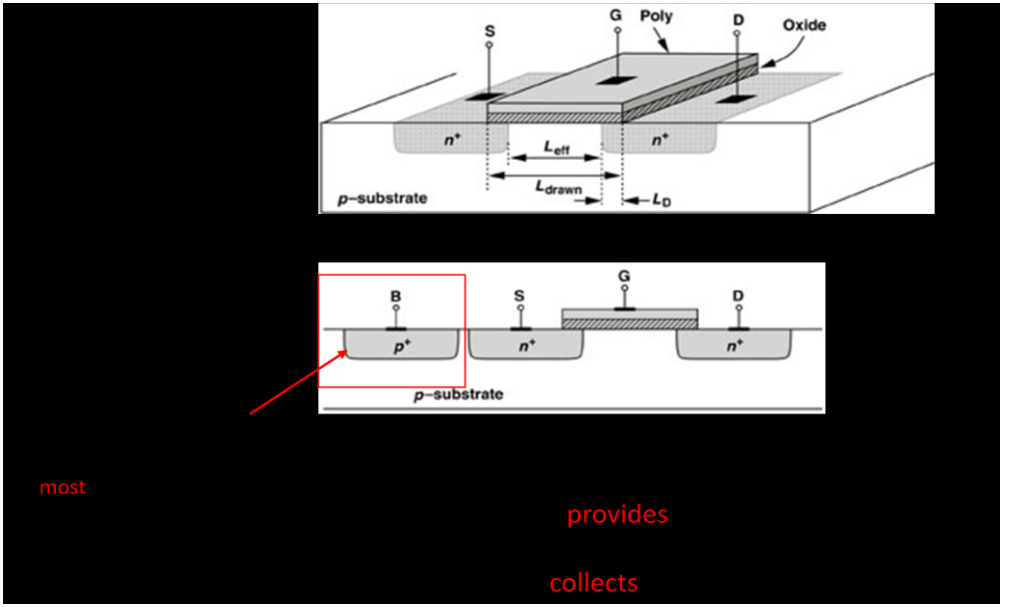


Figure 1.4: Cross Sectional Views

N-well Process:

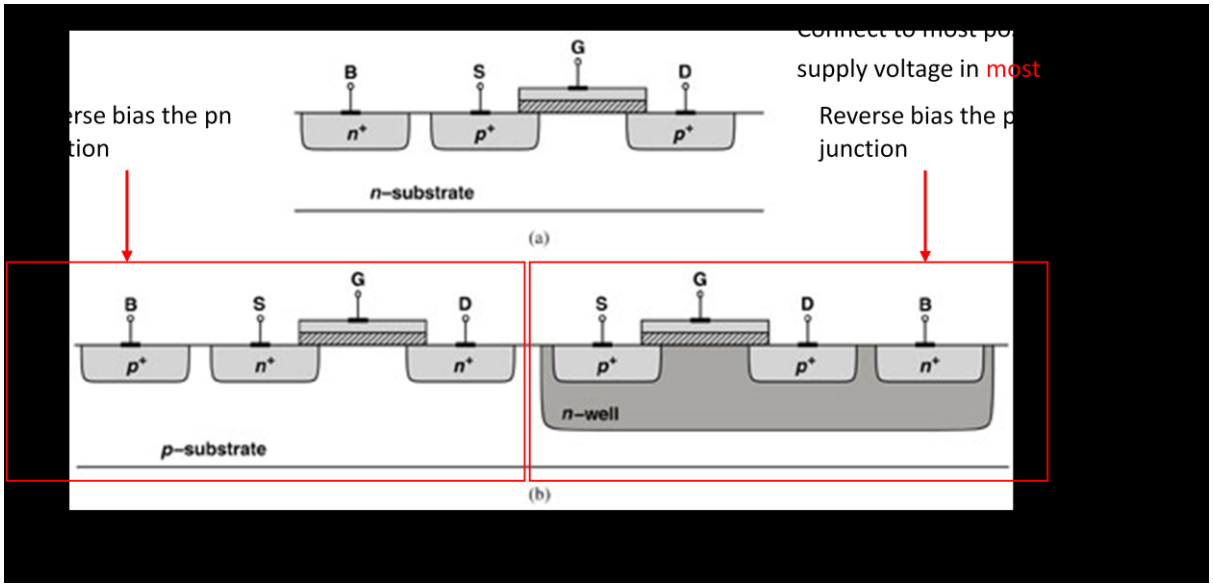


Figure 1.5: N-Well process

ENHANCEMENT TYPE

In this notes, we shall use metal-oxide semiconductor field effect transistors (MOSFET) as our conducting devices. There are two types of MOSFET's: enhancement type and depletion type. For each type, there are again two types: N-type and P-type, as shown in Table 1.1-1.

Table 1.1 : Type of transistors.

Type / Channel	**Enhancement**	Depletion

N	**Enhancement type NMOS**	Depletion type NMOS
P	**Enhancement type PMOS**	Depletion type PMOS

Q3. *Explain the Principle operation of NMOS Enhancement Transistor?*

Answer:

Working of NMOS Transistor and Regions of Operations:

- **Cut off Region :** With zero gate bias, i.e. Vgs = 0, Ids = 0 because the source and the drain are effectively insulated from each other by the two reversed-bias pn junctions (indicated as the diode symbol in the Figure).

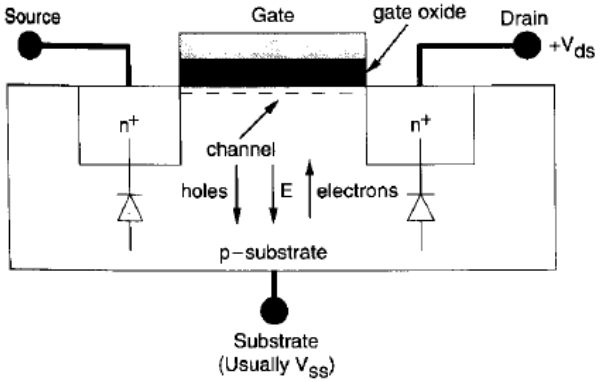


Figure 1.6: Cross sectional view

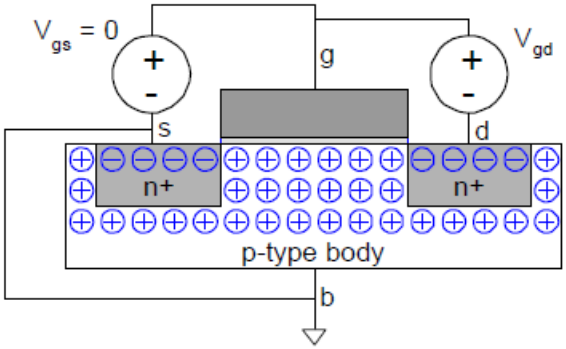


Figure 1.7: Cut off Region

- **Accumulation mode:** With positive gate bias with respect to the source and substrate (generally denoted by Vgs > 0), an electric field E across the substrate is established such that electrons are attracted to the gate and holes are repelled from the gate.

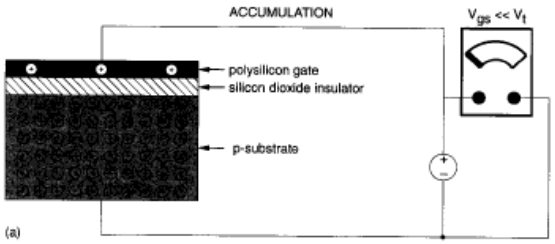


Figure 1.8: Accumulation Mode

- **Triode Region/Non-saturation Region:** If Vg is at Vtn, a depletion channel under the gate free of charges is established.

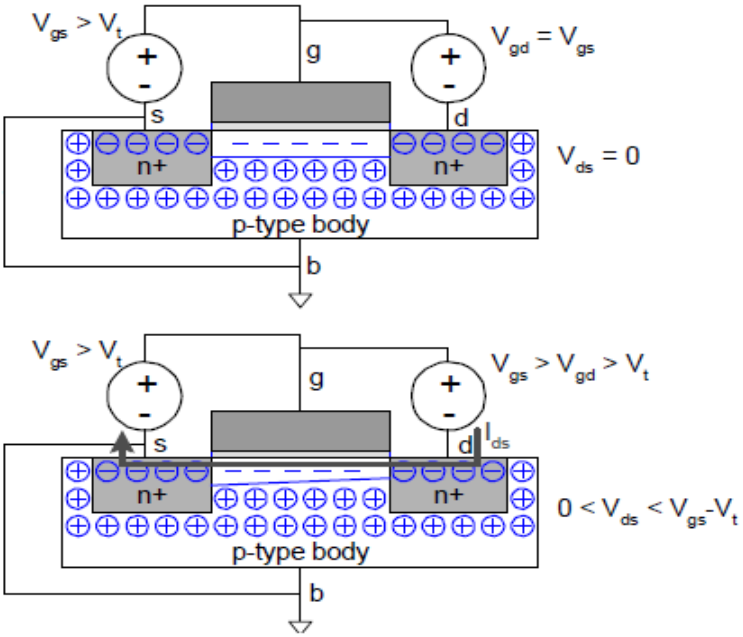


Figure 1.9: Non-saturation Region

- **Inversion mode/Saturation Region:** If Vgs > Vtn, an inversion channel (region) consisting of electrons is established just under the gate oxide and a depletion channel (region) is also established just under the inversion region. Hence the term "n-channel" is applied to the nMOS structure.

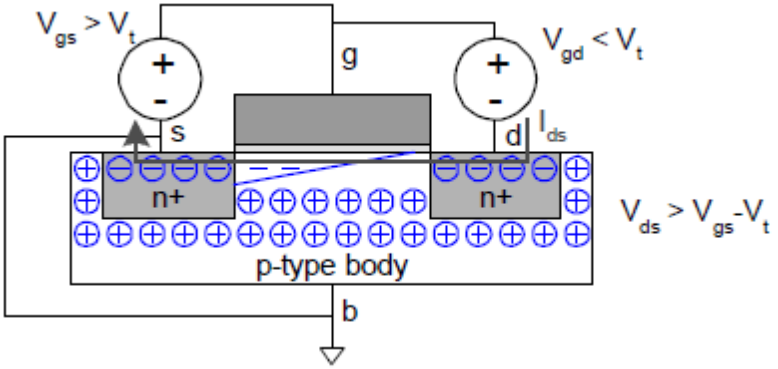


Figure 1.10: Saturation Region

- **Electrically, a MOS device acts as a voltage-controlled switch.**

• It conducts initially when Vgs = Vt.

• Vgs establishes a conducting channel, while Vds is responsible for sweeping the electrons from the source to the drain. Thus, establish a current flow between the drain and the source.

• The electric field established by Vgs is orthogonal to the electric field established by Vds.

• When Vgs >Vt and Vds = 0, the width of the n-type channel at the source end is equal to that at the drain end. This is due to Vgs = Vgd

• Non-saturated (resistive or linear) mode: when Vgs - Vt > Vds > 0, the width of the n-type channel at the source end is larger than that at the drain end.

• Saturated mode: When Vds > Vgs - Vt > 0, the n-type channel no longer reaches the drain. That is, the channel is pinched off. This is due to Vgs > Vt and Vgd < Vt.

Q4: *Derive an expression of voltage current characteristics of MOS Transistor and Small Signal Model of PMOS Transistor:*

Answer:

MOS Device Current -Voltage Equations

The current-voltage relationships for various bias is derived on an nMOS transistor, the basic expressions can be derived for a pMOS transistor by simply replacing the electron mobility μ_n by the hole mobility μ_p and reversing the polarities of voltages and currents. As mentioned in the earlier section, the fundamental operation of a MOS transistor arises out of the gate voltage V_{GS} (between the gate and the source) creating a channel between the source and the drain, attracting the majority carriers from the source and causing them to move towards the drain under the influence of an electric field due to the voltage V_{DS} (between the drain and the source). The corresponding current I_{DS} depends on both V_{GS} and V_{DS} .

Square-Law Model

The simplest description of current flow through a MOSFET is obtained by assuming that Vtn is a constant in the channel.

$$I_{Dn} = K_n\left(\frac{W}{L}\right)\left[(V_{GSn} - V_{Tn})\,V_{DSn} - \frac{1}{2}V_{DSn}^2\right]$$
$$= \frac{\beta_n}{2}\left[2\,(V_{GSn} - V_{Tn})\,V_{DSn} - V_{DSn}^2\right]$$

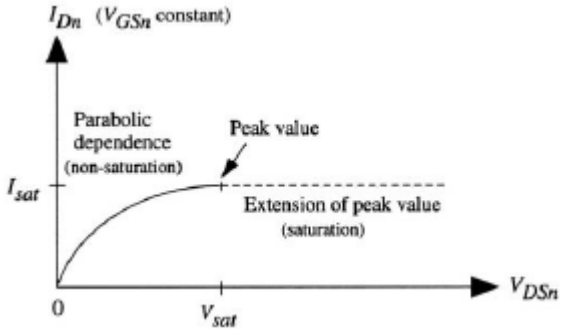


Figure 1.11: Saturation Region

Basic DC Equations

Let us consider the simplified structure of an nMOS transistor shown in Figure, in which the majority carriers electrons flow from the source to the drain.

The conventional current flowing from the drain to the source is given by

$$I_{DS} = -I_{SD} = (\text{charge induced in channel})/(\text{electron transit time}) = Q_C / \tau_n$$

Now, transit time τ_n = (length of the channel) / (electron velocity) = L / v

where velocity is given by the electron mobility and electric field; or, $v = \mu_n E_{DS}$

Now, $E_{DS} = V_{DS}/L$, so that velocity $v = (\mu_n V_{DS})/L$

Thus, the transit time is $\tau_n = L^2/(\mu_n V_{DS})$

At room temperature (300 K), typical values of the electron and hole mobility are given by

$\mu_n = 650\ \text{cm}^2/V-\text{sec}$, and $\mu_p = 240\ \text{cm}^2/V-\text{sec}$

We shall derive the current-voltage relationship separately for the linear (or non-saturated) region and the saturated region of operation.

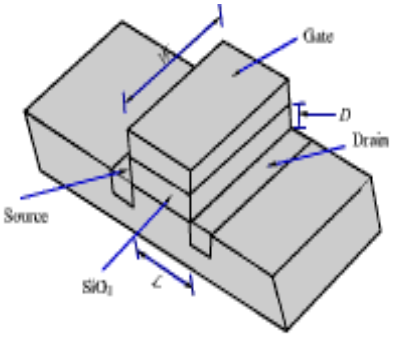


Figure 1.12: Simplified geometrical structure of an nMOS transistor

Linear region: Note that this region of operation implies the existence of the uninterrupted channel between the source and the drain, which is ensured by the voltage relation V_{GS} - V_{th} > V_{DS} .

In the channel, the voltage between the gate and the varies ***linearly*** with the distance x from the source due to the IR drop in the channel. Assume that the device is not saturated and the average channel voltage is V_{DS} /2.

The effective gate voltage $V_{G,eff} = V_{gs} - V_{th}$

Charge per unit area = $E_g \varepsilon_{ins} \varepsilon_0$

Where

E_g average electric field from gate to channel,

ε_{ins} : relative permittivity of oxide between gate and channel (~4.0 for SiO_2), and

ε_0 : free space permittivity (8.85 x 10 $^{-14}$ F/cm).

So, induced charge $Q_C = E_g \varepsilon_{ins} \varepsilon_0 WL$.

where W: width of the gate and L : length of channel.

$$Q_C = E_g \varepsilon_{ins} \varepsilon_0 WL$$

$$O_C = WL\varepsilon_{ins}\varepsilon_0 / D\left\{(V_{GS} - V_{th}) - V_{DS}/2\right\}$$

$$\tau_n = L^2 / (\mu_n V_{DS})$$

Thus, the current from the drain to the source may be expressed as

$$I_{DS} = Q_C / \tau_n = \varepsilon_{ins}\varepsilon_0\mu_n W / (LD)\left\{(V_{GS} - V_{th}) - V_{DS}/2\right\}V_{DS}$$

Thus, in the non-saturated region, where $V_{DS} < V_{GS} - V_{th}$

$$I_{DS} = (KW) / L\left\{(V_{GS} - V_{th})V_{DS} - V^2{}_{DS}/2\right\} \quad \text{.....(2.2)}$$

where the parameter $K = (\varepsilon_{ins}\varepsilon_0\mu_n) / D$

Writing $\beta = (KW) / L$, where W/L is contributed by the geometry of the device,

$$I_{DS} = \beta\left\{(V_{GS} - V_{th})V_{DS} - V^2{}_{DS}/2\right\} \quad \text{.....(2.3)}$$

Since, the gate-to-channel capacitance is $C_G = (\varepsilon_{ins}\varepsilon_0 WL)/D$ (parallel plate capacitance), then $K = (C_G\mu_n)/(WL)$

, so that (2.2) may be written as

$$I_{DS} = (C_G\mu_n)/L^2\{(V_{GS} - V_{th})V_{DS} - V^2_{DS}/2\} \quad \text{.....(2.4)}$$

Denoting $C_G = C_0\, WL$ where C_0 : gate capacitance per unit area,

$$I_{DS} = (C_0\mu_n W)/L^2\{(V_{GS} - V_{th})V_{DS} - V^2_{DS}/2\} \quad \text{..... (2.5)}$$

Saturation region : Under the voltage condition V_{GS} - V_{th} = V_{DS} , a MOS device is said to be in saturation region of operation. In fact, saturation begins when V_{DS} = V_{GS} - V_{th} , since at this point, the resistive voltage drop (IR drop) in the channel equals the effective gate-to-channel voltage at the drain. One may assume that the current remains *constant* as V_{DS} increases further. Putting V_{DS} = V_{GS} - V_{th} , the equations (2.2-2.5) under saturation condition need to be modified as

$$I_{DS} = (KW)/L\{(V_{GS} - V_{th})^2/2\} \quad \text{.....(2.6)}$$

$$I_{DS} = \beta(V_{GS} - V_{th})^2/2 \quad \text{.....(2.7)}$$

Basic MOSFET I-V Characteristics:

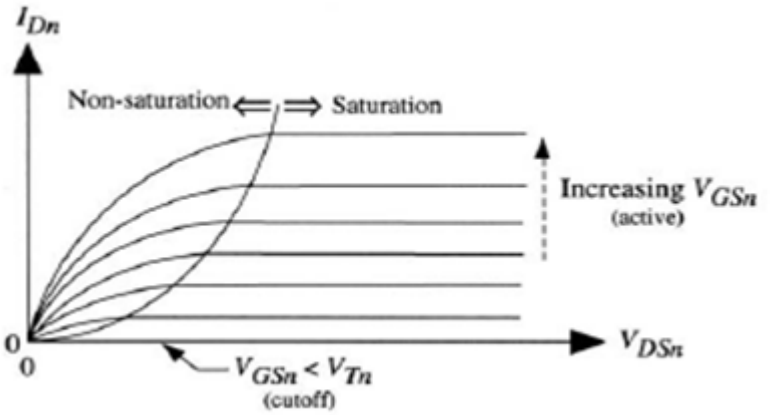
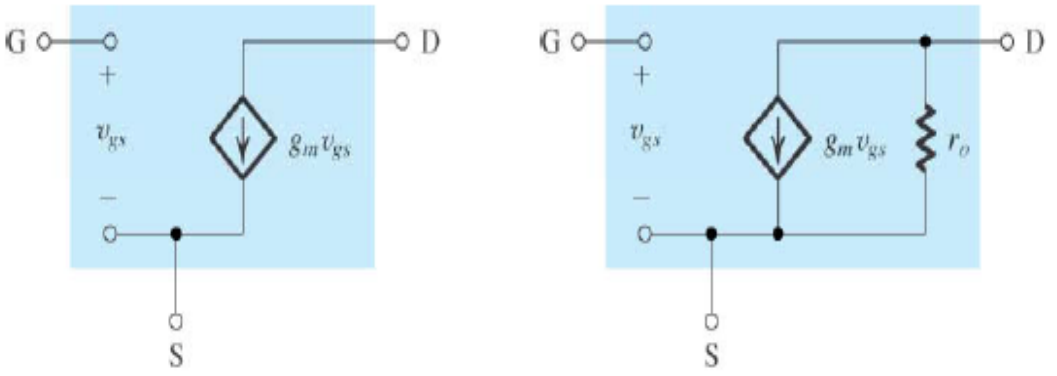


Figure 1.13: Basic MOSFET I-V Relation

Q5: *Draw the small signal model of enhancement type NMOS Transistor.*



This model assume (short coming) that drain current in saturation is independent of the drain voltage, we have learnt that in reality drain current depend on the V_{DS} in a linear manner and which is modeled by a finite resistance r_o (10 KΩ to 1000 KΩ) between drain and source. V_A is MOSFET parameter (It is proportional to the MOSFET channel length.

$$I_D = \frac{1}{2} K_n' \left(\frac{W}{L} \right) v_{ov}^2$$

$$A_v = \frac{v_d}{v_{gs}} = -g_m (R_D \parallel r_o) \quad \{ v_d = -i_d R_D = -g_m v_{gs} R_D \}$$

$$r_o = \frac{|V_A|}{I_D} \quad \text{where} \quad V_A = \frac{1}{\lambda}$$

(a) Neglecting the dependence of i_D on v_{DS} in saturation (the channel-length modulation effect); and **(b)** Including the effect of channel-length modulation, modeled by output resistance $r_o = |V_A| / I_D$.

Figure 1.14: Small Signal Model

Derivation of MOS small signal model

$$\begin{cases} i_G = 0 \\ i_D = 0.5\mu_n C_{ox}\dfrac{W}{L}(v_{GS}-V_t)^2(1+\lambda v_{DS}) = f(v_{GS}, v_{DS}) \end{cases} \qquad \begin{cases} I_G = 0 \\ I_D = 0.5\mu_n C_{ox}\dfrac{W}{L}(V_{GS}-V_t)^2(1+\lambda V_{DS}) \end{cases}$$

$$i_D = f(x,y) \quad \text{with} \quad v_{GS} \leftrightarrow x, \quad v_{DS} \leftrightarrow y$$

$$i_d = \left.\frac{\partial f}{\partial v_{GS}}\right|_{V_{GS},V_{DS}} \cdot v_{gs} + \left.\frac{\partial f}{\partial v_{DS}}\right|_{V_{GS},V_{DS}} \cdot v_{ds}$$

$$\left.\frac{\partial f}{\partial v_{GS}}\right|_{V_{GS},V_{DS}} = 2\times 0.5\mu_n C_{ox}\frac{W}{L}(v_{GS}-V_t)(1+\lambda v_{DS})\Big|_{V_{GS},V_{DS}}$$

$$= 2\times\frac{0.5\mu_n C_{ox}\dfrac{W}{L}(V_{GS}-V_t)^2(1+\lambda V_{DS})}{(V_{GS}-V_t)} = \frac{2I_D}{V_{OV}} \equiv g_m$$

$$\left.\frac{\partial f}{\partial v_{DS}}\right|_{V_{GS},V_{DS}} = \lambda\times 0.5\mu_n C_{ox}\frac{W}{L}(v_{GS}-V_t)^2\Big|_{V_{GS},V_{DS}}$$

$$= \lambda\times\frac{0.5\mu_n C_{ox}\dfrac{W}{L}(V_{GS}-V_t)^2(1+\lambda V_{DS})}{(1+\lambda V_{DS})} = \frac{\lambda I_D}{(1+\lambda V_{DS})} \equiv \frac{1}{r_o}$$

$$i_d = g_m \cdot v_{gs} + \frac{v_{ds}}{r_o}$$

$$i_g = 0$$

$$g_m = \frac{2I_D}{V_{OV}}$$

$$^{*}\ r_o = \frac{1}{\lambda \cdot I_D}$$

(* For $\lambda\, v_{DS} << 1$)

Q6: *Draw the small signal model of given circuit.*

Answer:

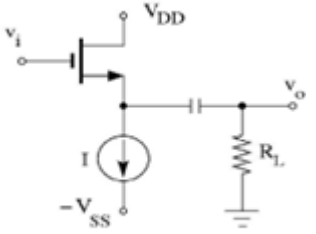


Figure 1.15: Given Circuit

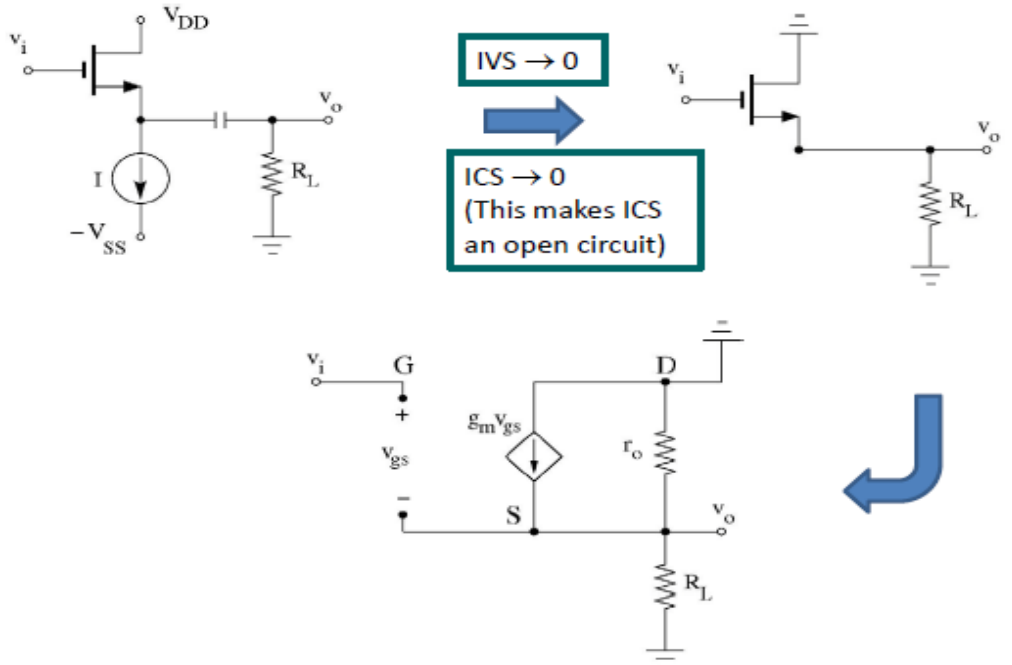


Figure 1.16: Small Signal Model

Q7: *Explain the Behavior of IDS with a Load for NMOS Transistors.*

Answer:

Consider Fig. 1.17 where a load is connected to the drain of the NMOS transistor and a power supply V_{DD} is connected to the load and a bias voltage V_{GS} is provided at the gate.

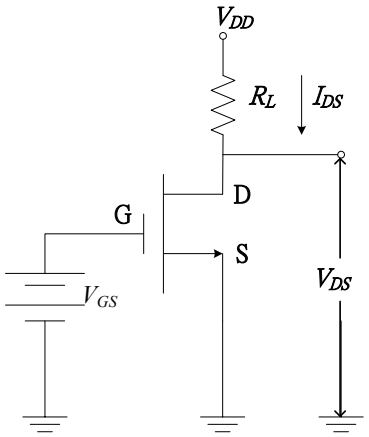


Figure 1.17: An NMOS transistor with a load.

From the circuit shown in Fig. 1.3-1, we have the following equation:

$$V_{DS} = V_{DD} - I_{DS} R_L . \qquad (1.3\text{-}1)$$

In Equation (1.3-1), there are two variables, namely V_{DS} and I_{DS}. But there is only one equation. Therefore, we cannot determine I_{DS} from this equation only. But, we may draw a straight line to illustrate Equation (1.3-1) as in Fig. 1.3-2.

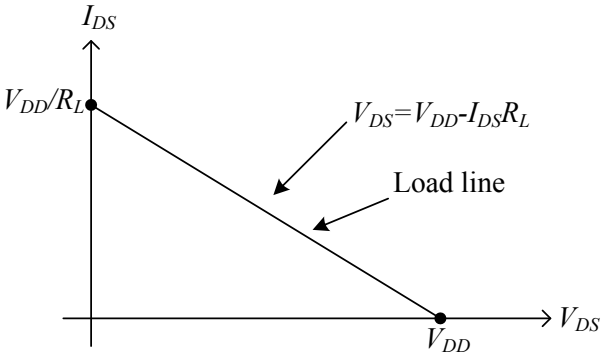


Figure 1.18: NMOS The load line.

What is missing in Equation (1.3-1) is the voltage V_{GS}. Note that current I_{DS} is heavily influenced by V_{GS}

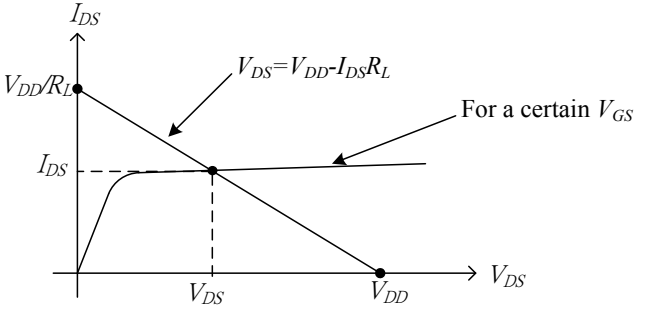


Figure 1.19: The determination of I_{DS} and V_{DS}.

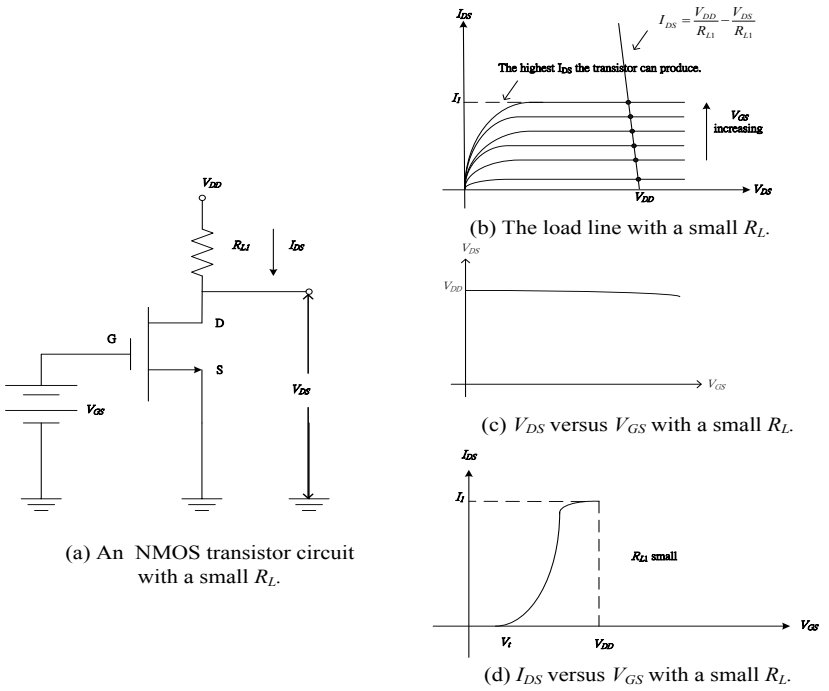
Fig. 1.19 shows how we can determine the value of I_{DS} by finding the intersection of the load line and the *I-V* curve of the transistor. From Fig. 1.3-3, we know that we can not only determine the value of I_{DS}, but also that of V_{DS}. Note that the *I-V* curve is fixed once V_{GS} is given. But the value of R_L plays a critical role now because it determines the slope of the load

line. Different R_L's will give different load lines and thus different I_{DS}'s and V_{DS}'s.

Let us consider the case where V_{GS} changes. There will be a family of *I-V* curves.

Case 1: R_L is small.

This case is illustrated in Fig. 1.3-4.



(a) An NMOS transistor circuit with a small R_L.

(b) The load line with a small R_L.

(c) V_{DS} versus V_{GS} with a small R_L.

(d) I_{DS} versus V_{GS} with a small R_L.

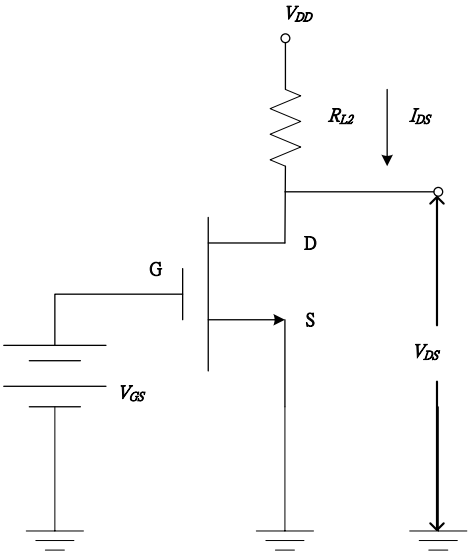
Figure 1.20: Voltage and current of an NMOS circuit with a small R_L.

In this case, as V_{GS} increases, we should note two phenomena: (1) I_{DS} rises sharply. (2) V_{DS} falls a little. We would like to point out here that V_{DS} is more

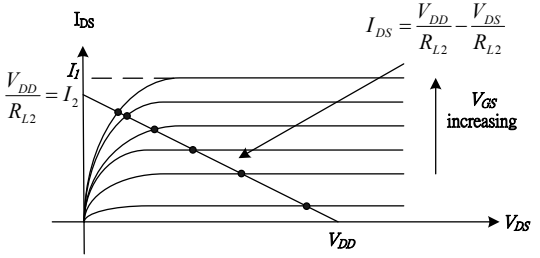
important than I_{DS} as it is usually the output of the circuit. We shall discuss this in detail in the next chapter. At present, the reader may simply note that when R_L is small, V_{DS} will not change much as V_{GS} changes.

Case 2: R_L **is moderate**.

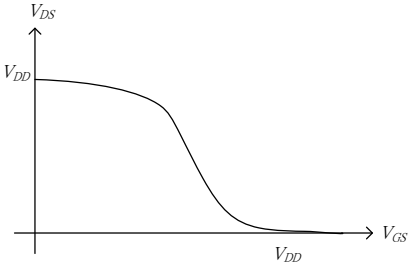
The case is illustrated in Fig. 1.21.



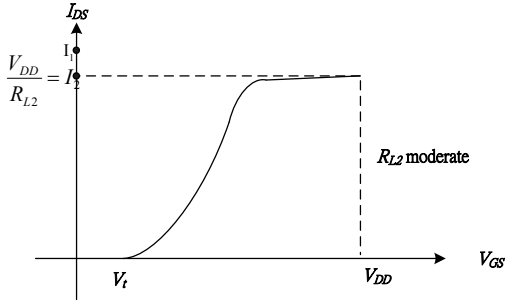
(a) An NMOS transistor circuit with a moderate R_L.



(b) The load line with a moderate R_L.



(c) V_{DS} versus V_{GS} with a moderate R_L.



(d) I_{DS} versus V_{GS} with a moderate R_L.

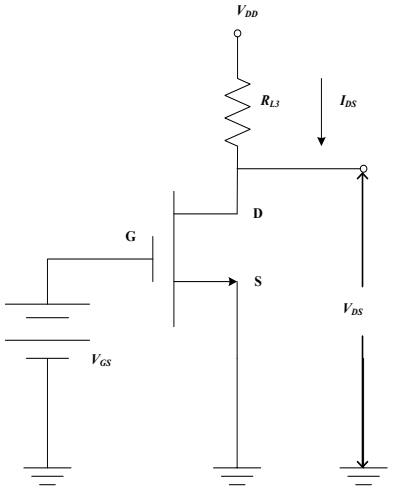
Figure 1.21: Voltage and current of an NMOS circuit with a moderate R_L.

We note that the changes of both I_{DS} and V_{DS} are moderate as V_{GS} increases.

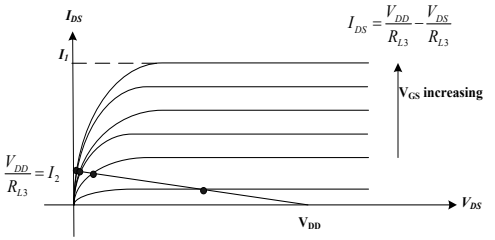
In other words, none of them changes sharply.

Case 3: R_L **is large**.

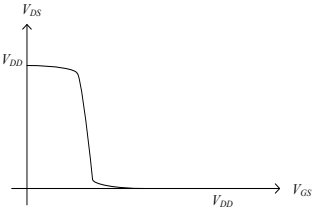
The case is illustrated in Fig. 1.22.



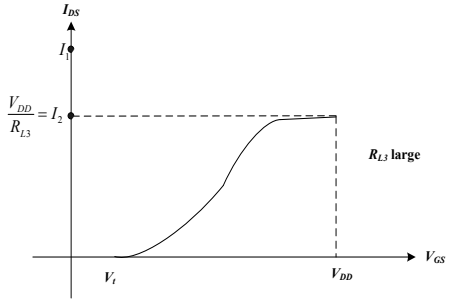
(a) An NMOS transistor circuit with a large R_L.



(b) The load line with a large R_L.



(c) V_{DS} versus V_{GS} with a large R_L.



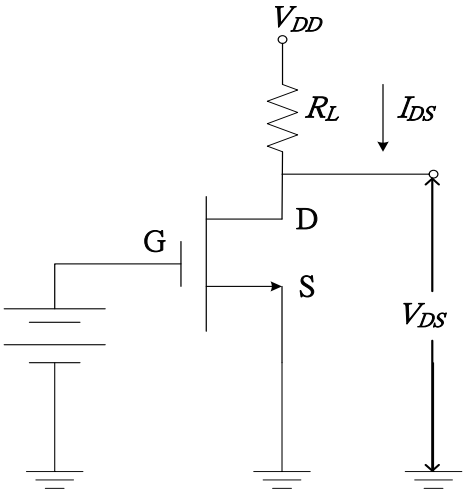
(d) I_{DS} versus V_{GS} with a large R_L.

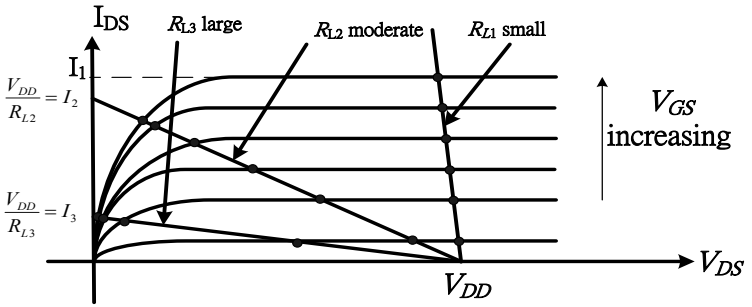
Figure 1.22: Voltage and current of an NMOS circuit with a large R_L.

In this case, we note that I_{DS} rises a little and V_{DS} falls sharply as V_{GS} increases. Again,

we shall emphasize here that the rate of change of V_{DS} is rather significant. In general, we would like V_{DS} to change drastically.

Fig. 1.23 summarizes the three cases.





For any case, $V_{DS}=V_{DD}-I_{DS}R_L$

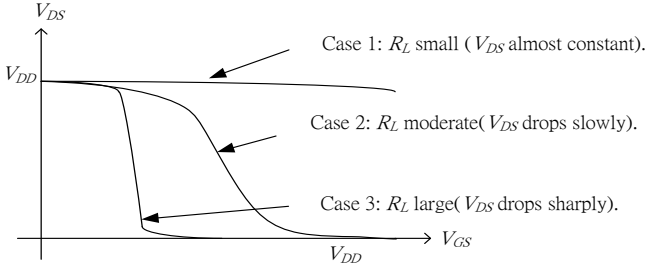


Figure 1.23: Fig. 1.3-7. V_{DS} versus V_{GS} of an NMOS transistor circuit for three different loads.

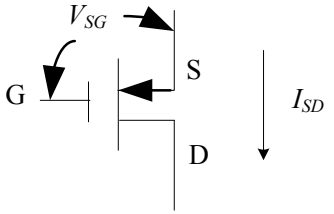
V_{GS} is called the bias voltage. Its significance will be explained later. V_{DS} is called the operating point voltage, or simply operating point. Fig. 1.3-8 illustrates how different operating points are produced. Note that it takes both V_{GS} and R_L to produce an operating point.

Q6: *Explain Enhancement type PMOS Transistor.*

Answer:

The PMOS Transistor:

A typical PMOS transistor is now shown in Fig. 1.4-1.



PMOS

Figure 1.24 Fig. 1.4-1. A PMOS transistor.

For a PMOS transistor, the controlling (biasing) voltage is V_{SG}, as opposed to V_{GS} in an NMOS transistor. The higher V_{SG} is, the higher I_{SD} will become. Note that in a PMOS transistor, the current flows from source to drain which is different from the case in an NMOS transistor. Fig. 1.25illustrates a family of *I-V* curves for PMOS transistors.

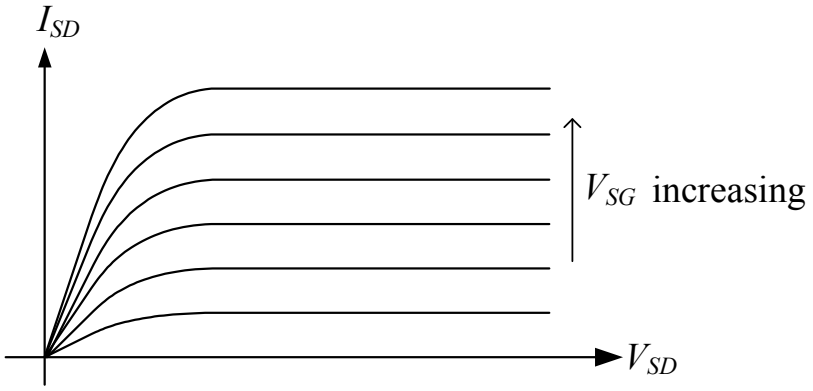
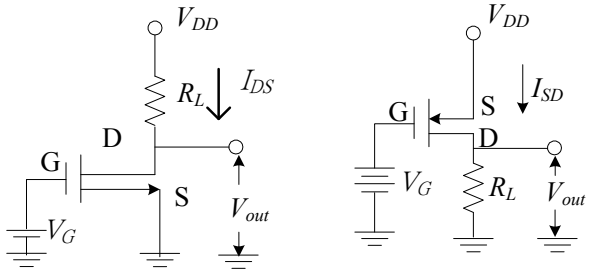


Figure 1.25 Fig. I-V curve for a PMOS transistor.

In Fig. 1.26, we show the difference between the NMOS circuits and the PMOS circuits.



(a) An NMOS transistor circuit.

(b) A PMOS transistor circuit.

Figure 1.26 Fig. 1.4-3 NMOS and PMOS transistor circuits

For the PMOS circuit, we have the following equation:

$$V_{out} = V_{DD} - V_{SD} = I_{SD} R_L \qquad (1.4\text{-}1)$$

First, we plot $-V_{SD}$ vs I_{SD} as in Fig. 1.27.

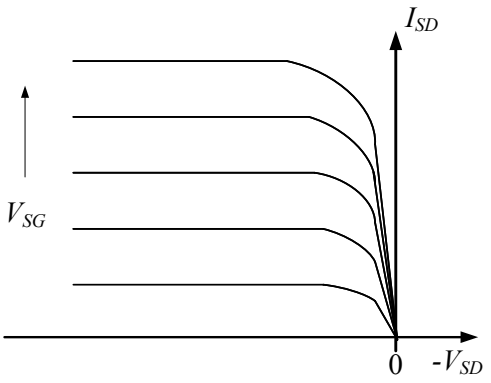


Figure 1.27 I-V curve for $-V_{SD}$ for a PMOS transistor.

We then plot $Vout = V_{DD} - V_{SD} = -V_{SD} + V_{DD}$ as in Fig. 1.28.

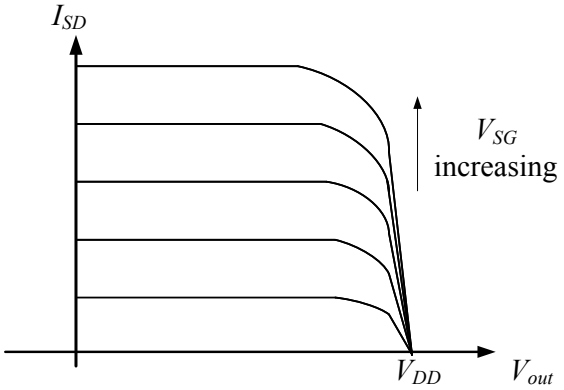


Figure 1.28 I-V curve for V_{out} for a PMOS transistor.

Finally, we add the load line which is $I_{SD} = V_{out} / R_L$ to Fig. 1.28 to produce Fig. 1.29.

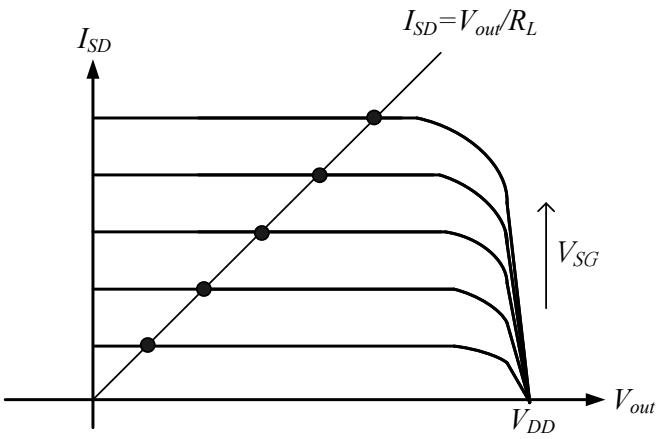


Figure 1.29 I-V curves and a load line for a PMOS transistor circuit

Let us compare the two circuits shown in Fig. 1.30.

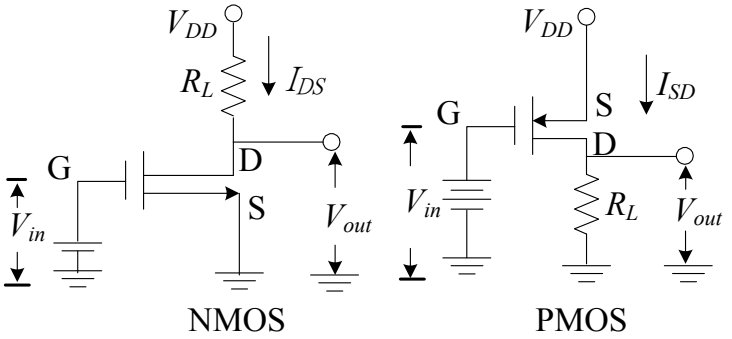


Figure 1.30 An NMOS transistor circuit and a PMOS transistor with the same V_{in}.

Q7:What is threshold voltage?

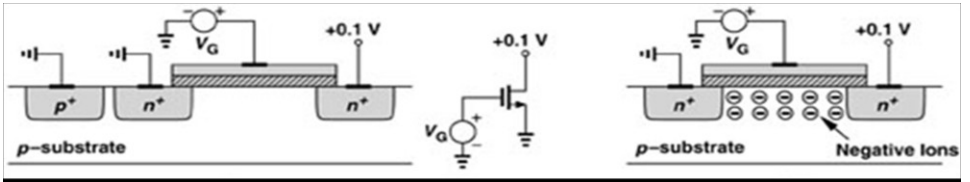
Answer:

Threshold Voltage:

The threshold voltage for a MOS transistor can be defined as the voltage applied between the gate and the source of a MOS device below which the drain-to-source current Ids "effectively" drops to zero.

– In general, V_t is a function of the following parameters.

- Gate conduction material
- Gate insulation material
- Gate insulator thickness
- Channel doping
- Impurities at the silicon-insulator interface
- Voltage between the source and the substrate, Vsb.



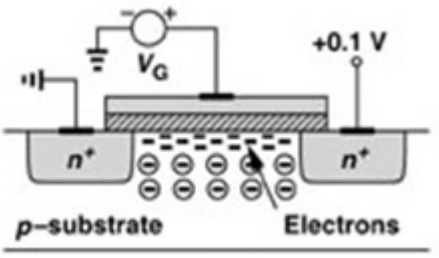


Figure 1.31 Cross Sectional view

When the surface potential increases to a critical value, inversion occurs.

1. No further change in the width of the depletion region is observed.
2. A thin layer of electrons in the depletion region appear underneath the oxide.
3. A continuous n-type (hence the name inversion) region is formed between the source and the drain. Electrons can no be sourced from S and be collected at the drain terminal. (Current, however, flows from drain to source)
4. Further increase in VG will further increase the charge density.

The voltage VG required to provide an inversion layer is called the threshold voltage.

Threshold voltage equations:

- $V_t = V_{t\text{-}mos} + V_{fb}$
- $V_{t\text{-}mos} = 2\phi_b + \frac{Q_b}{C_{ox}}$
- $\phi_b = \frac{kT}{q}\ln(\frac{N_A}{N_i})$
- $Q_b = \sqrt{2\varepsilon_{Si} q N_A 2\phi_b}$

$$V_{fb} = \phi_{ms} - \frac{Q_{fc}}{C_{ox}}$$

Vt-mos is the ideal threshold voltage for an ideal MOS capacitor

• V_{fb} is the flat-band voltage

• k: Boltzmann's constant = 1.38 * 10^{-23} J/oK.

• q: electronic charge = 1.602 * 10^{-19} Coulomb.

• T: Temperature (^oK).

• N_A: the density of carriers in the doped substrate.

• N_i: the density of carriers in the undoped substrate.

• $\in_{si}$: the permittivity of silicon

• Cox: the gate-oxide capacitance, which is inversely proportional to the gate oxide thickness (tox).

• Q_{fc}: the fixed charge due to surface states that arise due to imperfections in the silicon-oxide interface and doping.

• f_{ms}: the work function difference between the gate material and the silicon substrate.

– More details can be found in the text book by Weste.

Two common techniques for the adjustment of Vt.

• Affecting Qfc by varying the doping concentration at the silicon-insulator interface through ion implantation.

• Affecting Cox by using different insulating material for the gate. A layer of silicon nitride (Si_3N_4) combined with a layer of silicon oxide can effectively increase the relative permittivity of gate insulator from 3.9 to 6.

Summary:

TABLE Relations Between Voltages for the Three Regions of Operation of a CMOS Inverter

	CUTOFF	NONSATURATED	SATURATED
p-device	$V_{gsp} > V_{tp}$	$V_{gsp} < V_{tp}$ $V_{in} < V_{tp} + V_{DD}$	$V_{gsp} < V_{tp}$ $V_{in} < V_{tp} + V_{DD}$
	$V_{in} > V_{tp} + V_{DD}$	$V_{dsp} > V_{gsp} - V_{tp}$ $V_{out} > V_{in} - V_{tp}$	$V_{dsp} < V_{gsp} - V_{tp}$ $V_{out} < V_{in} - V_{tp}$
n-device	$V_{gsn} < V_{tn}$	$V_{gsn} > V_{tn}$ $V_{in} > V_{tn}$	$V_{gsn} > V_{tn}$ $V_{in} > V_{tn}$
	$V_{in} < V_{tn}$	$V_{dsn} < V_{gs} - V_{tn}$ $V_{out} < V_{in} - V_{tn}$	$V_{dsn} > V_{gs} - V_{tn}$ $V_{out} > V_{in} - V_{tn}$

$V = I\,R$	$Q = C\,V$ $I = Q / t$
$n\,p = n_i^2$	$\sigma = q(\mu_n n + \mu_p p)$
$R = L/\sigma A$	$Jx = \sigma\,Ex$
$Cox = \varepsilon_{ox}/t_{ox}$	$Q_c = -C_G(V_G - V_{tn})$
$k'_n = \mu_n C_{OX}$, $\beta_n = \mu_n Cox\ (W/L)$	$R_n = 1 / \beta_n\,[(VDD - Vtn)]$, $R_p = 1 / \beta_p\,[(VDD - \lvert Vtp \rvert)]$
$I_D = I_S\left(e^{V_D/V_T} - 1\right)$, $\Psi_0 = V_T \ln\left(\frac{N_A N_D}{n_i^2}\right)$	$W = \left[\frac{2\varepsilon(\Psi_0 + V_R)}{q}\frac{N_D + N_A}{N_D N_A}\right]^{1/2}$
$C_j = A\left[\frac{q\varepsilon N_A N_D}{2(N_A + N_D)}\right]^{1/2}\left(\frac{1}{\sqrt{\Psi_0 + V_R}}\right)$	$W \cong x_p = \left[\frac{2\varepsilon(\Psi_0 + V_R)}{qN_A}\right]^{1/2}$, $W \cong x_n = \left[\frac{2\varepsilon(\Psi_0 + V_R)}{qN_D}\right]^{1/2}$
$C_{SB} = C_j\,A_{Sbot} + C_{jsw}\,P_{Ssw}$ $C_{DB} = C_j\,A_{Dbot} + C_{jsw}\,P_{Dsw}$	$C_{GS} = \frac{1}{2}\,C_G$ $C_{GD} = \frac{1}{2}\,C_G$
$t_f = 2.2\,\tau_n$, $t_r = 2.2\,\tau_p$ $t_p = 0.35(\tau_n + \tau_p)$	DRAM: $t_h = (Cs / I_L)(\Delta Vs)$ $f_{refresh} = 1 / 2t_h$

region	nMOS equations	pMOS equations
Cutoff	$I_D = 0$	$I_D = 0$
Triode	$I_D = \frac{\mu_n C_{OX}}{2}\frac{W}{L}\left[2(V_{GS} - V_m)V_{DS} - V_{DS}^2\right]$	$I_D = \frac{\mu_n C_{OX}}{2}\frac{W}{L}\left[2(V_{SG} - \lvert V_{tp} \rvert)V_{SD} - V_{SD}^2\right]$
Saturation	$I_D = \frac{\mu_n C_{OX}}{2}\frac{W}{L}(V_{GS} - V_m)^2$	$I_D = \frac{\mu_n C_{OX}}{2}\frac{W}{L}(V_{SG} - \lvert V_{tp} \rvert)^2$

Constants

kT = 0.026 eV, at room temperature
k = 8.62x10-5 eV/K, Boltzman's constant
V_T = 0.026 V, thermal voltage
q=1.6x10^{-19} C (coulombs)
n_i = 1.45x10^{10} cm^{-3}, Si at room temperature
ε_0 = 8.85x10^{-14} F/cm
ε_{ox} = (3.9) 8.85x10^{-14} F/cm
ε_{si} = (11.8) 8.85x10^{-14} F/cm

Quadratic Equation:

$ax^2 + bx + c = 0 \rightarrow x = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a}$

DeMorgan's Rules

(a * b)' = a' + b'
(a + b)' = a' * b'

Useful Logic Properties

1 + x = 1 0 + x = x
1 * x = x 0 * x = 0
x + x' = 1 x * x' = 0
a * a = a a + a = a
ab + ac = a (b+c)

properties which can be proven

(a+b)(a+c) = a+bc a + a'b = a + b
a + ab +ac = a

References

MOSFETs are discussed in a large number of books and an even larger number of journal articles. All of the books listed below contain excellent discussions of MOSFET characteristics. A few select journal articles have also been listed to aid the reader in performing a literature search that starts with some original papers.

[1] Antognetti and G. Massobrio (eds.), Semiconductor Device Modelling with SPICE,McGraw-Hill, New York, 1988.
[2] J.R. Brews, W. Fichtner, E.H. Nicollian and S.M. Sze, "Generalized guide for MOSFET Miniaturization",*IEEE Electron Device Letters,* vol. EDL-1, pp. 2-4, 1980.
[3] J.Y. Chi and R.P. Holstrom, "Constant voltage scaling of FET's for high frequency and high power applications", *Solid-State Electronics,* vol. 26, pp. 667-670, July, 1983.
[4] P.E. Cottrell, R.R. Troutman, and T.H. Ning, "Hot-Electron Emission in N-Channel IGFET's",*IEEE Trans. Electron Devices,* vol. ED-26, pp. 520-532, April, 1979.
[5] M.J. Deen and Z.P. Zuo, "Edge Effects in Narrow-Width MOSFET's", *IEEE Trans. Electron Devices,* vol. 38, pp. 1815-1819, August, 1991.
[6] R.H. Dennard, et. al, "Design of ion-implanted MOSFETs with very small physical dimensions",*IEEE J. Solid-State Circuits,* vol. SC-9, pp. 256-268, October, 1974.
[7] D. A. Divekar, FET Modeling for Circuit Simulation, Kluwer Academic Publishers, Boston,1988.
[8] D. Foty, MOSFET Modelling with SPICE, Prentice-Hall, Upper Saddle River, NJ, 1997.

UNIT No 2: Physical Structure and Fabrication of CMOS IC

1 PHYSICAL STRUCTURE OF ENHANCEMENT PMOS TRANSISTOR

Q1. *Draw the Physical Structure of Enhancement PMOS Transistor.*

Answer:

PMOS physical structure:

- p-substrate
- n-well (bulk)
- p+ source/drain
- gate oxide (SiO_2)
- polysilicon gate
- CVD oxide
- metal 1

PMOS layout representation:

- Implicit layers:
  - oxide layers
- Drawn layers:
  - n-well (bulk)
  - n+ regions
  - polysilicon gate
  - oxide contact cuts
  - metal layers

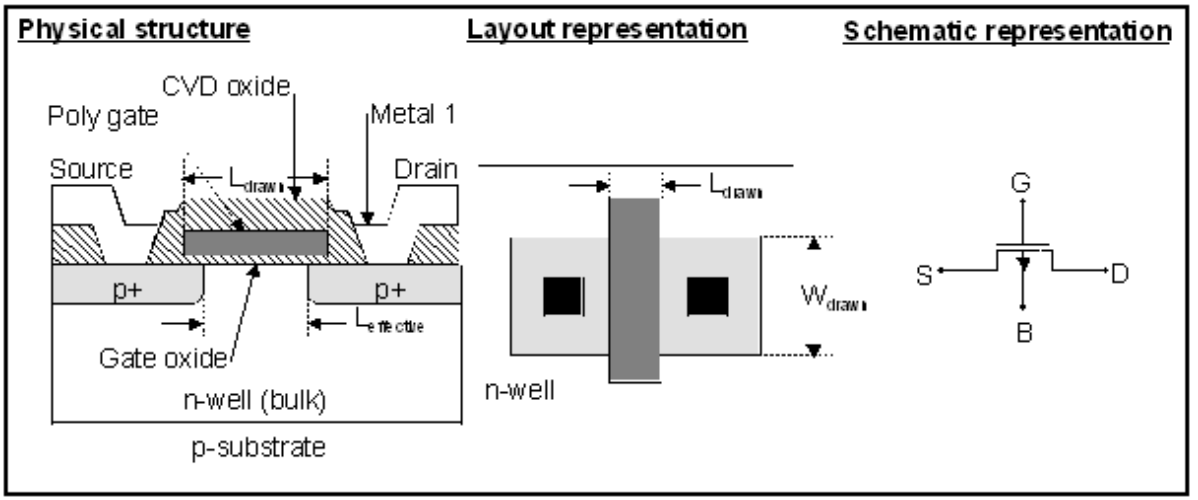


Figure 2.1: Physical Structure of PMOS Transistor

Q2. *Draw the Physical Structure of Enhancement NMOS Transistor.*

Answer:

NMOS physical structure:

- p-substrate
- n+ source/drain
- gate oxide (SiO_2)
- polysilicon gate
- CVD oxide
- metal 1

NMOS layout representation:

- Implicit layers:
  - oxide layers
  - substrate (bulk)
- **Drawn layers:**
  - n+ regions
  - polysilicon gate
  - oxide contact cuts
  - metal layers

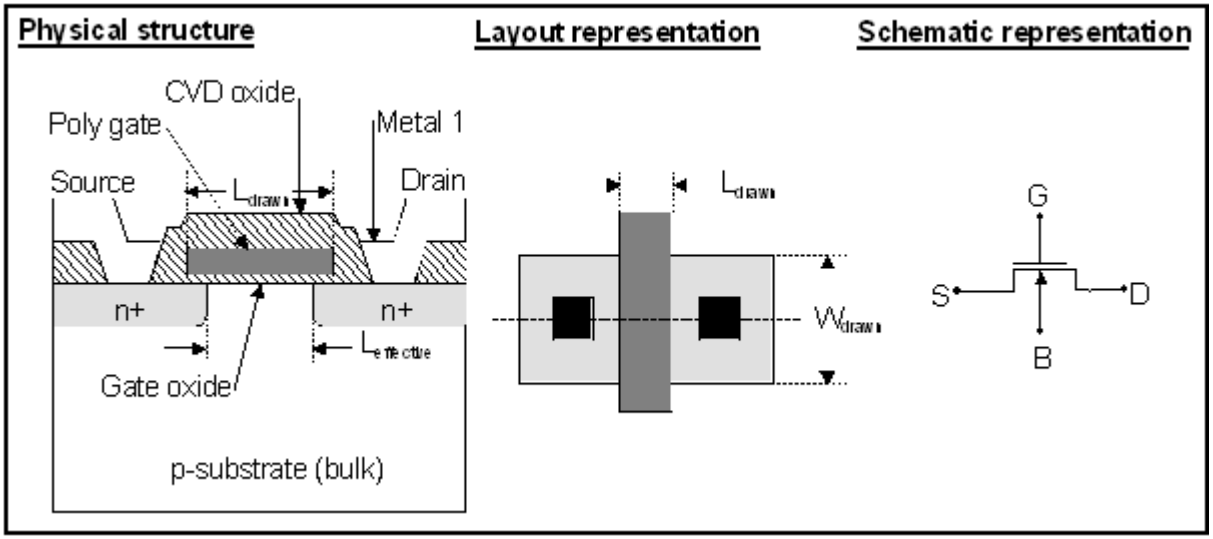
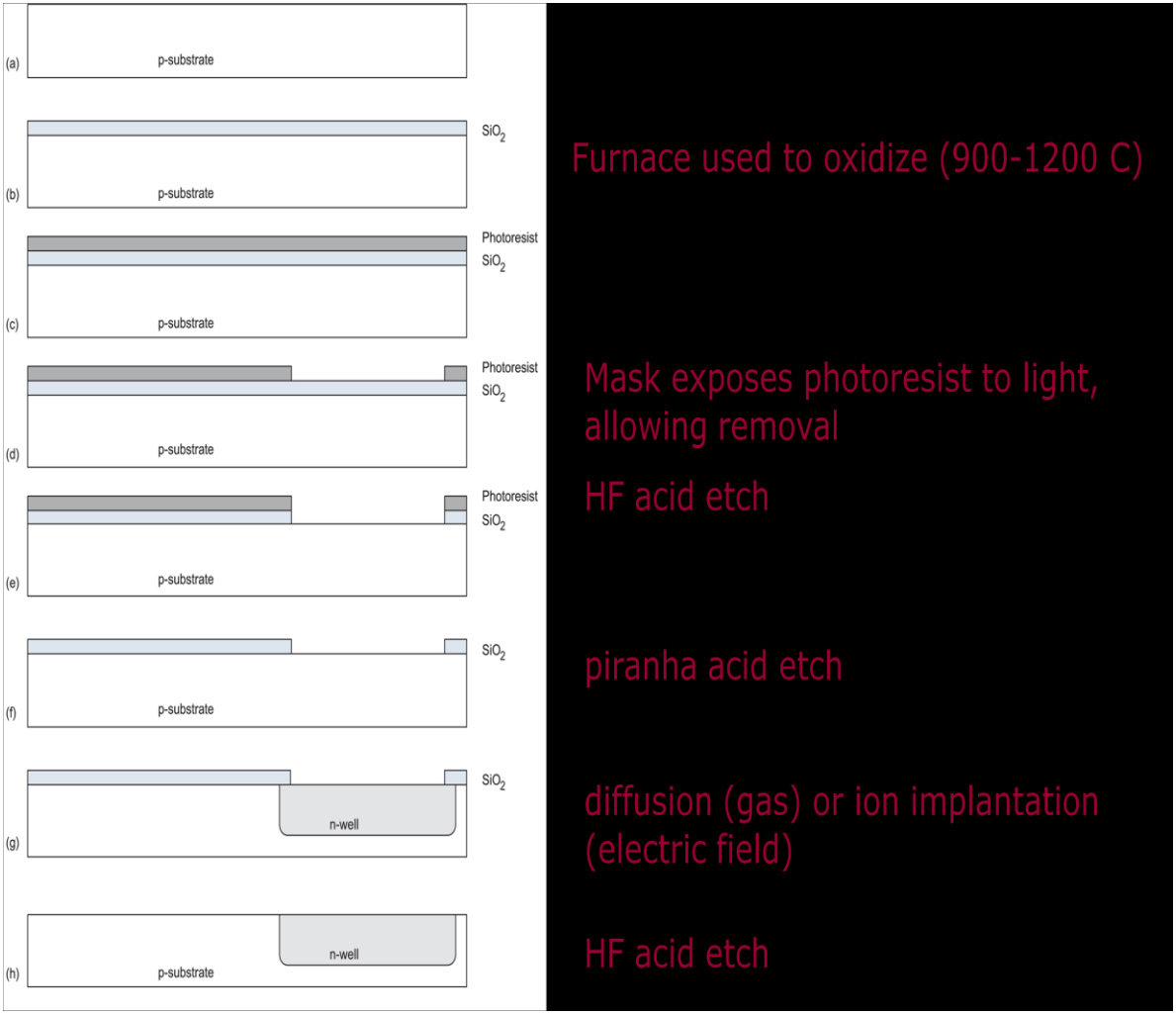
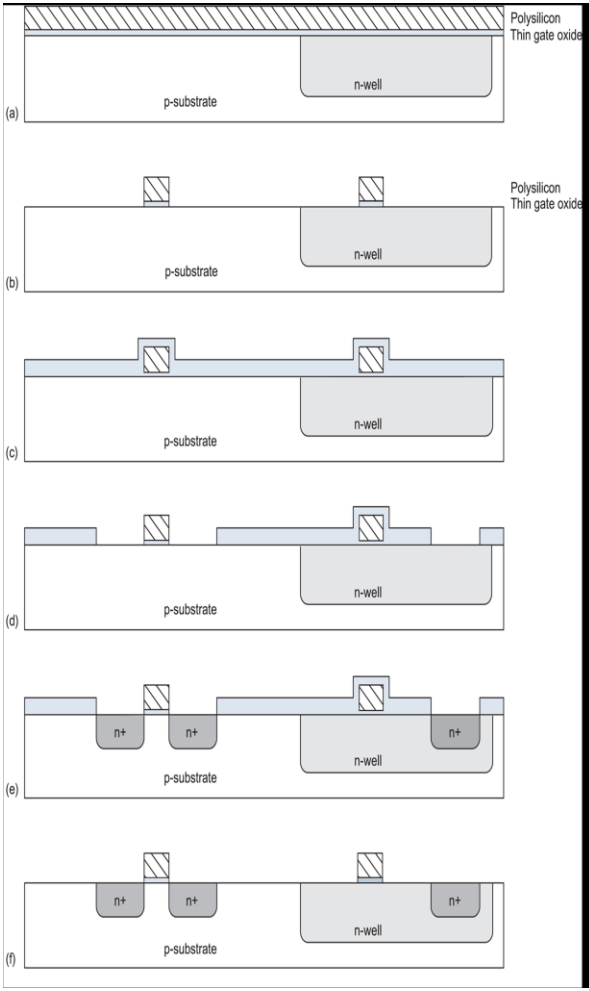


Figure 2.2: Physical Structure of PMOS Transistor

Q3. *Draw and explain the N-Well Process.*

Answer:





Heavy doped poly is grown with gas in furnace (chemical vapor deposition)

Masked used to pattern poly

Poly is not affected by ion implantation

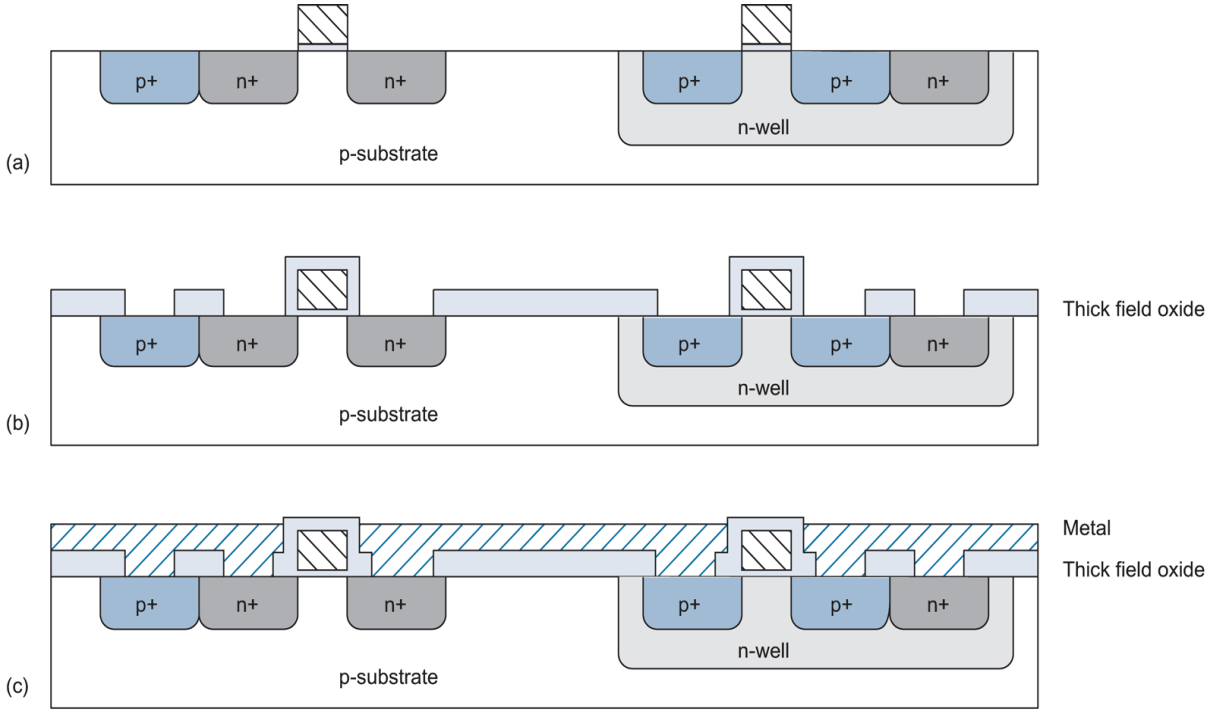
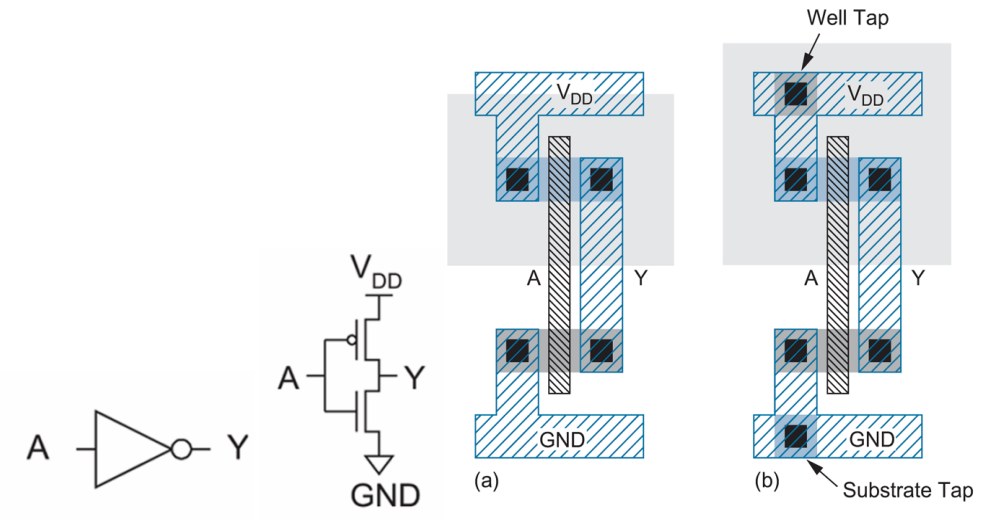


Figure 2.3: N-Well Process

Q4. *Draw schematic and Physical Layout of CMOS Inverter.*

Answer:



Symbol Schematic Physical Layout

Figure 2.4: CMOS Inverter

Q5. *Draw Basic Physical Design of Simple Logic Gates.*

Answer:

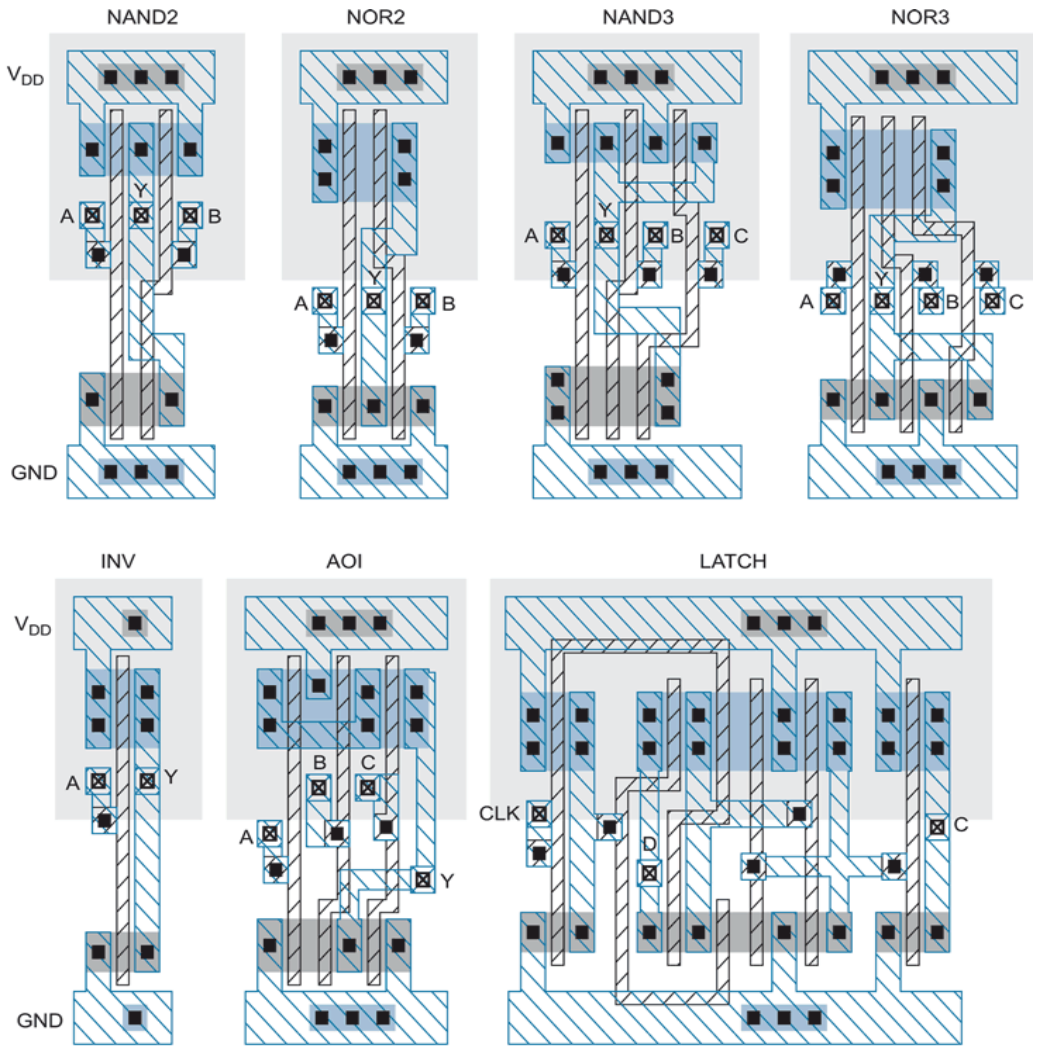


Figure 2.5: Layout of Basic Gates

Q6. *Draw Stick Diagram of CMOS Inverter and two input NAND Gate.*

Answer:

- A stick diagram is a graphical view of a layout.
- Does show all components/vias (except possibly tub ties), relative placement.
- Does not show exact placement, transistor sizes, wire lengths, wire widths, tub boundaries.
- Represents relative positions of transistors
- *Stick diagrams* help plan layout quickly
    - Need not be to scale
    - Draw with color pencils or dry-erase markers

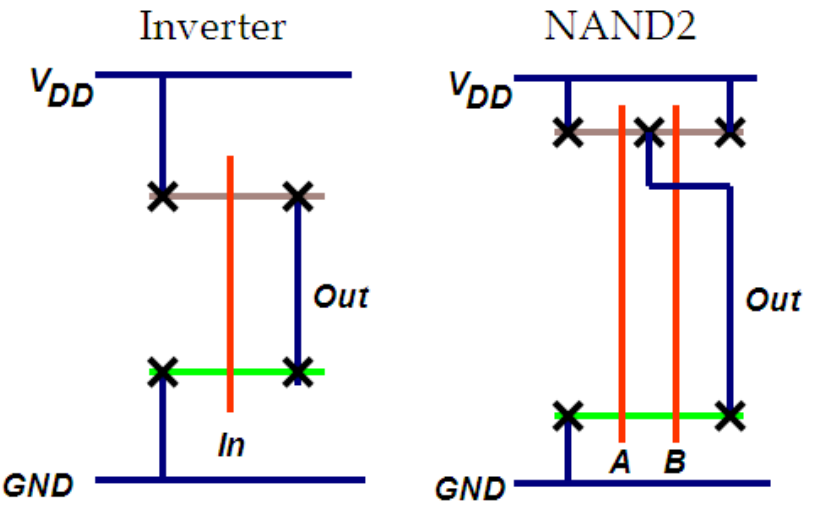


Figure 2.6: Stick diagram of Inverter and NAND Gate

Q7. *Draw Twin-well process*

Answer:

- **Twin-well process**
  - n+ or p+ substrate plus a lightly doped epi-layer (latchup prevention)
  - wells for the n- and p-transistors
  - Advantages, simultaneous optimization of p- and n-transistors:
    - threshold voltages
    - body effect
    - gain

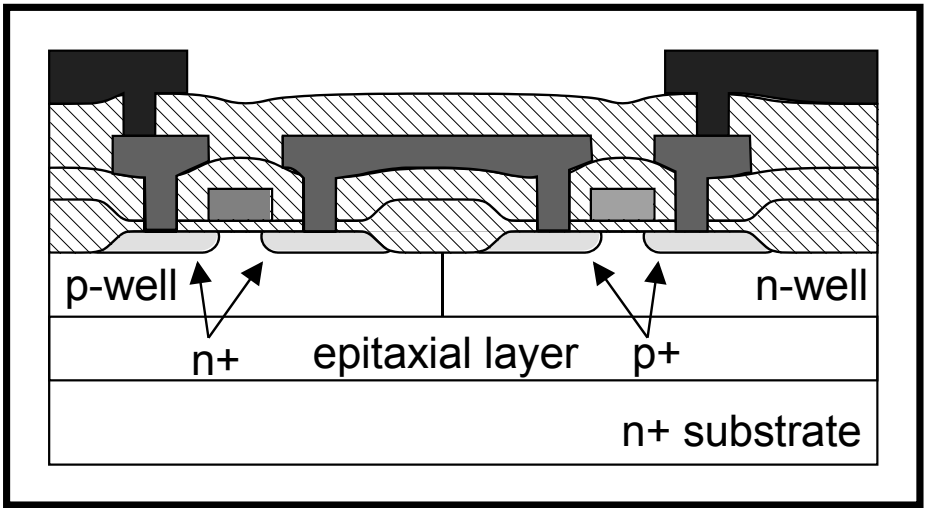


Figure 2.7: Twin-well process

Q8. *Write a short note on Silicon On Insulator (SoI).*

Answer:

- **Silicon On Insulator (SOI)**
  - Islands of silicon on an insulator form the transistors

    Advantages:
  - No wells ⇒ denser transistor structures
  - Lower substrate capacitances
  - Very low leakage currents
  - No FOX FET exists between unrelated devices
  - No latchup
  - No body-effect:
  - Radiation tolerance

    Disadvantages:
  - Absence of substrate diodes (hard to implement protection circuits)
  - Higher number of substrate defects ⇒ lower gain devices
  - More expensive processing

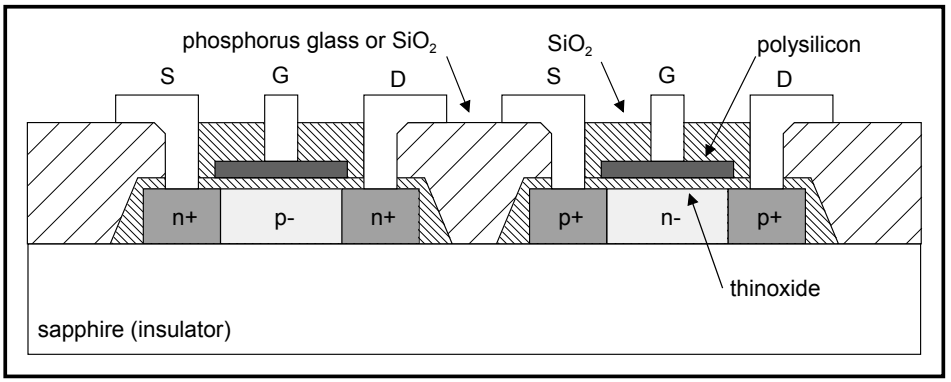
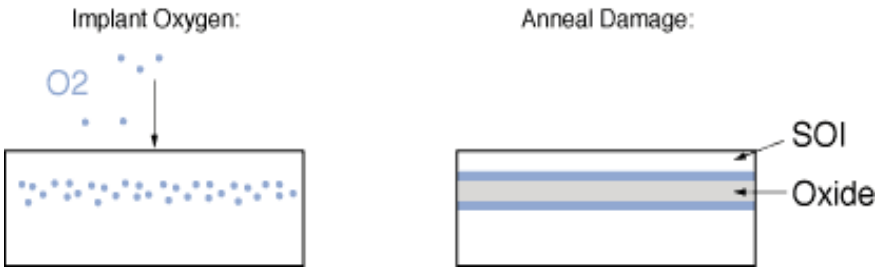


Figure 2.8: SoI Process

- SOI wafers can also be manufactured by a method called: Separation by Implantation of Oxygen (SIMOX)
- The starting material is a silicon wafer where heavy doses of oxygen are implanted
- The wafer is annealed until a thin layer of SOI film is formed
- Once the SOI film is made, the fabrication steps are similar to those of a bulk CMOS process



Q8. *Explain latch up Effect.*

Answer:

Latch-up Effect:

A byproduct of the Bulk CMOS structure is a pair of parasitic bipolar transistors. The collector of each BJT is connected to the base of the other transistor in a positive feedback structure. A phenomenon called latchup can occur when (1) both BJT's conduct, creating a low resistance path between Vdd and GND and (2) the product of the gains of the two transistors in the feedback loop, b1 x b2, is greater than one. The result of latchup is at the minimum a circuit malfunction, and in the worst case, the destruction of the device.

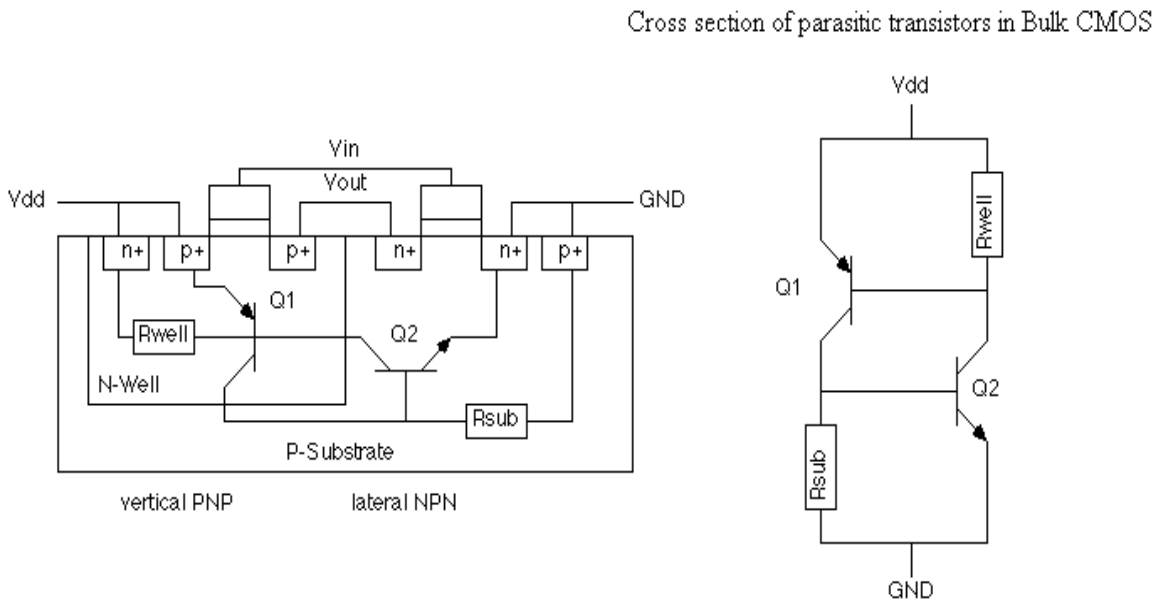


Figure 2.9: Latch Up Effect

Latchup may begin when Vout drops below GND due to a noise spike or an improper circuit hookup (Vout is the base of the lateral NPN Q2). If sufficient current flows through Rsub to turn on Q2 (I Rsub > 0.7 V), this will draw current through Rwell. If the voltage drop across Rwell is high enough, Q1 will also turn on, and a self-sustaining low resistance path between the power rails is formed. If the gains are such that b1 x b2 > 1, latchup may occur. Once latchup has begun, the only way to stop it is to reduce the current below a critical level, usually by removing power from the circuit.

The most likely place for latchup to occur is in pad drivers, where large voltage transients and large currents are present.

Preventing latchup:

A. Fab/Design Approaches

1. Reduce the gain product b1 x b1
    - move n-well and n+ source/drain farther apart increases width of the base of Q2 and reduces gain beta2 > also reduces circuit density
    - buried n+ layer in well reduces gain of Q1
2. Reduce the well and substrate resistances, producing lower voltage drops
    - higher substrate doping level reduces Rsub
    - reduce Rwell by making low resistance contact to GND
    - guard rings around p- and/or n-well, with frequent contacts to the rings, reduces the parasitic resistances

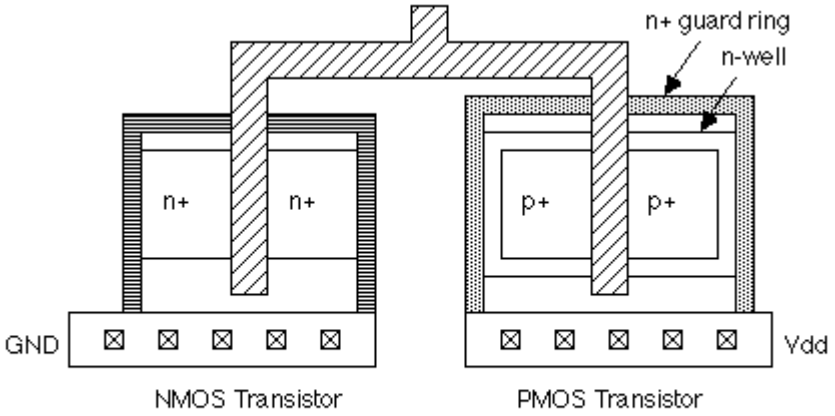


Figure 2.10: Guard Rings

B. Systems Approaches

1. Make sure power supplies are off before plugging a board. A "hot plug in" of an unpowered circuit board or module may cause signal pins to see surge voltages greater

than 0.7 V higher than Vdd, which rises more slowly to is peak value. When the chip comes up to full power, sections of it could be latched.

2. Carefully protect electrostatic protection devices associated with I/O pads with guard rings. Electrostatic discharge can trigger latchup. ESD enters the circuit through an I/O pad, where it is clamped to one of the rails by the ESD protection circuit. Devices in the protection circuit can inject minority carriers in the substrate or well, potentially triggering latchup.
3. Radiation, including x-rays, cosmic, or alpha rays, can generate electron-hole pairs as they penetrate the chip. These carriers can contribute to well or substrate currents.
4. Sudden transients on the power or ground bus, which may occur if large numbers of transistors switch simultaneously, can drive the circuit into latchup. Whether this is possible should be checked through simulation.

Summary:

There was an era, where computers were such mammoth in size that to install them, easily a room space was required. But today they are so evolved that we can even carry them as notebooks easily. The innovation that made this possible was the concept of Integrated Circuits. In Integrated Circuits, a large number of active and passive elements along with their interconnections are developed over a small silicon wafer typically of 50 by 50 mils in cross section. The basic processes followed for production of such circuits include epitaxial growth, masked impurity diffusion, oxide growth, and oxide etching, using photolithography for making pattern. The components over the wafer include resistors, transistors, diodes, capacitors etc. The most complicated element to manufacture over IC's is transistors. Transistors are of various types such as CMOS, BJT, FET. We choose the type of transistor technology to be implemented over an IC based on requirements. In this article let us get familiarized with the concept of CMOS fabrication (or) fabrication of transistors as CMOS.

References

[1] L.A. Akers and J.J. Sanchez, "Threshold Voltage Models of Short, Narrow and Small Geometry MOSFET's: A Review", *Solid-State Electronics,* vol. 25, pp. 621-641, July, 1982.

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[4] J.Y. Chi and R.P. Holstrom, "Constant voltage scaling of FET's for high frequency and high power applications", Solid-State Electronics, vol. 26, pp. 667-670, July, 1983.

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[8] D. A. Divekar, FET Modeling for Circuit Simulation, Kluwer Academic Publishers, Boston,1988.

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UNIT No 3: **Logic Design with MOSFETs**

Unit-3

Que 1: Explain how MOSFETs acts as an Ideal Switches ?

Answer:

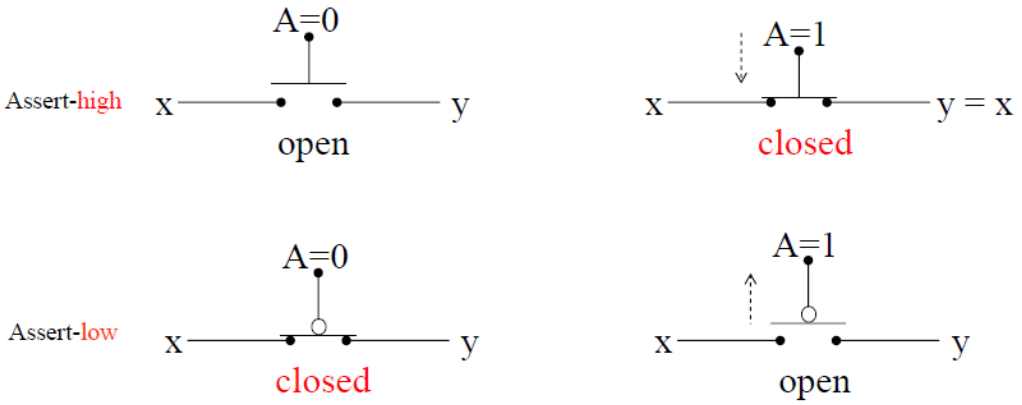


Figure 3.1: Ideal Switches

MOS Transistor:

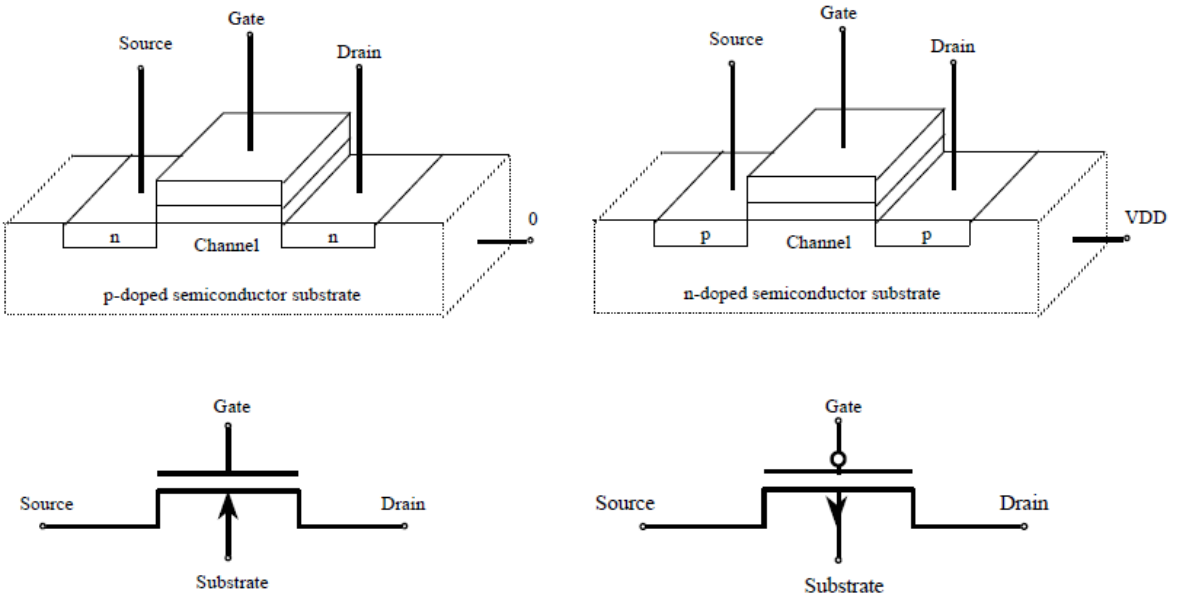


Figure 3.2: NMOS AND PMOS TRANSISTOR

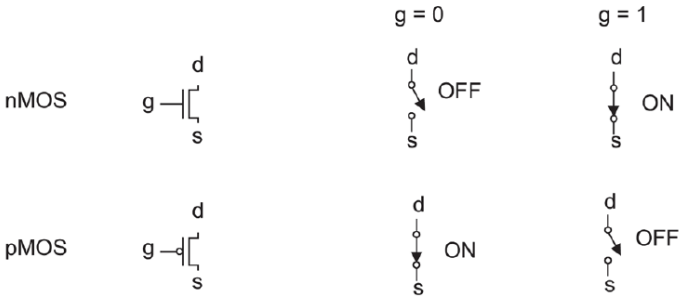


Figure 3.3: Transistors Symbols and switch level models

Que 2: ***Explain Connection and behaviour of series and parallel transistors.***

Answer:

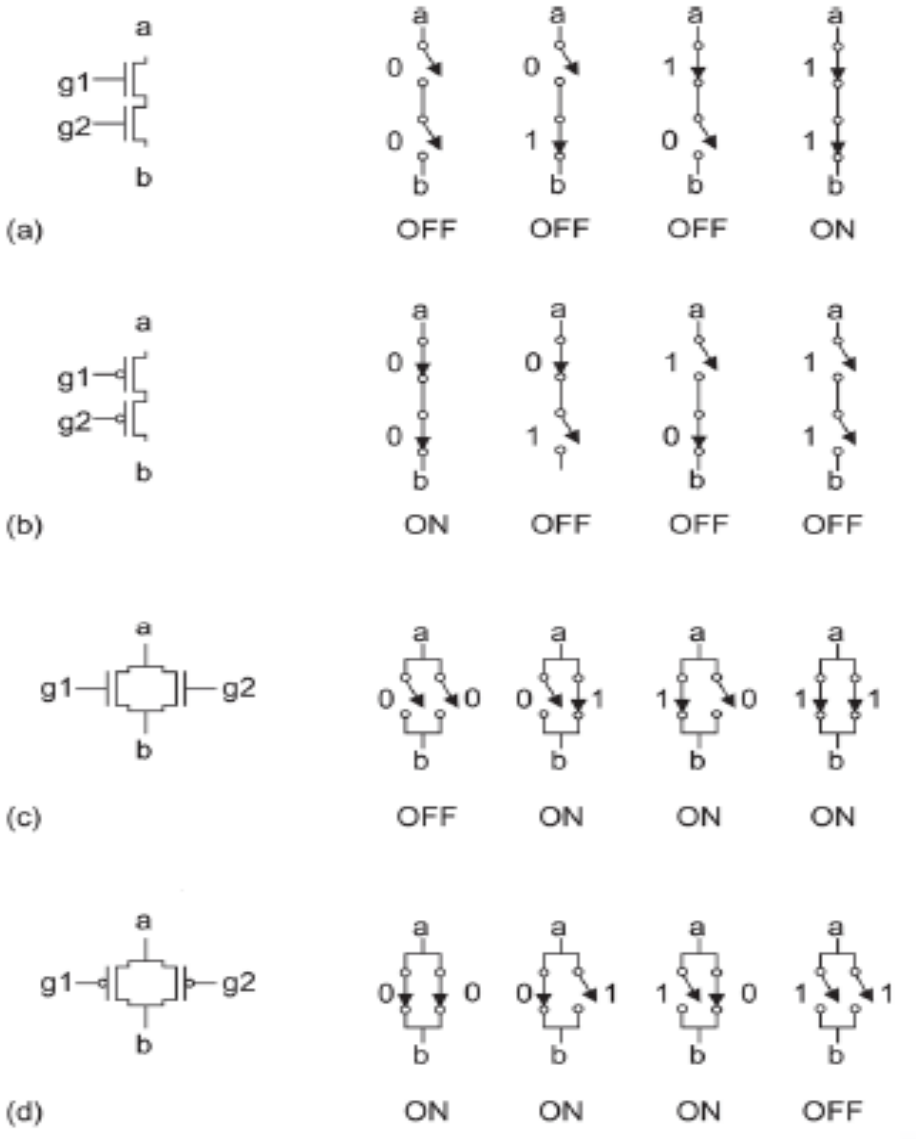


Figure 3.4: Connection and behavior of series and parallel transistors

Table 01: NAND Gate Truth Table				
Inputs		Operation		Output
A	B	Pull Down Network	Pull Up Network	Y
0	0	OFF	ON	1
0	1	OFF	ON	1
1	0	OFF	ON	1
1	1	ON	OFF	0

Table 02: NOR Gate Truth Table				
Inputs		Operation		Output
A	B	Pull Down Network	Pull Up Network	Y
0	0	OFF	ON	1
0	1	ON	OFF	0
1	0	ON	OFF	0

1	1	ON	OFF	0

NAND Gate NOR Gate

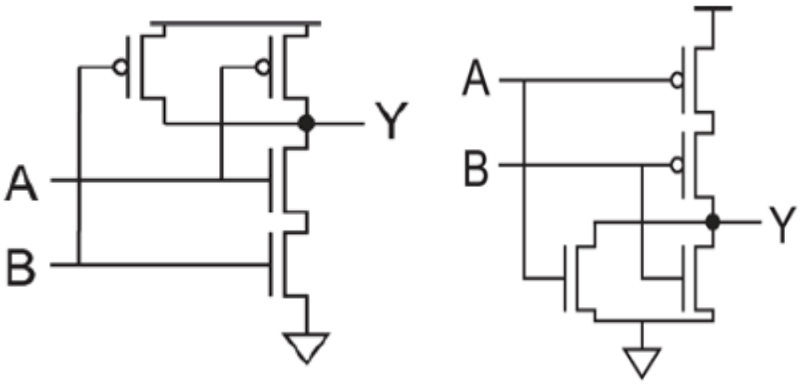


Figure 3.5: Schematic of NAND and NOR Gate

Q 3: *Write a short note on Compound Gates.*

Answer: The following logic diagram shows an inefficient discrete gate implementation of AOI (AND OTR INVERT Logic) .But with the help of complementary Logic circuit the same logic can be implemented with less number of transistors.

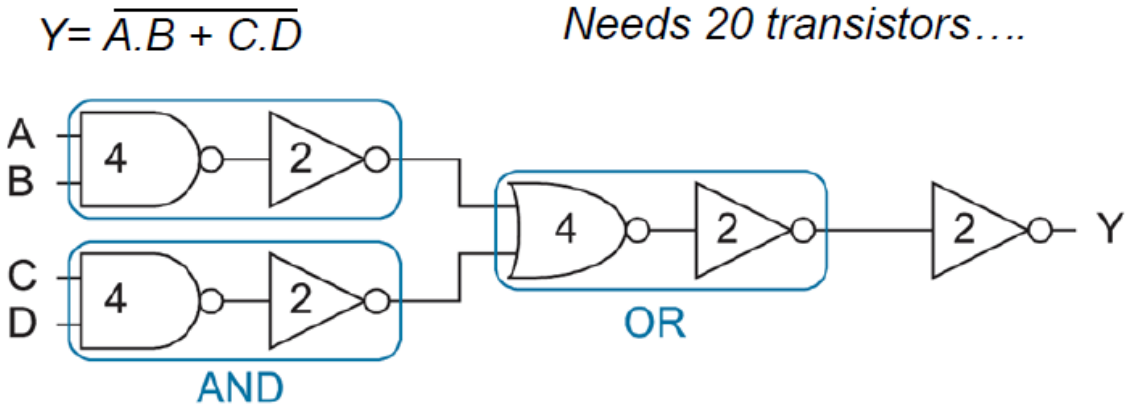


Figure 3.6: inefficient discrete gate implementation of AOI (AND OTR INVERT Logic)

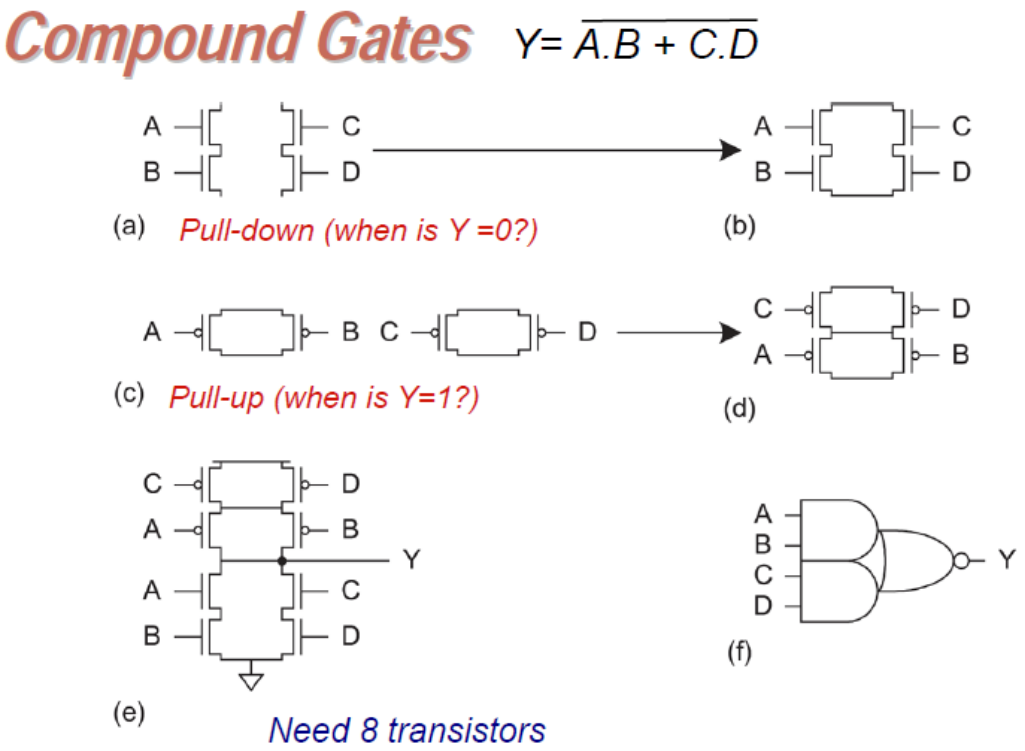


Figure 3.7: Efficient Implementation [1]

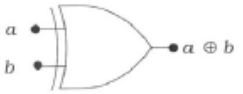
An important example of using an AOI circuit is constructing Exclusive-OR (XOR) and Exclusive-NOR circuits

$$a \oplus b = \bar{a} \cdot b + a \cdot \bar{b}$$

$$\overline{a \oplus b} = a \cdot b + \bar{a} \cdot \bar{b}$$

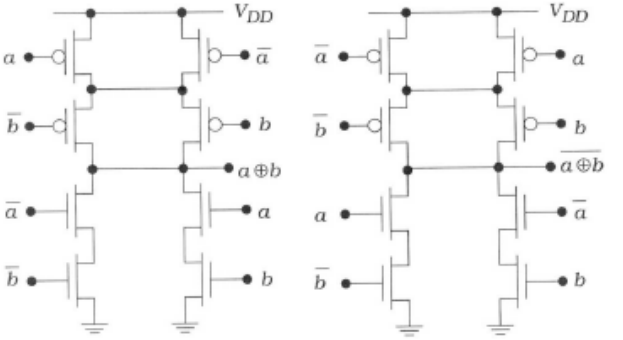
$$\Rightarrow a \oplus b = \overline{\overline{(a \oplus b)}} = \overline{a \cdot b + \bar{a} \cdot \bar{b}}$$

$$\Rightarrow \overline{a \oplus b} = \overline{\bar{a} \cdot b + a \cdot \bar{b}}$$



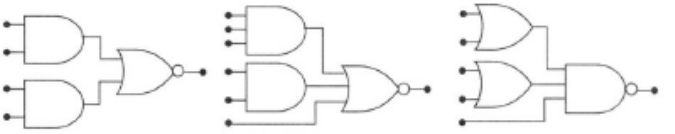
a	b	a ⊕ b
0	0	0
0	1	1
1	0	1
1	1	0

Figure XOR gate



(a) Exclusive-OR (b) Exclusive-NOR

Figure AOI XOR and XNOR gates



(a) AOI22 (b) AOI321 (c) AOI221

Figure General naming convention

Q 4: *Explain the working of Pass Transistors.*

Answer: Pass Transistors:

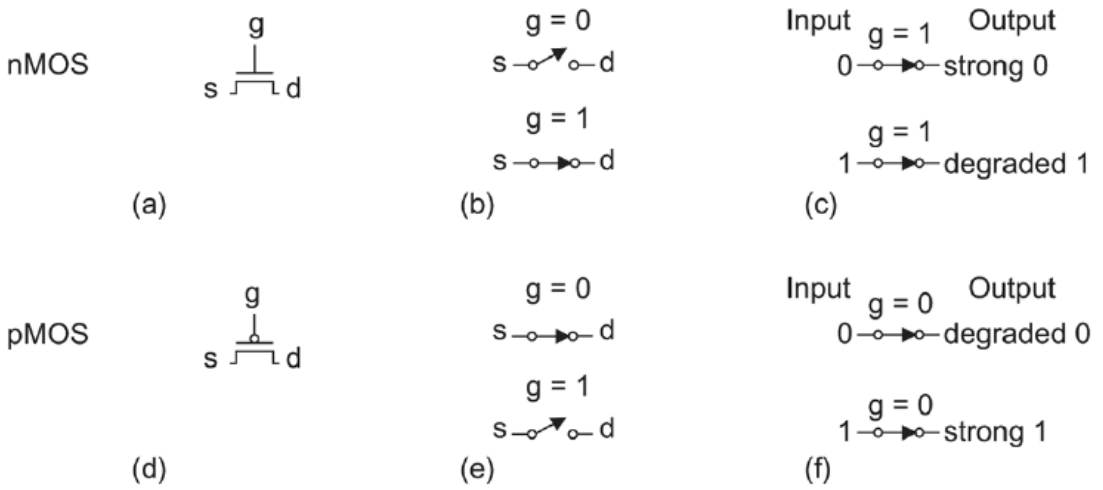


Figure 3.8: Pass Transistors

Q 5: *Explain the working of Transmission Gates.*

Answer:

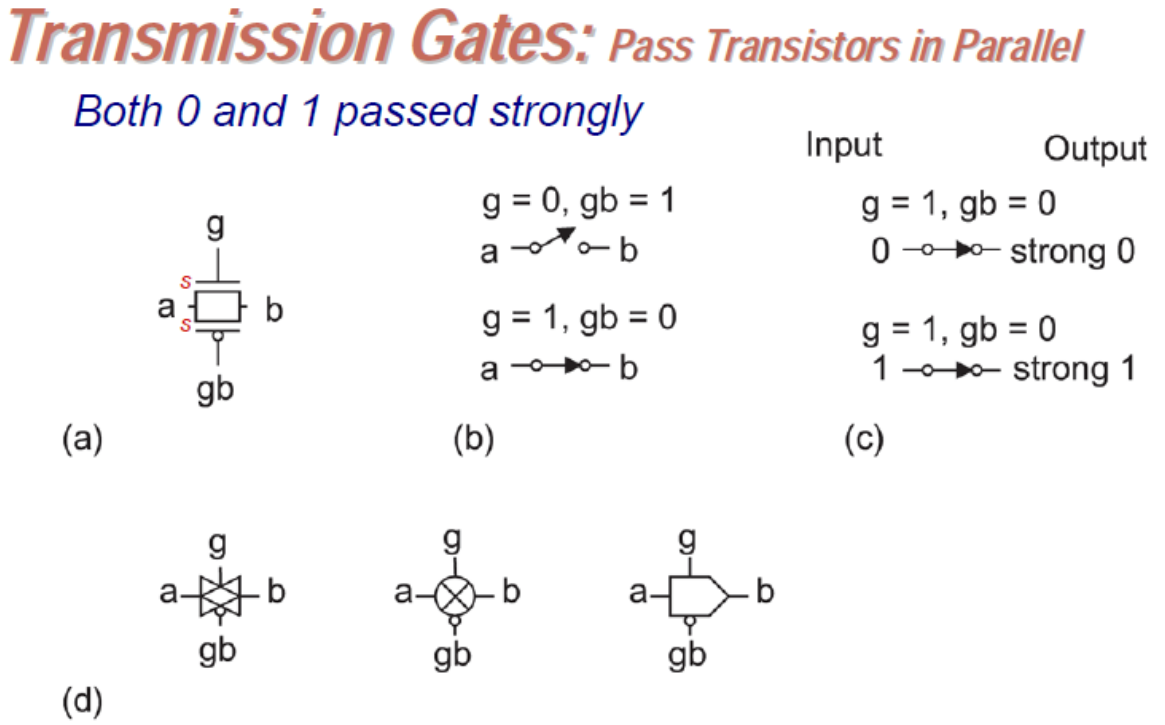


Figure 3.9: TG Gates

Q 6: Explain principle operation of Tri state buffer.

Answer: Tri-state Buffer:

Table 02: Truth Table for Tristate		
EN/$\overline{EN}$	**A**	**Y**
0/1	0	Z
0/1	1	Z
1/0	0	0
1/0	1	1

Figure 12: Tri-state Buffer

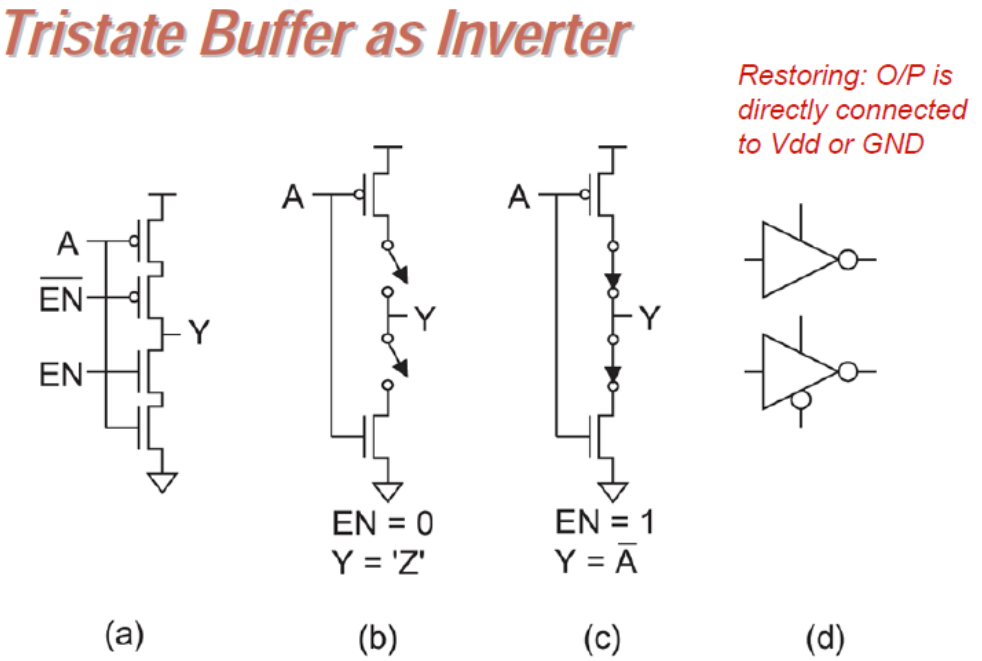
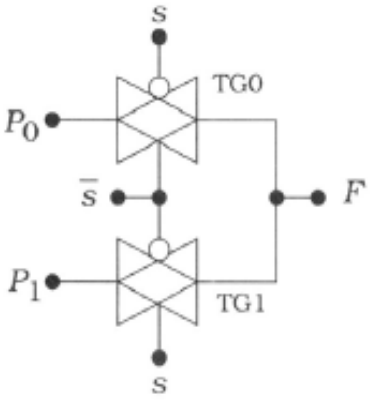


Figure 3.10: Tri-state Buffer as Inverter

Q 7: Implement Transmission Gate Based 2:1 Multiplexer:

Answer: Transmission Gate Based 2:1 Multiplexer:

$$F = P_0 \cdot \overline{s} + P_1 \cdot s$$

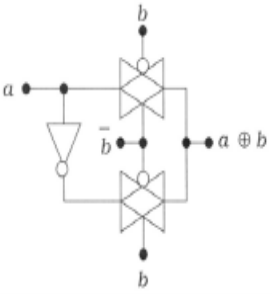


s	TG0	TG1	F
0	Closed	Open	P_0
1	Open	Closed	P_1

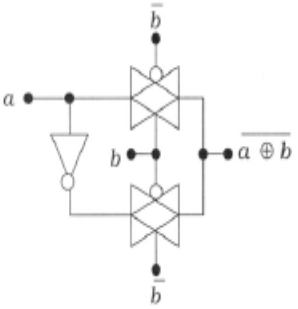
Q 8: Implement Transmission Gate Based XOR and XNOR gates.

Answer: Transmission Gate Based OR, Ex-or, Ex-nor Gates:

TG based XOR/XNOR



$$a \cdot \bar{b} + \bar{a} \cdot b = a \oplus b$$

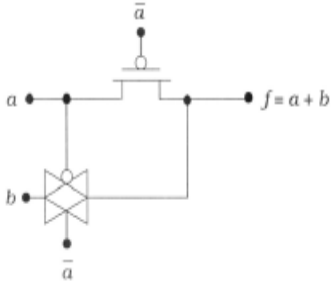


$$\overline{a \oplus b} = a \cdot b + \bar{a} \cdot \bar{b} = a \otimes b$$

(a) XOR circuit (b) XNOR circuit

Figure TG-based exclusive-OR and exclusive-NOR circuits

TG based OR gate



$$f = a \cdot (\bar{\bar{a}}) + \bar{a} \cdot b$$
$$= a + \bar{a} \cdot b$$
$$= a + b$$

Figure A TG-based OR gate

Q 9: Implement 2: 1Multiplexer with Transmission Gate.

Answer: Multiplexers:

- Connects one of n inputs to the output
- Used as data selectors

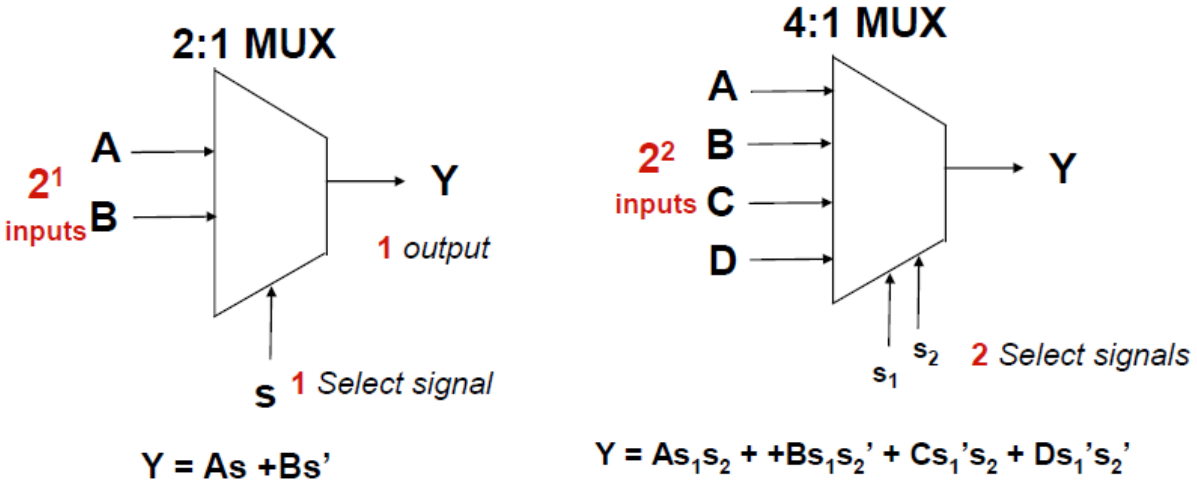


Figure 14: Multiplexer

Transmission Gate Multiplexer:

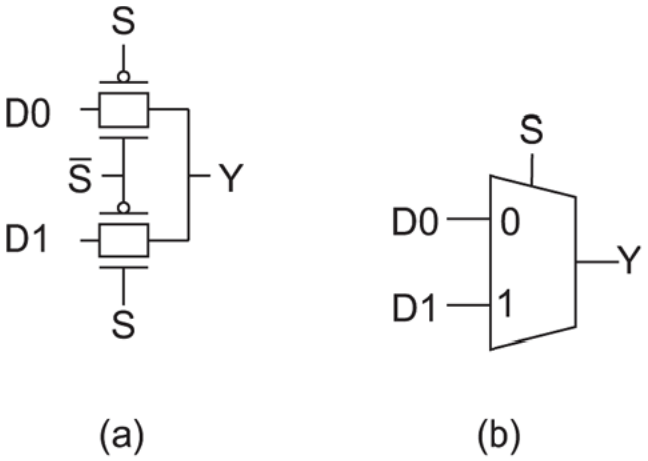
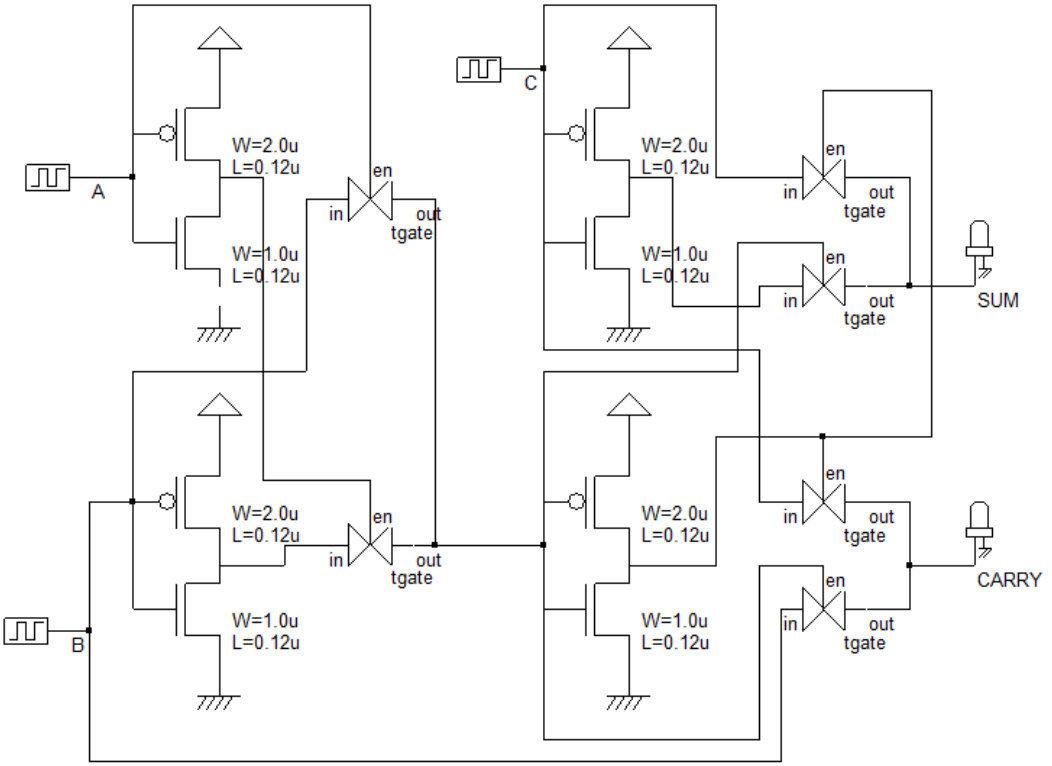


Figure 3.11: Multiplexer using Transmission Gate

Q 10: Design and implement 1-bit full adder using Transmission gate .

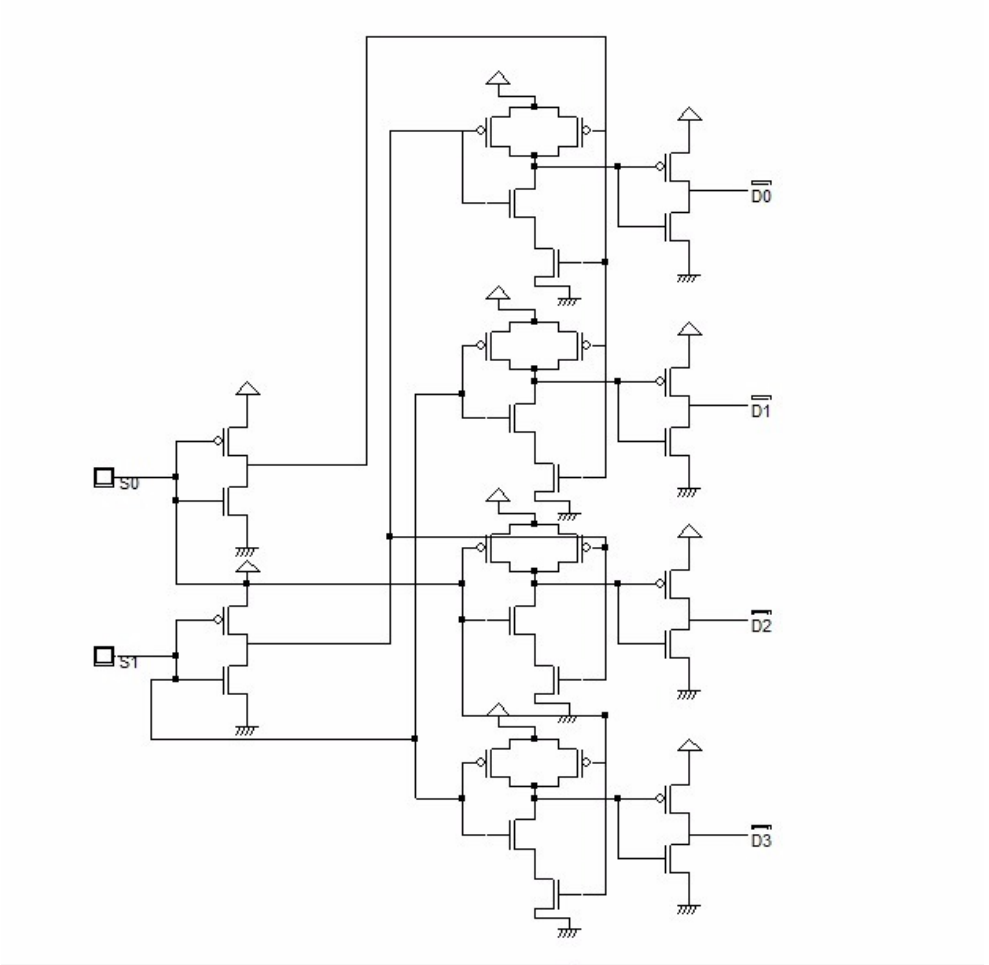
Answer:



Full Adder –Truth Table				
Input			Output	
A	B	Carry in	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Q 11. Design and implement 2:4 decoder using cmos.

Answer:


S0
S1
D0
D1
D2
D3

Summary:

Compound logic gates (sometimes Complex logic gate) are simple devices that function like a few basic logic gates combined. Typically made from a few levels of logic, those gates can be used in optimizing various circuits in terms of area and transistors, yielding better performance. This is especially true when development is restricted to a vendor's standard cell library. While some are rarely used by actual logic designers (simply due to their complexity), those gates are often used by optimization programs are able to make efficient use of such gates.

A Tri-state Buffer can be thought of as an input controlled switch with an output that can be electronically turned “ON” or “OFF” by means of an external “Control” or “Enable” (EN) signal input. This control signal can be either a logic “0” or a logic “1” type signal resulting in the Tri-state Buffer being in one state allowing its output to operate normally producing the required output or in another state were its output is blocked or disconnected. Then a tri-state buffer requires two inputs. One being the data input and the other being the enable or control input as shown**.**

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[1] L.A. Akers and J.J. Sanchez, “Threshold Voltage Models of Short, Narrow and Small Geometry MOSFET’s: A Review”, *Solid-State Electronics,* vol. 25, pp. 621-641, July, 1982.

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UNIT No 4: MOS Inverter Characteristics

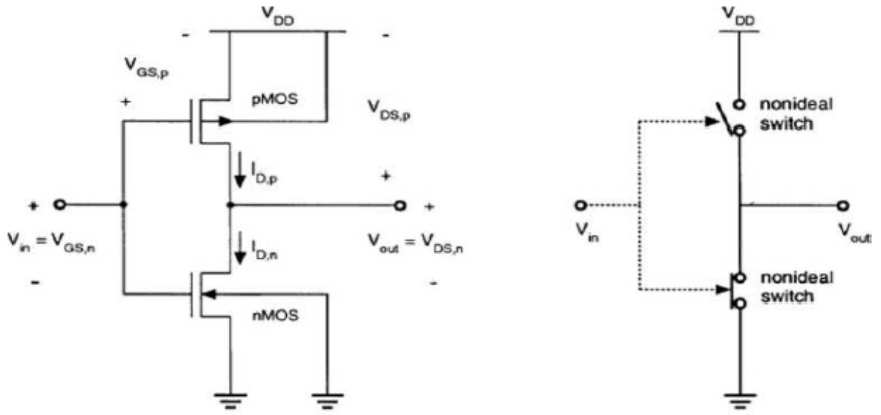
Question 1: Explain the principle of CMOS inverter with V-I wave forms and show all the five regions of operations. Assume VDD=5 V, Vtn= 1 V, Vtp= -1V

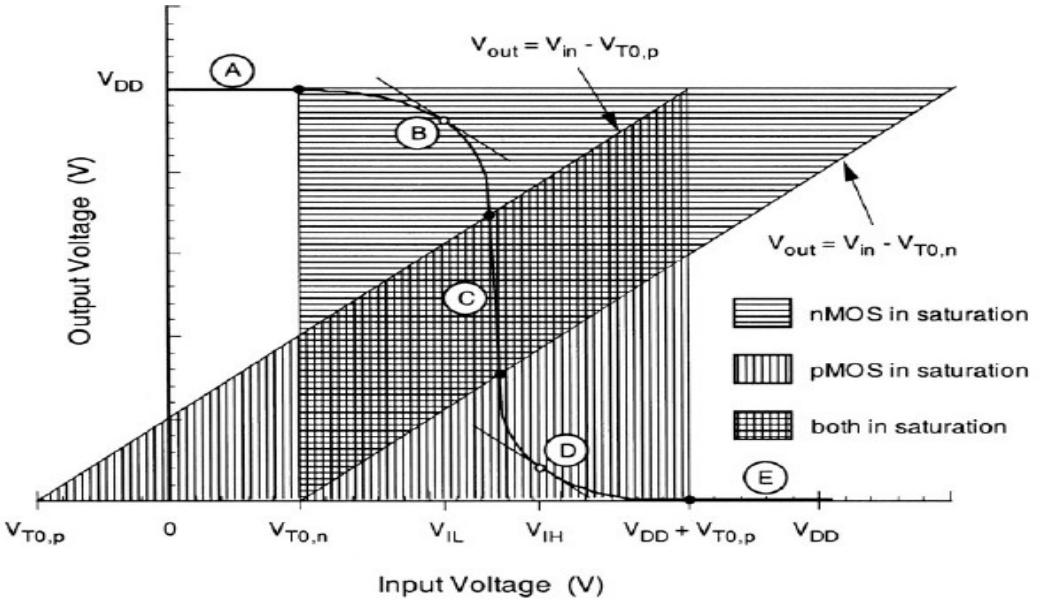
Answer:

- the CMOS inverter uses an NMOS and a PMOS transistor in a complementary push/pull configuration
- for a Logic "1" output, the PMOS=ON and the NMOS=OFF
- for a Logic "0" output, the PMOS=OFF and the NMOS=ON
- this configuration has two major advantages:

1) low static power consumption : due to one MOSFET always being off

2) a sharp and symmetric VTC profile giving full swing signals (1=V_{DD}, 0=V_{SS})





$$V_{GS,n} = V_{in}$$

$$V_{DS,n} = V_{out}$$

$$V_{GS,p} = -(V_{DD} - V_{in})$$

Region A

- let's assume V_{DD}=5v, $V_{T,n}$=1, $V_{T,p}$= -1 (V_{in} = 0v, V_{out} = 5v)

- When V_{in} = 0v, the output is V_{out}=V_{DD}

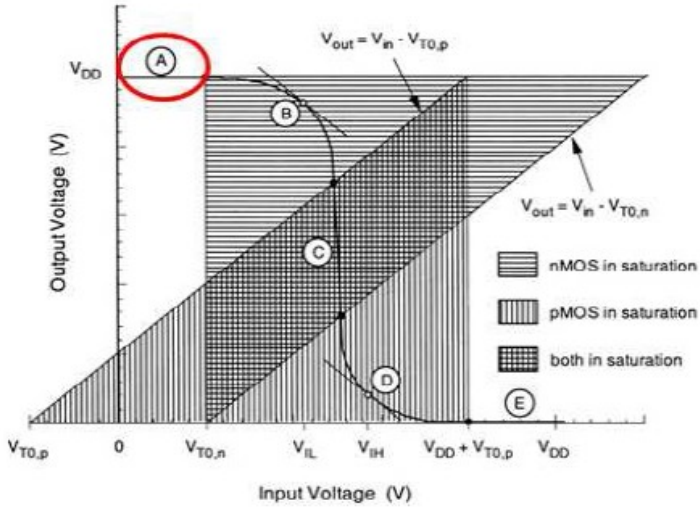
- the NMOS transistor is OFF since $V_{GS,n} \leq V_{T,n}$ (**cut-off**) i.e., 0 ≤ 1

- the NMOS drain current $I_{D,n}$=0

- the PMOS transistor is ON since $V_{GS,p} \leq V_{T,p}$ i.e., (0-5) ≤ -1

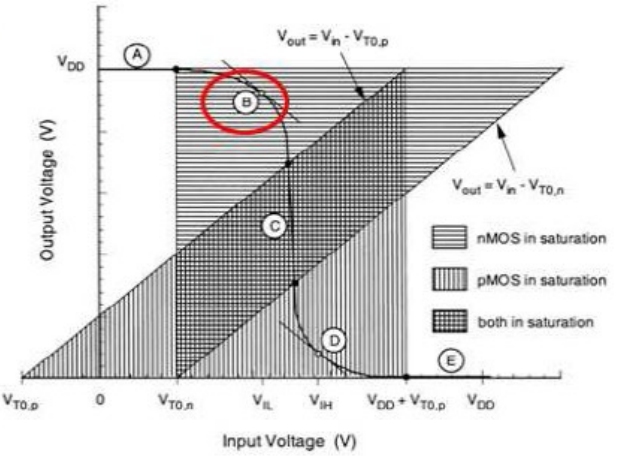
- the PMOS drain current $I_{D,p}$=0 since $I_{D,n}$=$I_{D,p}$

- since $V_{DS,p}$=0v, then the PMOS is in the ***linear*** *region* since: $V_{DS,p} > (V_{GS,p}-V_{T,p})$ i.e., 0 > (0-5) - (-1)



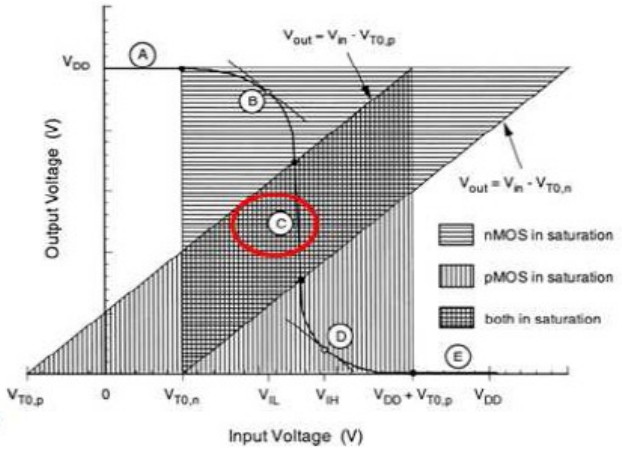
Region B

- Now let's move V_{in} above $V_{T,n}$ but below V_{th} (V_{in} ~= 1v, V_{out} ~=5v)
- the NMOS transistor turns ON since $V_{GS,n} \geq V_{T,n}$, i.e., $1 \geq 1$
- since $V_{DS,n}$ is still near V_{DD}, the NMOS goes directly into ***saturation*** since: $V_{DS,n} > (V_{GS,n}-V_{T,n})$ i.e., $(\sim 5) > 1-1$
- the PMOS transistor is still ON since $V_{GS,p} \leq V_{T,p}$ i.e., $\sim(1-5) \leq -1$
- the PMOS is still in the ***linear region*** since: $V_{DS,p} > (V_{GS,p}-V_{T,p})$ i.e., $(\sim 5-5) > (1-5) - (-1)$



Region C

- Now let's move to where $V_{in} = V_{out}$ (V_{in} ~= 2.5v, V_{out} ~=2.5v)
- This is defined as V_{th}
- the NMOS transistor is ON since $V_{GS,n} \geq V_{T,n}$ i.e., $2.5 \geq 1$
- the NMOS transistor is in ***saturation*** since $V_{DS,n} > (V_{GS,n}-V_{T,n})$ i.e., $\sim 2.5 > (2.5 - 1)$
- the PMOS transistor is ON since $V_{GS,p} \leq V_{T,p}$ i.e., $(2.5-5) \leq -1$
- the PMOS is in ***saturation*** since: $V_{DS,n} < (V_{GS,n}-V_{T,p})$ i.e., $(2.5-5) < (2.5-5) - (-1)$



Region D

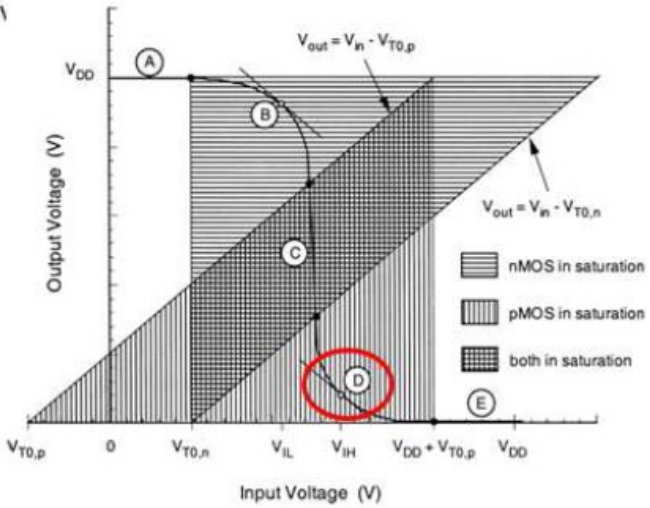
- Now let's move V_{in} above V_{th} but below (V_{DD}+\
(V_{in} ~= 4v, V_{out} ~=1v)

- the NMOS transistor is ON since
$V_{GS,n} \geq V_{T,n}$ i.e., $4 \geq 1$

- the NMOS transistor is in ***linear*** since
$V_{DS,n} < (V_{GS,n}-V_{T,n})$ i.e., ~1 < (4 - 1)

- the PMOS transistor is ON since
$V_{GS,p} \leq V_{T,p}$ i.e., (4-5) ≤ -1

- the PMOS is in ***saturation*** since:
$V_{DS,n} < (V_{GS,n}-V_{T,p})$ i.e., (1-5) < (4-5) - (-1)



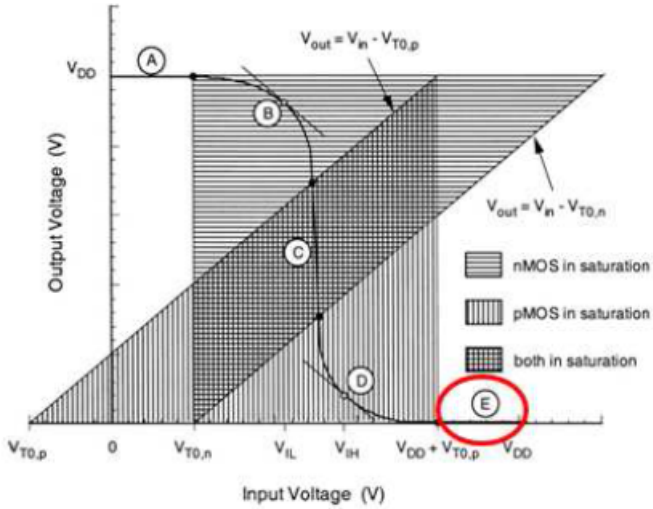
Region E

- Now let's move V_{in} above (V_{DD}+$V_{T,p}$)
(V_{in} = 5v, V_{out} = 0v)

- the NMOS transistor is ON since
$V_{GS,n} \geq V_{T,n}$ i.e., $5 \geq 1$

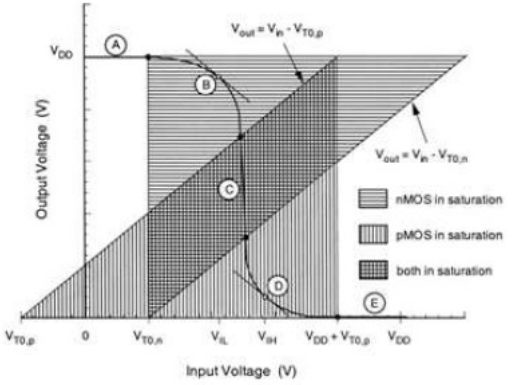
- the NMOS transistor is in ***linear*** since
$V_{DS,n} < (V_{GS,n}-V_{T,n})$ i.e., ~0 < (5 - 1)

- the PMOS transistor is OFF since
$V_{GS,p} \geq V_{T,p}$ i.e., (5-5) ≥ -1 (***cut-off***)



Summary

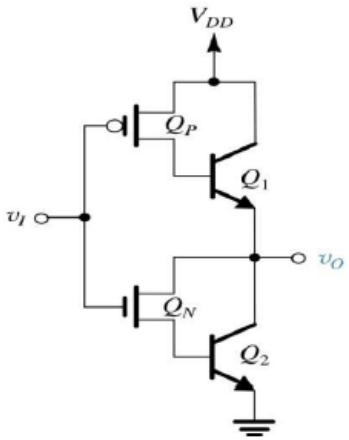
Region	NMOS	PMOS
A	cut-off	linear
B	saturation	linear
C	saturation	saturation
D	linear	saturation
E	linear	cut-off



Q 2: Explain Bi-CMOS inverters circuit diagram and explain its operation. Draw all the four versions of Bi-CMOS inverters.

Answer:

➢ Introduction to Bi-CMOS Inverter



BiCMOS is a logic family that combines Bipolar and CMOS devices into single integrated circuits

- Higher speed
- Lower power dissipation
- Higher packing densities

BICOMOS logic gates:

- BiCMOS is a VLSI technology that unites Bipolar and CMOS circuits on the same chip to combine the advantages of both logic families. Consequently, Bi-CMOS digital gates enjoys both, the low-power, high-input-impedance and wide-noise-margin of CMOS and the high current-driving-capability and high-speed-switching of BJT
- Furthermore, since Bi-CMOS technology is well suited for implementing high performance analog circuits, realization of both analog and digital functions on the same IC chip or 'system on a chip' becomes attainable.
- BiCMOS Logic Gates are especially suitable for large capacitive loads (greater than 0.5 pF or so) or when the logic gate has to drive a number of other logic gates, requiring large amount of output current.
- Modern BiCMOS, invented by intel, was available in the market in 1992 and was eventually used to construct VLSI chips for personal computers.

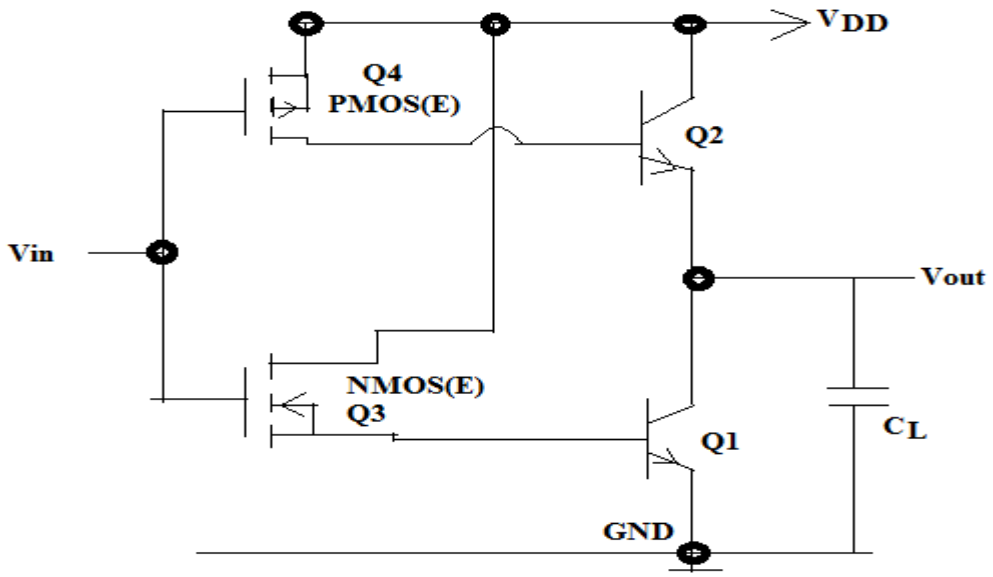
BiCMOS

Advantages:

- Lower power dissipation than bipolar
- Improved speed in comparison to CMOS
- Larger current drive than CMOS

Disadvantages:

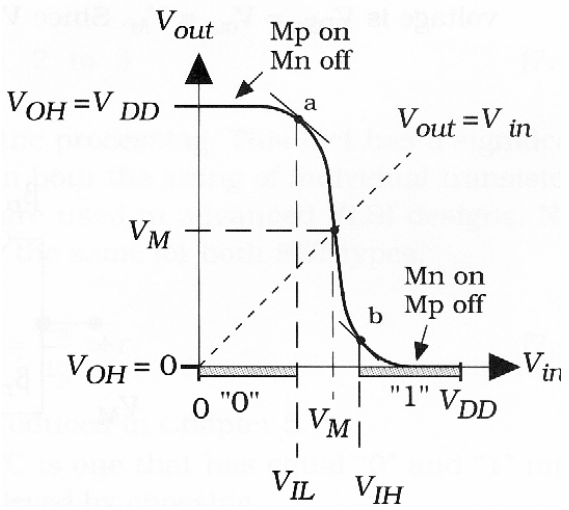
- Higher cost
- Larger fabrication time (more mask steps)



Q 3: Write short notes on
i) Noise Margin
ii) Rise time
iii) Fall time

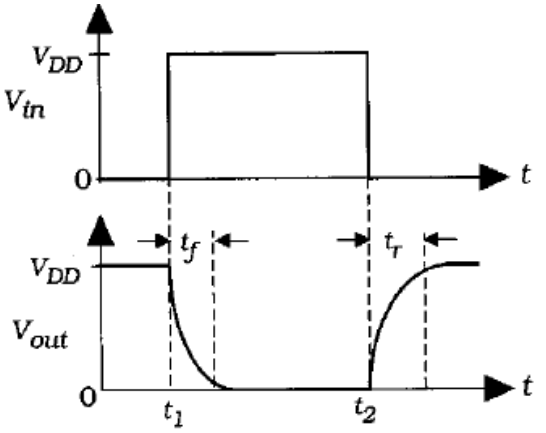
Answer:

i) Noise Margin - noise margin is the ratio by which the signal exceeds the minimum acceptable amount. It is normally measured in decibels.



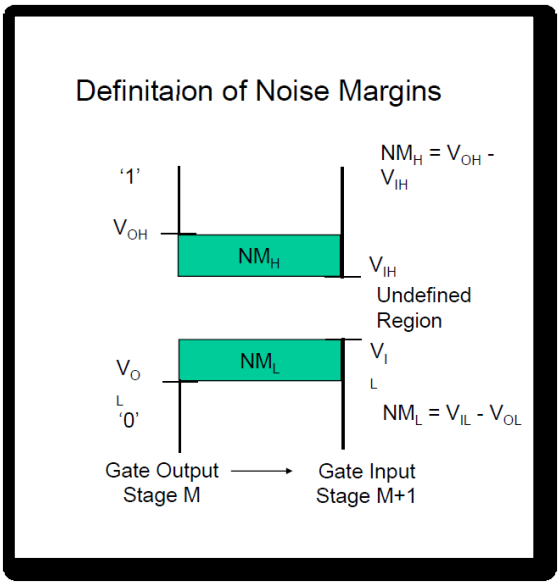
ii) Rise time - (tr) time for output to **rise** from '0'to '1'or it is the time to rise from 10% value to 90% value

iii) Fall Time- (tf) time for output to fall from '1'to '0' or it is the time to fall from 90% value to 10% value



Q 4: Explain DC Noise Margin of CMOS inverter ?

Answer:

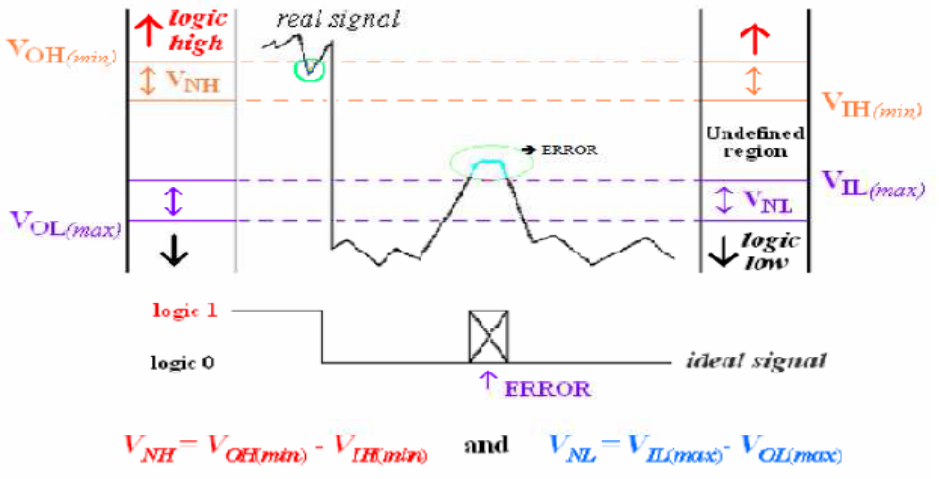


- **DC Noise Margins (NM)**

HIGH State Noise Margin : $(NM_H) = (V_{OH} - V_{IH}) = (V_{OHmin} - V_{IHmin})$

LOW State Noise Margin : $(NM_L) = (V_{IL} - V_{OL}) = (V_{ILmax} - V_{OLmax})$

Noise Margin (≈ *expressed in volt*): Noise margin is a measure of the extent to which a logic circuit can tolerate noise or unwanted signals.



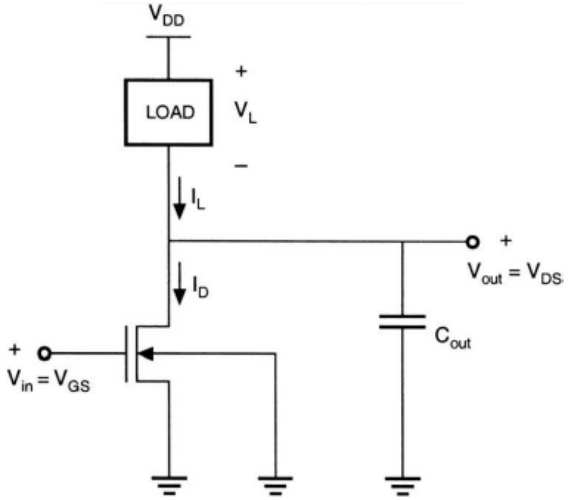
Q 5: Explain in brief Static load inverter ?

Answer:
-Static load inverter

- this circuit consists of an enhancement-type, N-Channel MOSFET as the *driver*
- a load resistor is connected between V_{DD} and the Drain (Vout) of the MOSFET
- the gates that this inverter drives are assumed to be of the same configuration so there is no DC load current looking into their gate terminals.

- $V_{out} = V_{DS}$

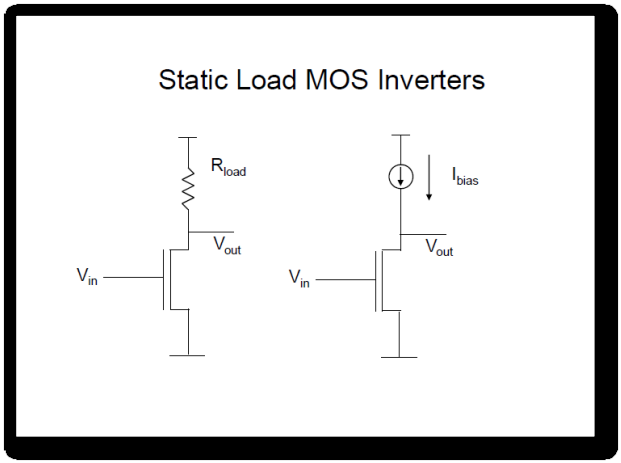
- $V_{in} = V_{gs}$



- we solve for $V_{out}(V_{in})$ using KVL where:

$$V_{out} = V_{DD} - R_L \cdot I_R$$

$$I_R = I_{DS} = \frac{V_{DD} - V_{out}}{R_L}$$



Resistor and Current-Source Loads

Resistance/length of minimum-width lines of various connecting elements is far less than effective resistance of the switched on MOSFET

• In some memory processes, resistors are implemented by highly resistive undoped polysilicon

• Normally use transistors in CMOS to implement resistor and current-source loads

• If biased for use as a resistor, called an unsaturated load inverter

• If load transistor operates in saturation as a constant

current source, called a saturated load inverter

VOL = output low voltage.

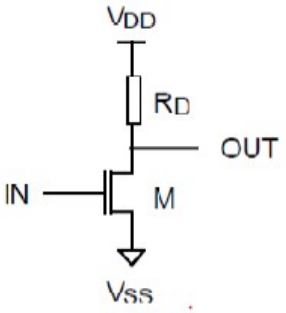


Figure 1. Resistively loaded inverter.

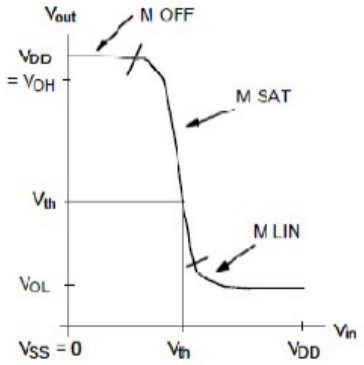


Figure 2. The transfer characteristic.

By analysing the circuit we observe:

- $V_{OUT} - V_{DS}$, $V_{IN} - V_{GS}$
- For $V_{IN} < V_t$, M is OFF, therefore $I_{DS} = 0$ and $V_{OUT} = V_{OH}$
- For $0 < (V_{IN} - V_t) < V_{OUT}$ M is in saturation region and $V_{OUT} = V_{DD} - I_{DS}R_D$
- For $0 < I < (V_{IN} - V_t)$ M is in the linear region and $V_{OUT} = V_{DD} - I_{DS}R_D$
- The gate threshold voltage occurs at $V_{IN} - V_{OUT}$

An unfortunate aspect of the resistively loaded inverter is that for $V_{IN} - V_{DD}$, $V_{OUT} - V_{OL} \neq 0$. As a result there is a static current that flows from supply to ground. This gives rise to an unwanted instantaneous power dissipation in the circuit when $V_{OUT} - V_{OL}$ of

$P = I_{DS}V_{OL} + (V_{DD}-V_{OL})^2/R_D = I_{DS}V_{DD}$

Summary:

The inverter is truly the nucleus of all digital designs. Once its operation and properties are clearly understood, designing more intricate structures such as NAND gates, adders, multipliers, and microprocessors is greatly simplified. The electrical behavior of these complex circuits can be almost completely derived by extrapolating the results obtained for inverters. The analysis of inverters can be extended to explain the behavior of more complex gates such as NAND, NOR, or XOR, which in turn form the building blocks for modules such as multipliers and processors. In this chapter, we focus on one single incarnation of the inverter gate, being the static CMOS inverter — or the CMOS inverter, in short. This is certainly the most popular at present and therefore deserves our special attention.

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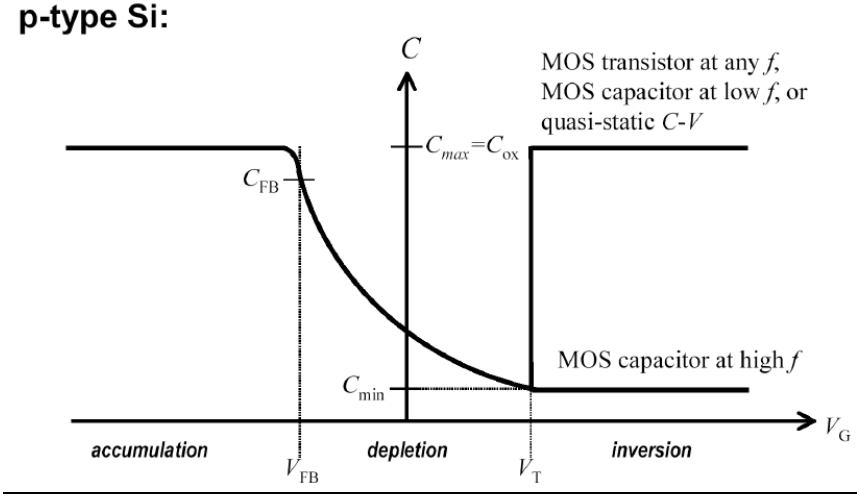
UNIT No 5: Analysis of CMOS Logic Gates

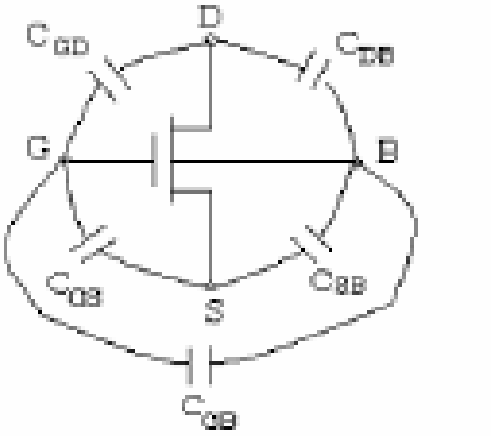
Q 1: Explain the MOS capacitor characteristics in Accumulation,depletion and inversion region.

A. Answer: MOS Device Capacitance



B.

C. *Figure: C-V Characteristics*



D. *The acronym MOS stands for metal–oxide–semiconductor. An MOS capacitor is made of a semiconductor body or substrate, an insulator film, such as SiO2, and a metal electrode called a gate. The oxide film can be as thin as 1.5 nm. One nanometer is equal to 10 Å, or the size of a few oxide molecules.*

Before 1970, the gate was typically made of metals such as Al (hence the M in MOS). After 1970, heavily doped polycrystalline silicon (see the sidebar, Three Kinds of Solid, has been the standard gate material because of its ability to withstand high temperature without reacting with SiO2. But the MOS name stuck. Unless specified otherwise, you may assume that the gate is made of heavily doped, highly conductive, polycrystalline silicon, or poly-Si for short. After 2008, the trend is to reintroduce metal gate and replace SiO2 with more advanced dielectrics for the most advanced transistors

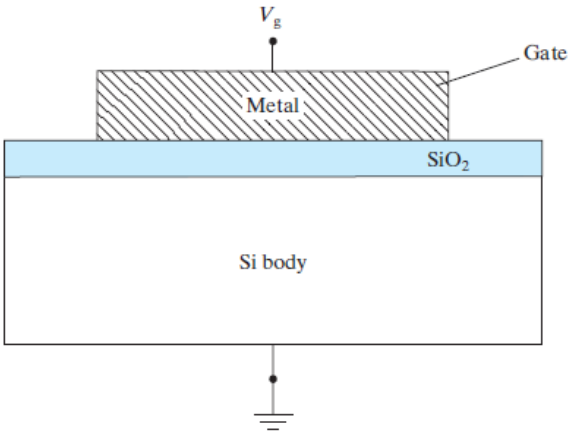
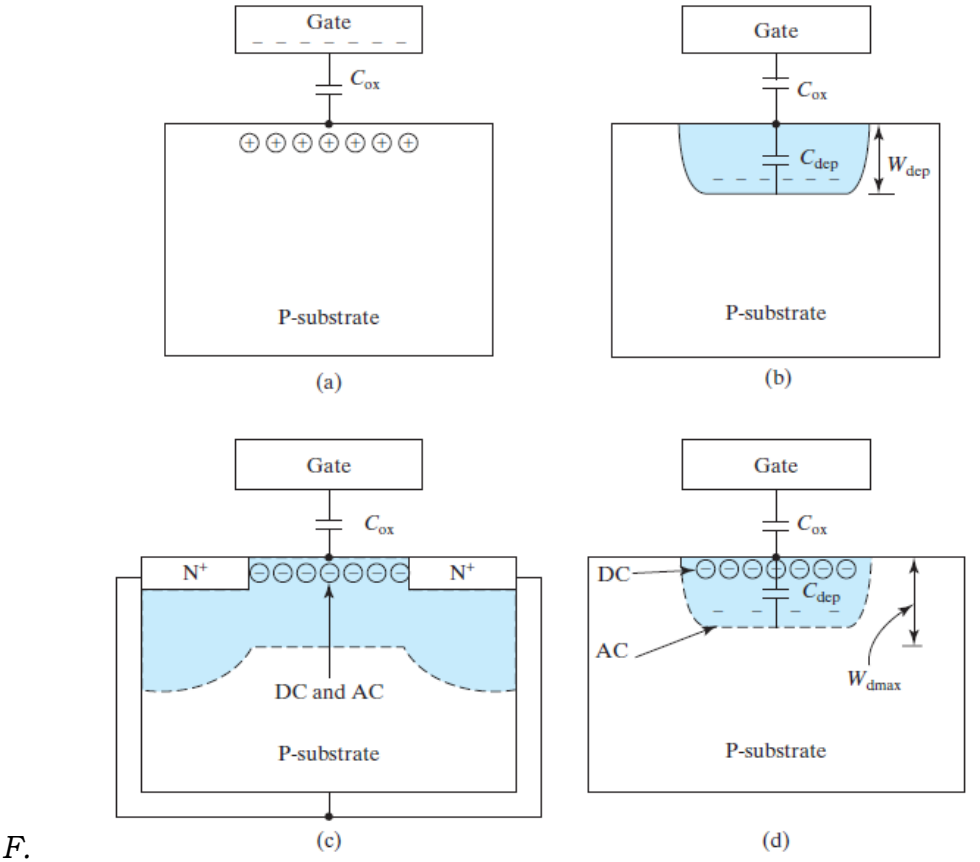


FIGURE 5.1: The MOS capacitor

E.



F.

G. *FIGURE 5.2: Illustration of the MOS capacitor in all bias regions with the depletion layers shaded. (a) Accumulation region; (b) depletion region; (c) inversion region with efficient supply of inversion electrons from the N region corresponding to the transistor C–V or the quasi-static C–V; and (d) inversion region with no supply of inversion electrons (or weak supply by thermal generation) corresponding to the high-frequency capacitor C–V case.*

H. *The most important property of the MOS capacitor is that its capacitance changes with an applied DC voltage. As a result, the modes of operation of the MOS capacitor change as a function of the applied voltage.*

Accumulation Region

With no voltage applied, a p-type semiconductor has holes, or majority carriers, in the valence band. When a negative voltage is applied between the metal gate and the semiconductor, more holes will appear in the valence band at the oxide-semiconductor interface. This is because the negative charge of the metal causes an equal net positive charge to accumulate at the interface between the semiconductor and the oxide. This state of the p-type semiconductor is called accumulation.

For a p-type MOS capacitor, the oxide capacitance is measured in the strong accumulation region. This is where the voltage is negative enough that the capacitance is essentially constant and the C-V curve is almost flat. This is where the oxide thickness can also be extracted from the oxide capacitance. However, for a very thin oxide, the slope of the C-V curve doesn't flatten in accumulation and the measured oxide capacitance differs from the actual oxide capacitance.

Depletion Region

When a positive voltage is applied between the gate and the semiconductor, the majority carriers are replaced from the semiconductor-oxide interface. This state of the semiconductor is called depletion because the surface of the semiconductor is depleted of majority carriers. This area of the semiconductor acts as a dielectric because it can no longer contain or conduct charge. In effect, it becomes an insulator.

The total measured capacitance now becomes the oxide capacitance and the depletion layer capacitance in series, and as a result, the measured capacitance decreases. This decrease in capacitance is illustrated in ***Figure 3*** in the depletion region. As a gate voltage increases, the depletion region moves away from the gate, increasing the effective thickness of the dielectric between the gate and the substrate, thereby reducing the capacitance.

Inversion Region

As the gate voltage of a p-type MOS-C increases beyond the threshold voltage, dynamic carrier generation and recombination move toward net carrier generation. The positive gate voltage generates electron-hole pairs and attracts electrons (the minority carriers) toward the gate. Again, because the oxide is a good insulator, these minority carriers accumulate at the substrate-to-oxide/well-to-oxide interface. The accumulated minority-carrier layer is called the inversion layer because the carrier polarity is inverted. Above a certain positive gate voltage, most available minority carriers are in the inversion layer, and further gate-voltage increases do not further deplete the semiconductor. That is, the depletion region

reaches a maximum depth.

Once the depletion region reaches a maximum depth, the capacitance that is measured by the high frequency capacitance meter is the oxide capacitance in series with the maximum depletion capacitance. This capacitance is often referred to as minimum capacitance. The C-V curve slope is almost flat.

Q 2: Write a short note on NMOS/PMOS Ratio.

Answer:

So far, we have consistently widened the PMOS transistor so that its resistance matches that of the pull-down NMOS device. This typically requires a ratio of 3 to 3.5 between PMOS and NMOS width. The motivation behind this approach is to create an inverter with a symmetrical VTC, and to equate the high-to-low and low-to-high propagation delays. However, this does not imply that this ratio also yields the minimum overall propagation delay. If symmetry and reduced noise margins are not of prime concern, it is actually possible to speed up the inverter by reducing the width of the PMOS device!

The reasoning behind this statement is that, while widening the PMOS improves the *tpLH* of the inverter by increasing the charging current, it also degrades the *tpHL* by cause of a larger parasitic capacitance. When two contradictory effects are present, there must exist a transistor ratio that optimizes the propagation delay of the inverter.

Q 3: Explain Static Power Dissipation in CMOS Inverter.

Answer: Power Dissipation in a CMOS Inverter:

Total Power =Static Power + Dynamic Power + Short Circuit Power

$$P_t = P_{static} + P_{dynamic} + P_{short\ circuit}$$

1. Static Power Dissipation

The static (or steady-state) power dissipation of a circuit is expressed by following Equation, where I_{static} is the current that flows between the supply rails in the absence of switching activity

$$P_{static} = I_{static} * V_{DD}$$

Ideally, the static current of the CMOS inverter is equal to zero, as the PMOS and NMOS devices are never on simultaneously in steady-state operation. There is, unfortunately, a leakage current flowing through the reverse-biased diode junctions of the transistors, located between the source or drain and the substrate as shown in Figure 5.31. This contribution is, in general, very small and can be ignored. For the device sizes under consideration, the leakage current per unit drain area typically ranges between 10-100 pA/mm^2 at room temperature. For a die with 1 million gates, each with a drain area of 0.5 mm^2 and operated at a supply voltage of 2.5 V, the worst-case power consumption due to diode leakage equals 0.125 mW, which is clearly not much of an issue.

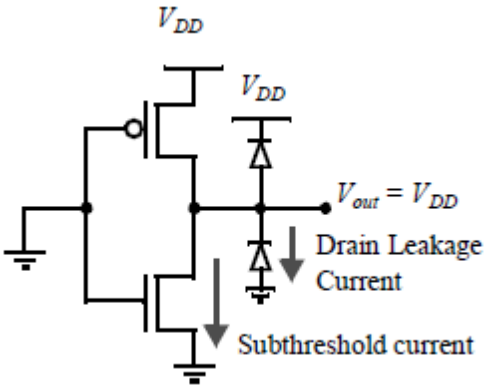


Figure 5.3: Sources of leakage currents in CMOS inverter (for *Vin* = 0 V).

However, be aware that the junction leakage currents are caused by thermally generated carriers. Their value increases with increasing junction temperature, and this occurs in an exponential fashion. At 85°C (a common junction temperature limit for commercial hardware), the leakage currents increase by a factor of 60 over their room-temperature values. Keeping the overall operation temperature of a circuit low is consequently a desirable goal. As the temperature is a strong function of the dissipated heat and its removal mechanisms, this can only be accomplished by limiting the power dissipation of the circuit and/or by using chip packages that support efficient heat removal. An emerging source of leakage current is the subthreshold current of the transistors. A MOS transistor can experience a drain-source current, even when *VGS* is smaller than the threshold voltage The closer the threshold voltage is to zero volts, the larger the leakage current at *VGS* = 0 V and the larger the static power consumption. To offset this effect, the threshold voltage of the device has generally been kept high enough. Standard processes feature *VT* values that are never smaller than
0.5-0.6V and that in some cases are even substantially higher (~ 0.75V).

Q 4: Explain Dynamic Power Dissipation.

Answer: Dynamic Power Dissipation

Each time the capacitor *CL* gets charged through the PMOS transistor, its voltage rises from 0 to *VDD,* and a certain amount of energy is drawn from the power supply. Part of this energy is dissipated in the PMOS device, while the remainder is stored on the load capacitor.

During the high-to-low transition, this capacitor is discharged, and the stored energy is dissipated in the NMOS transistor. A precise measure for this energy consumption can be derived. Let us first consider the low-to-high transition. We assume, initially, that the input

waveform has zero rise and fall times, or, in other words, that the NMOS and PMOS devices are never on simultaneously. Therefore, the equivalent circuit of Figure 5.23 is valid. The values of the energy *EVDD*, taken from the supply during the transition, as well as the energy *EC*, stored on the capacitor at the end of the transition, can be derived by integrating the instantaneous power over the period of interest.

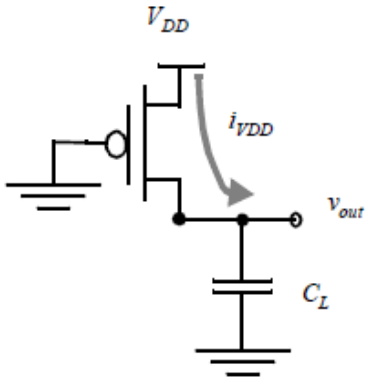


Figure 5.4: Equivalent circuit during the low-to-high transition.

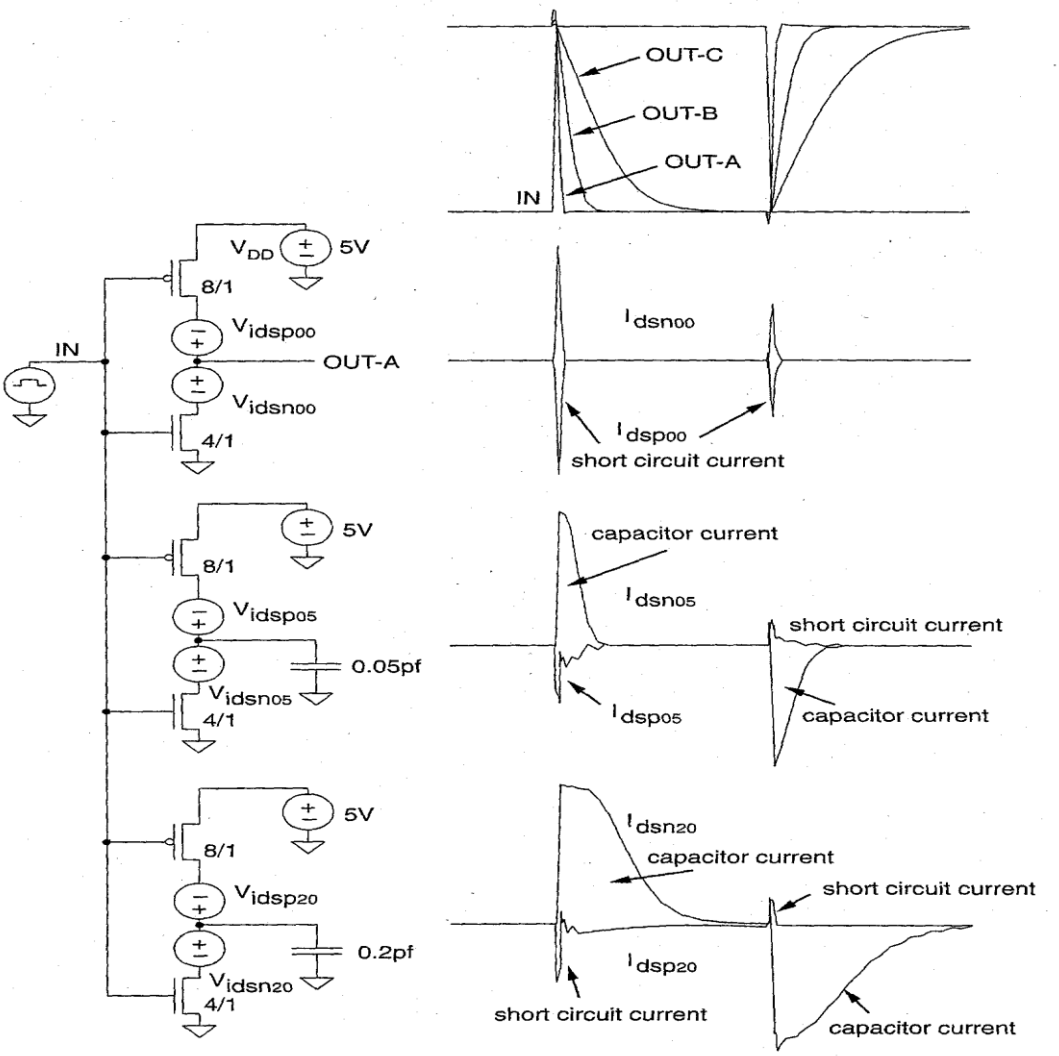


Figure 5.5: Effect of Capacitive Load on CMOS Inverter (Switching activity)

- Average dynamic power derivation:

- On negative going input, pull-up device charges the load capacitance. On positive going input, pull-down device discharges the load into ground.
- Average power given by

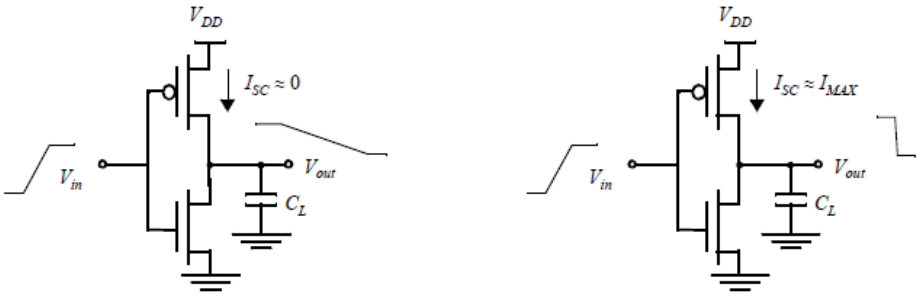
$P_{ave} = (1/T)fC_L\,(dv_{out}/dt)\,(V_{dd} - v_{out})dt + (1/T)f(-1)\,C_L\,(dv_{out}/dt)\,v_{out}\,dt$

where the first integral is taken from 0 to T/2 and the second integral is from T/2 to T

- completion of the integral yields $P_{ave} = C_L V_{dd}^2 f$ where $f = 1/T$
- Note that the dynamic power is independent of the typical device parameters, but is simply a function of power supply, load capacitance and frequency of the switching!

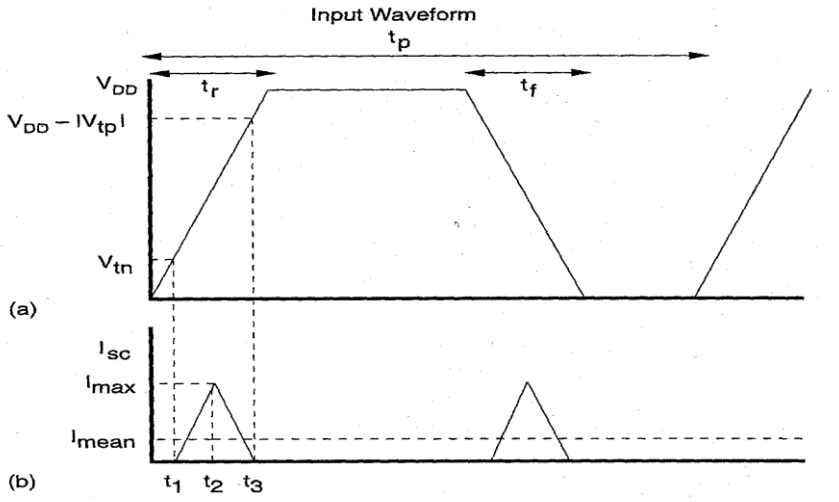
Q 5: Explain Short Circuit Power Dissipation.

Answer: CMOS Short-Circuit Power Dissipation



(a) Large capacitive load (b) Small capacitive load

Figure 5.6**:** Impact of load capacitance on short-circuit current.



- The total power in a CMOS circuit is given by
- $\mathbf{P_{total} = P_d + P_{sc} + P_s}$ where Pd is the dynamic average power (previous chart), Psc is the short circuit power, and Ps is the static power due to ratio circuit current, junction leakage, and subthreshold I_{off} leakage current.
- Short circuit current flows during the brief transient when the pull down and pull up devices both conduct at the same time where one (or both) of the devices are in saturation.
- For a balanced CMOS inverter with βn=βp, and Vtn = |Vtp|, the short circuit power can be expressed by

$$\mathbf{P_{sc} = (\beta/12)(V_{dd} - 2V_t)^3 (t_{rf}/t_p)}$$

where t_p is the period of the input waveform and t_{rf} is the total rise time (or fall time) $tr = t_f = t_{rf}$

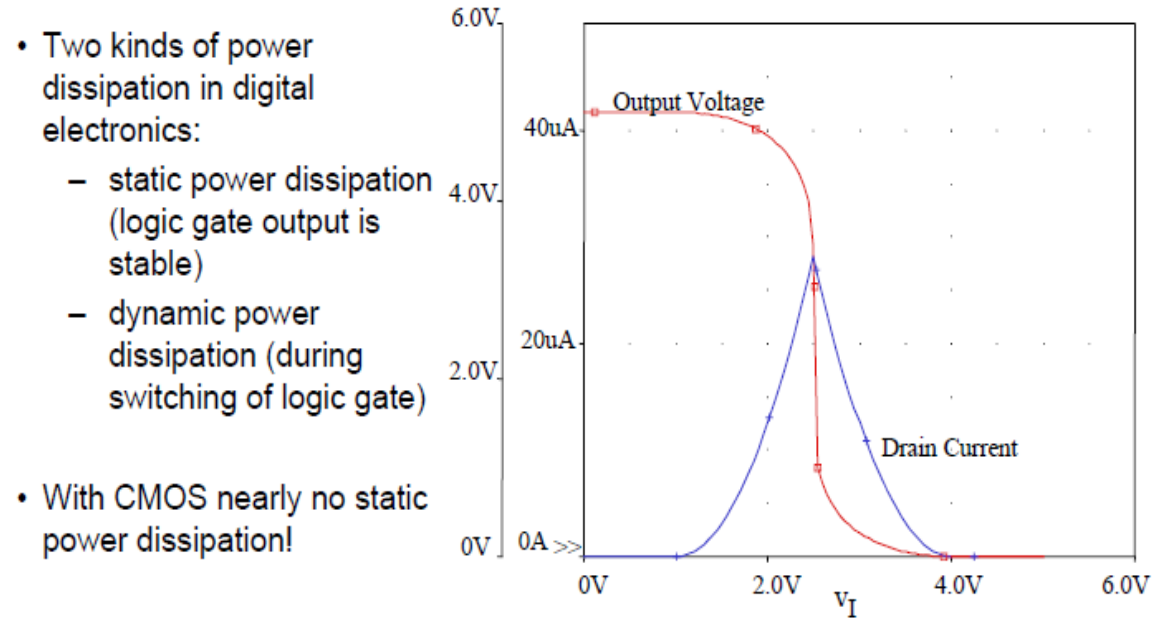


Figure 5.7: Current and voltage waveforms of CMOS Inverter

Question 6: Explain the concept of charge sharing.

Answer: Charge Sharing:

- At time t=0-, switch is open and each capacitor contains some initial charge
- At time t=0+, the switch is closed and the charge redistributes across both capacitors
- Conserve the total charge:
  - Sum up initial charge Qt = Qb + Qs = CbVb + CsVs
  - Final charge is given by Qt = (Cb + Cs)Vf
  - Therefore, **Vf = (CbVb + CsVs)/(Cb + Cs)**

- If Vb = Vdd and Vs = 0, then

  Vf = Vdd Cb/(Cb + Cs) (which is similar to the equation for a resistor divider)

- Charge sharing plays an important role in many dynamic circuits, especially pulsed DOMINO and NOR logic as well as in DRAM operation.

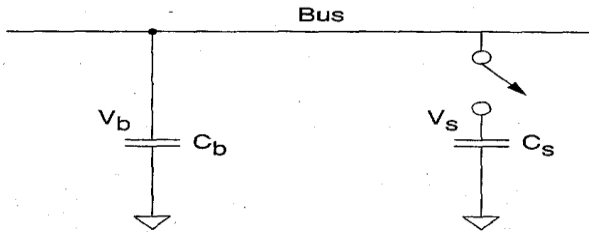


Figure 5.8: Charge sharing

Question 7: What is the concept of Ratioed Logic?

Answer: **Ratioed Logic:**

One method to reduce the circuit complexity of static CMOS. Here, the logic function is built in the PDN and used in combination with a simple load device.

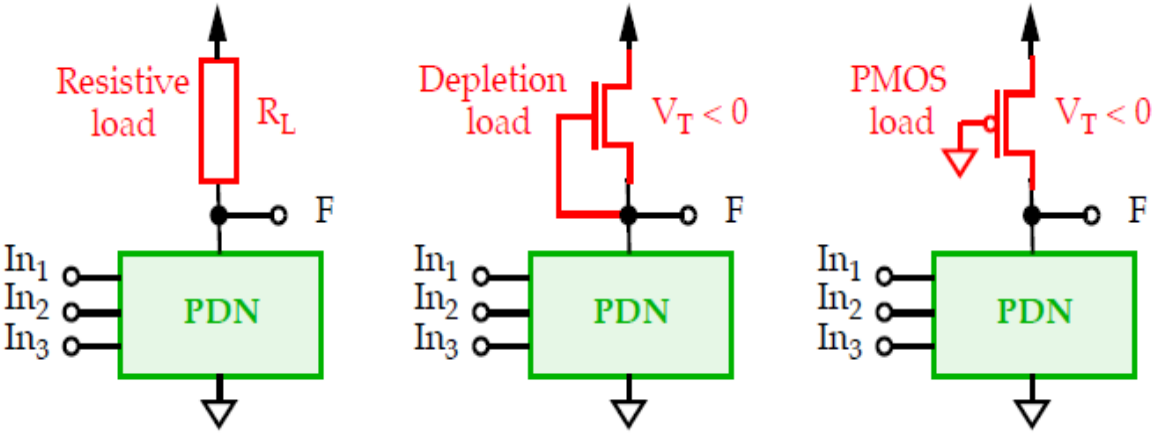


Figure: Ratioed Logic

Goal of Ratioed Logic: to reduce the number of devices over complementary CMOS

Figure 5.9:Ratioed Logic

Let's assume the load can be represented as **linearized resistors**.

When the PDN is on, the output voltage is determined by:

$$V_{OL} = \frac{R_{PDN}}{R_L + R_{PDN}} V_{DD}$$

This logic style is called **ratioed** because care must be taken in scaling the impedances properly. Note that full complementary CMOS is **ratioless**, since the output signals do not depend on the size of the transistors.

In order to keep the noise margins high, RL >> RPDN. However, RL must be able to provide as much current as possible to minimize delay.

$$t_{pLH} = 0.69 R_L C_L$$

$$t_{pHL} = 0.69 (R_L /\!/ R_{PDN}) C_L$$

These are **conflicting** requirements:

R_L large: Noise margins.

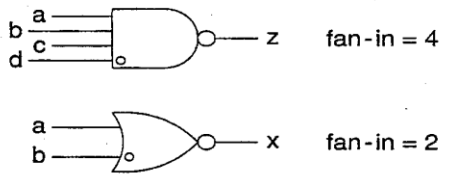
R_L small: performance and power dissipation

This has resulted in a wide variety of possible load configurations.

Question 8: Write a short note on Fan in and Fan out.

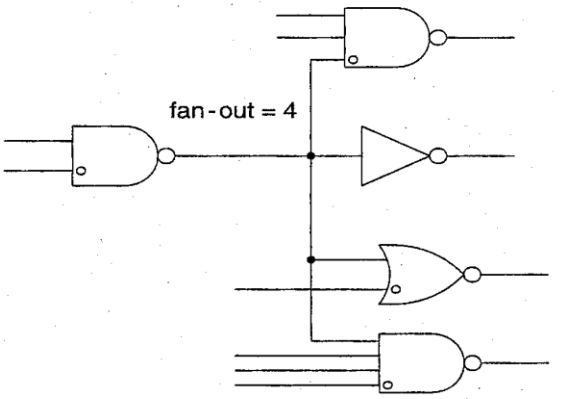
Answer: Fan-In and Fan-Out :

- Fan-In = number of inputs to a logic gate
  - 4 input NAND has a FI = 4
  - 2 input NOR has a FI = 2, etc. (See Fig. a below.)
- Fan-Out = number of gate inputs which are driven by a particular gate output
  - FO = 4 in Fig. b below shows an output wire feeding an input on four different logic gates
- The circuit delay of a gate is a function of both the Fan-In and the Fan-Out.



(a)

Note: The open circle adjacent to a logic gate input denotes the series transistor closest to the output.



(b)

Figure 5.10 :Fan in and fan out examples

Q 9: Write a short note on Classification of logic circuits.

Answer: Sequential circuit: Latches and Flip Flops:

The sequential logic circuits contain one or more combinational logic blocks along with memory in a feedback loop with the logic: The next state of the machine depends on the present state and the inputs. The output depends on the present state of the machine and perhaps also on the inputs

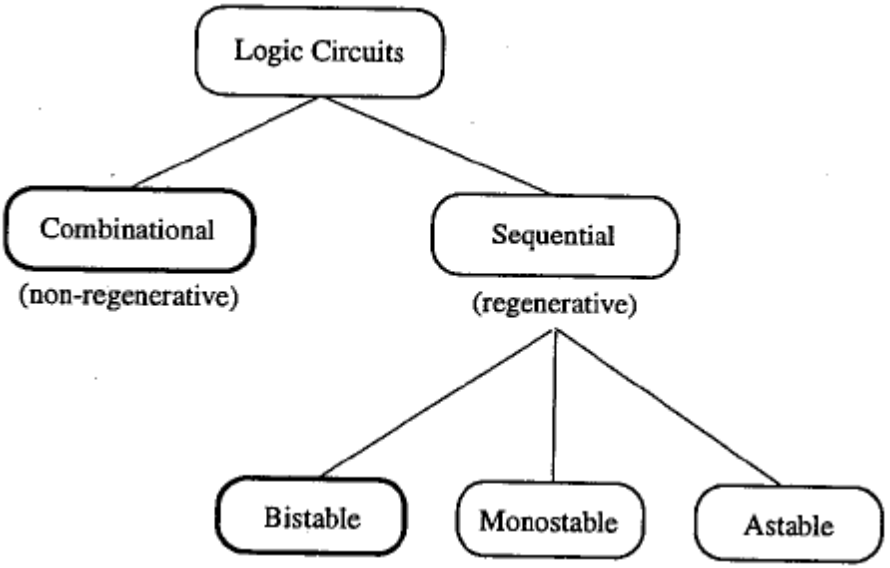


Figure 5.11**:** Classification of logic circuits.

Sequential Circuit Types

• Bistable circuits have two stable operating points and will remain in either state unless perturbed to the opposite state

– Memory cells, latches, flip-flops, and registers

• Mono-stable circuits have only one stable operating point, and even if they are temporarily perturbed to the opposite state, they will return in time to their stable operating point

• Astable circuits have no stable operating point and oscillate between several states

– Ring oscillator

Q 10.Explain CMOS Positive –level-sensitive D Latch.

Answer: CMOS Positive –level-sensitive D Latch:

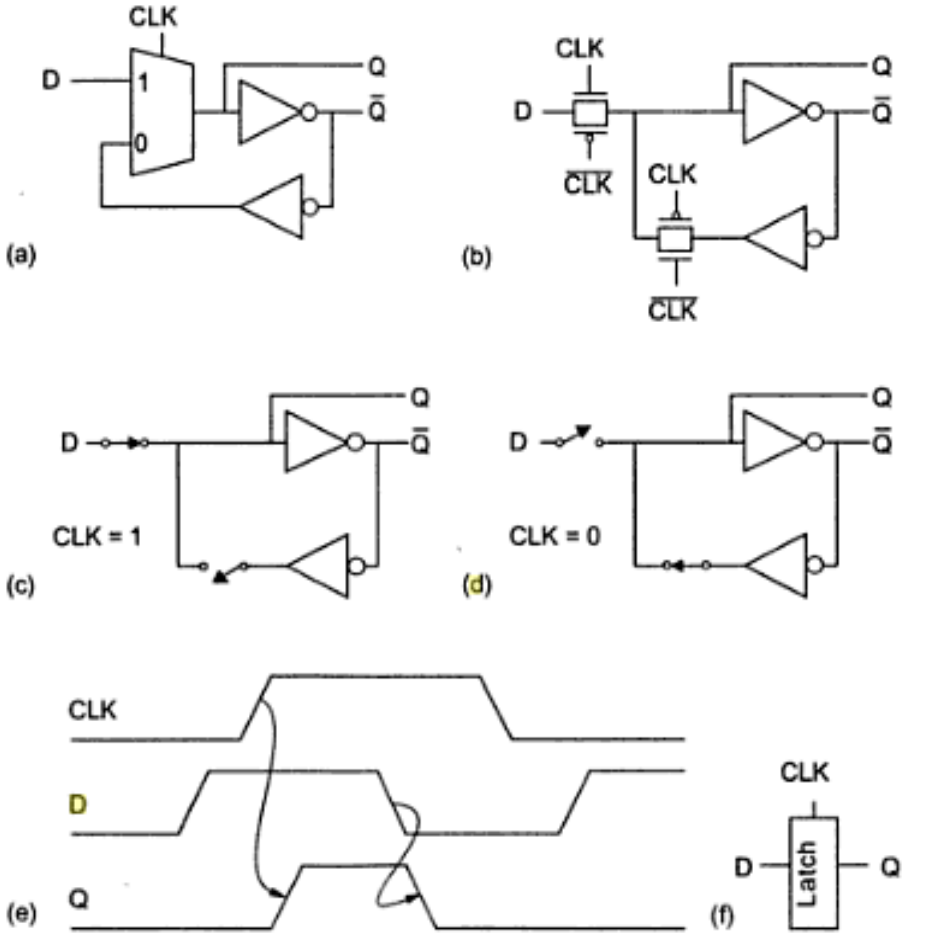


FIG 1.30 CMOS positive-level-sensitive D latch

Q 11.Explain CMOS Positive –level-sensitive D Flip flop.

Answer: **CMOS Positive –edge-triggered D Flip Flop:**

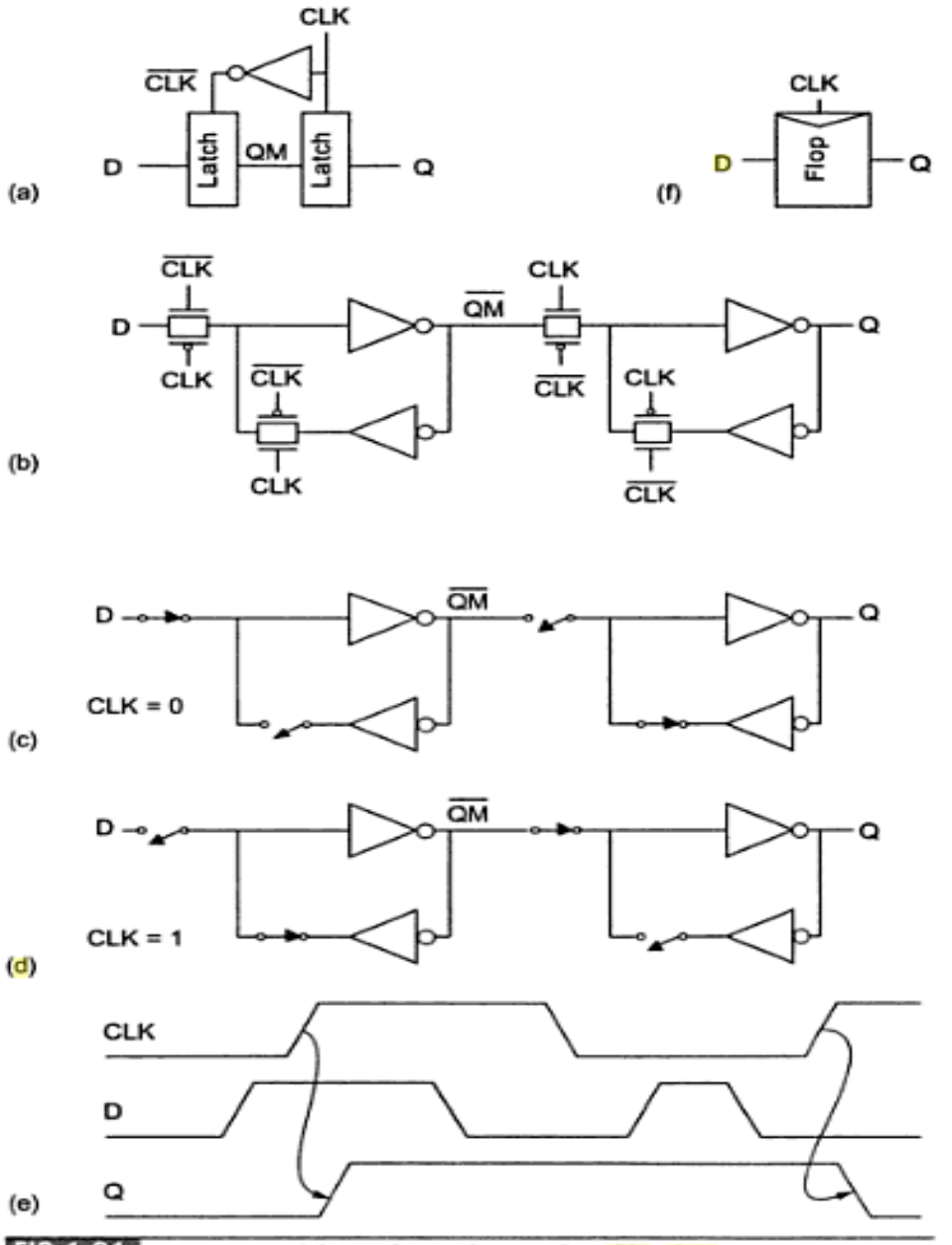


FIG 1.31 CMOS positive-edge-triggered D flip-flop

Summary:

Power dissipation in CMOS devices is composed of both a static and a dynamic component. Anyway, the dominant part is the dynamic part, expressed by the switching activity power $P = \mathrm{VDD}^2 f_{\mathrm{CLK}} C_{\mathrm{EFF}}$ where V_{DD} is the supply voltage, f_{CLK} is the system clock frequency and C_{EFF} is the effective switched capacitance (that is the product of the total physical capacitance C_{Li} of each node in the circuit and the switching activity factor α_i of each node summed over all the N nodes in the circuit).

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UNIT No 6: Complex Logic Structures

Question 1: Explain advantages and disadvantages of Complementary CMOS Logic.

Answer: Complementary CMOS Logic:

Full complementary static CMOS gates may be undesirable

because:

- The area overhead.
- Their speed may be too slow.
- The function may not be feasible as a full complementary structure

Smaller faster gates can be implemented at the cost of:

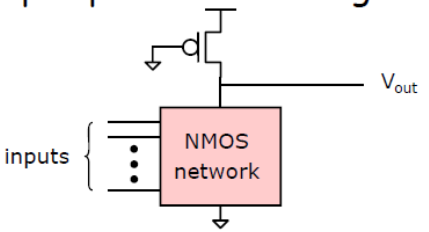
- Increased design time.
- Increased operational complexity.
- Decreased operational margin

Question 2: Explain the concept of Pseudo NMOS Logic with suitable example.

Answer: Pseudo NMOS Logic:

Pseudo-NMOS Logic

- An N-input pseudo-NMOS gate



- Features of pseudo-NMOS logic
  - Advantages
    - Low area cost→only N+1 transistors are needed for an N-input gate
    - Low input gate-load capacitance→C_{gn}
  - Disadvantage
    - Non-zero static power dissipation

The inverter that uses a p-device pull-up or load that has its gate permanently ground. An n-device pull-down or driver is driven with the input signal. This roughly equivalent to use of a depletion load is **Nmos** technology and is thus called '**Pseudo-NMOS**'. The circuit is used in a variety of CMOS logic circuits.

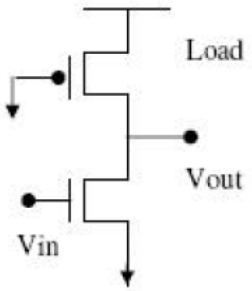


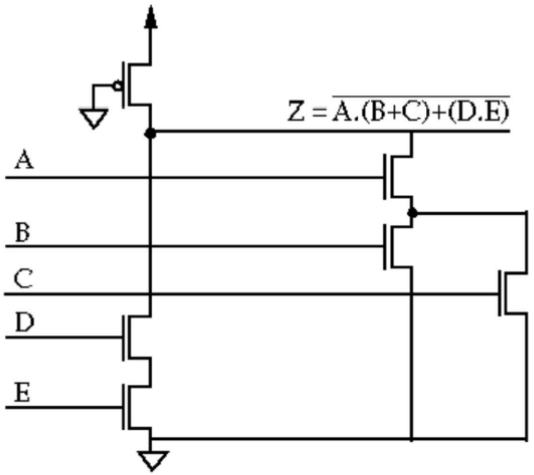
Fig. Generic Structure

The CMOS pull up network is replaced by a single pMOS transistor with

its gate grounded. Since the pMOS is not driven by signals, it is always ‘on'. The effective gate voltage seen by the pMOS transistor is Vdd . Thus the overvoltage on the p channel gate is always Vdd -VTp. When the nMOS is turned ‘on', a direct path between supply and ground exists and static power will be drawn. However, the dynamic power is reduced due to lower capacitive loading.

Static CMOS gates are slowed because an input must drive both NMOS and PMOS transistors. In any transition, either the pull-up or pull-down network is activated; meaning the input capacitance of the inactive network loads the input. Moreover, PMOS transistors have poor mobility and must be sized larger to achieve comparable rising and falling delays, further increasing input capacitance. Pseudo-NMOS and dynamic gates offer improved speed by removing the PMOS transistors from loading the input. This section analyzes pseudo-NMOS gates

Example:



Advantages:
Capacitive load on inputs is only one gate unit.
Density advantage over full complementary CMOS.

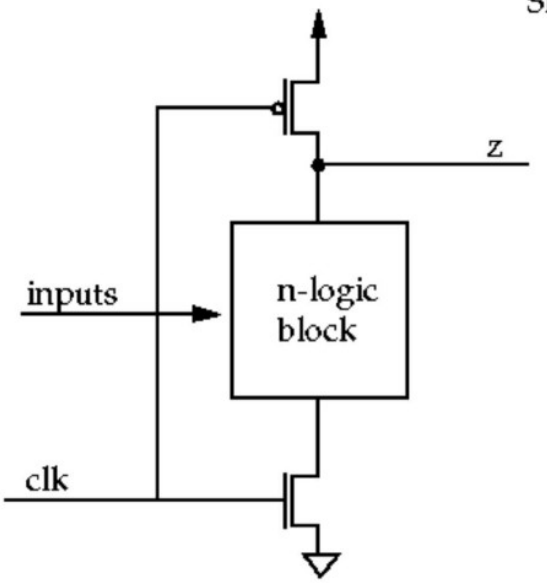
Main problem:
Static power dissipation

Gain of the pull-up has to be decreased to provide adequate noise margins (when minimum sized transistors are used).
→ Slows rise time.

- *Gain ratio of n-driver transistors to p-transistor load (beta* driver */beta* load *), is important to ensure correct operation.*
- *Accomplished by ratioing the n and p transistor sizes.*

Question 3: Explain the concept of Dynamic CMOS Logic and explain it with suitable example.

Answer: Dynamic CMOS Logic:



Simple single phase dynamic CMOS:

Precharge phase: Clk = 0

Evaluate phase: Clk = 1

Input capacitance: Same as that of pseudo-nMOS.

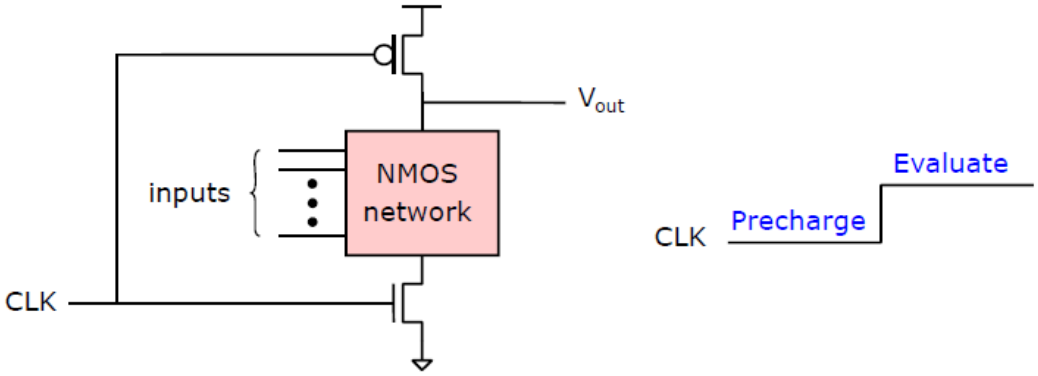
Problem:

Inputs can only change during the precharge phase.

If they change during evaluate, charge redistribution can corrupt output voltage.

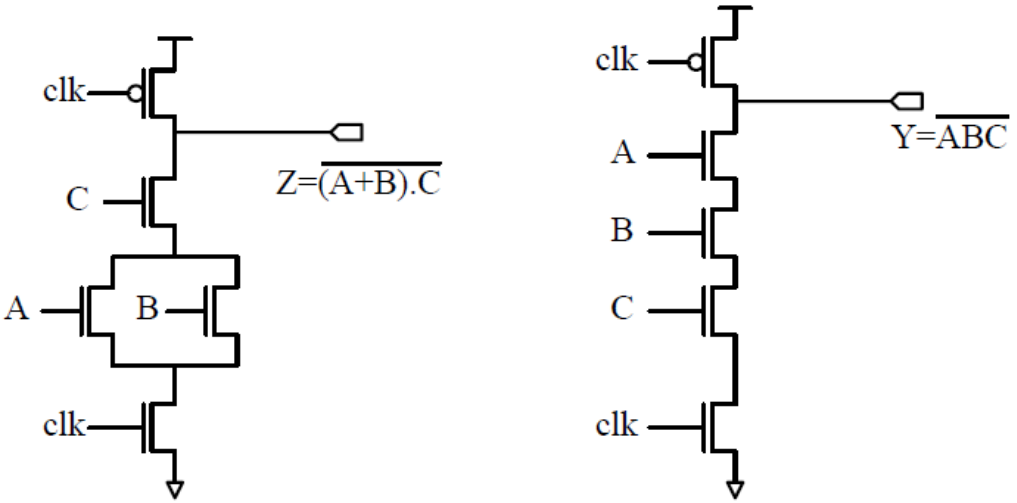
Dynamic Logic

- Another dynamic logic technique



- Two-phase operation: precharge & evaluate
- This can fully eliminate static power dissipation

Examples:

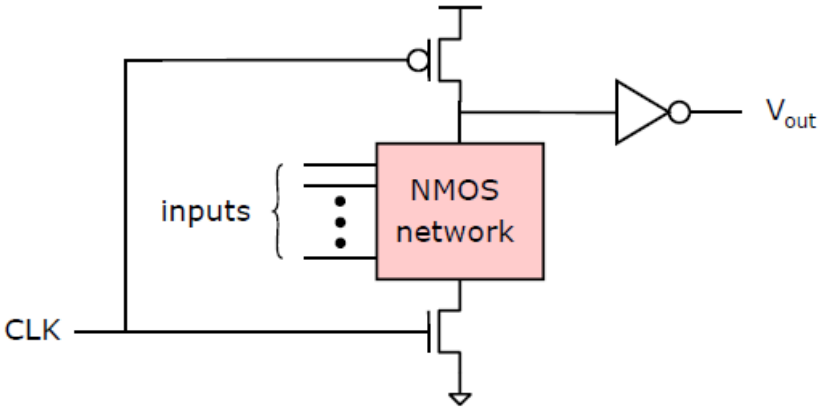


Question 4: Explain the concept of Domino CMOS Logic and explain it with suitable example.

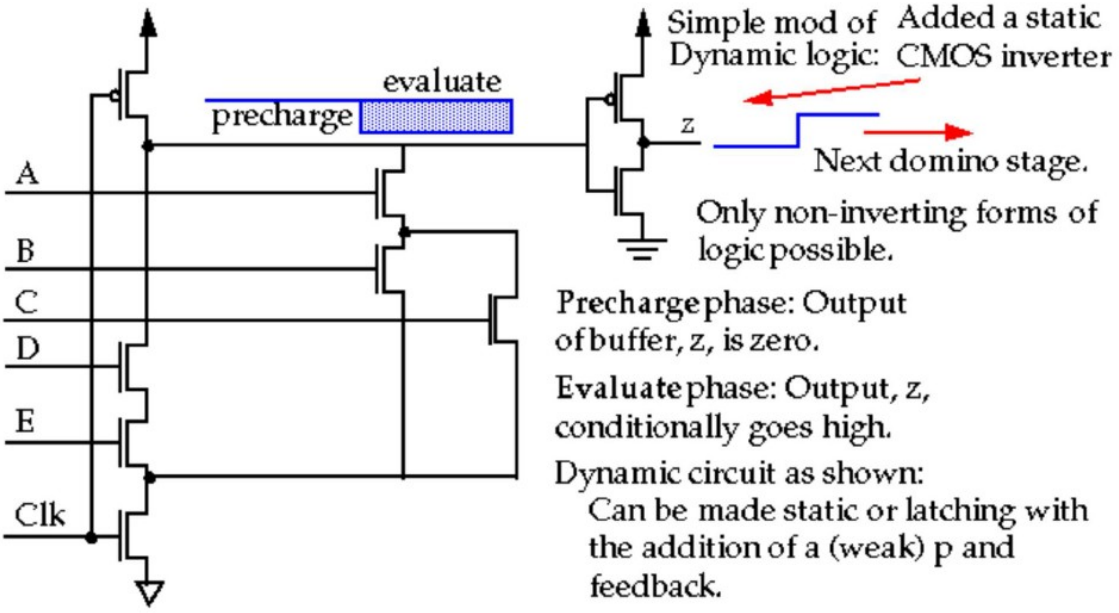
Answer: Domino CMOS Logic:

CMOS Domino Logic

- Domino logic can be cascaded
- The basic structure of domino logic



Example:

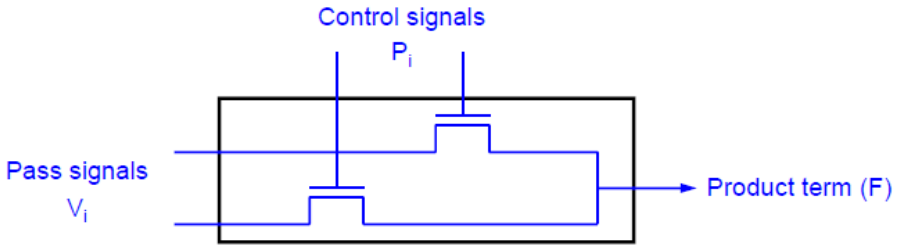


Question 5: Explain the concept of Pass Transistor Logic and explain it with suitable example.

Answer: Pass Transistor Logic

Pass-Transistor Logic

- Model for pass transistor logic

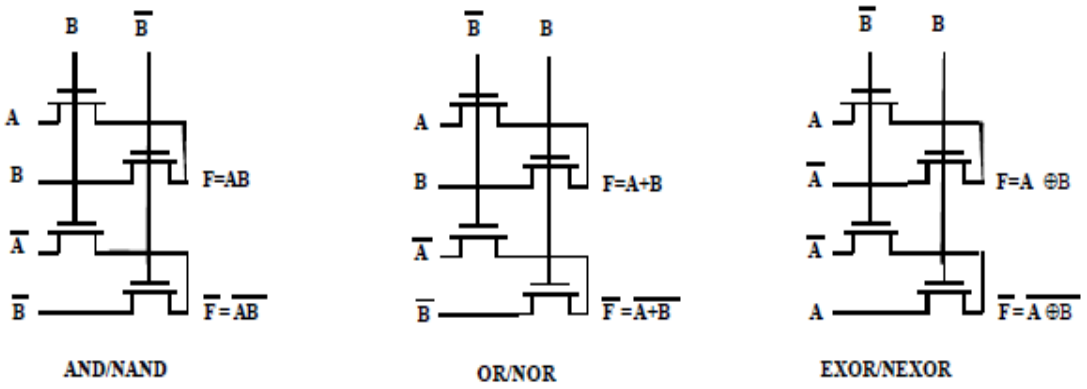


- The product term
  - $F=P_1V_1+P_2V_2+...+P_nV_n$
  - The pass variables can take the values $\{0,1,X_i,-X_i,Z\}$, where X_i and $-X_i$ are the true and complement of the ith input variable and Z is the high-impedance

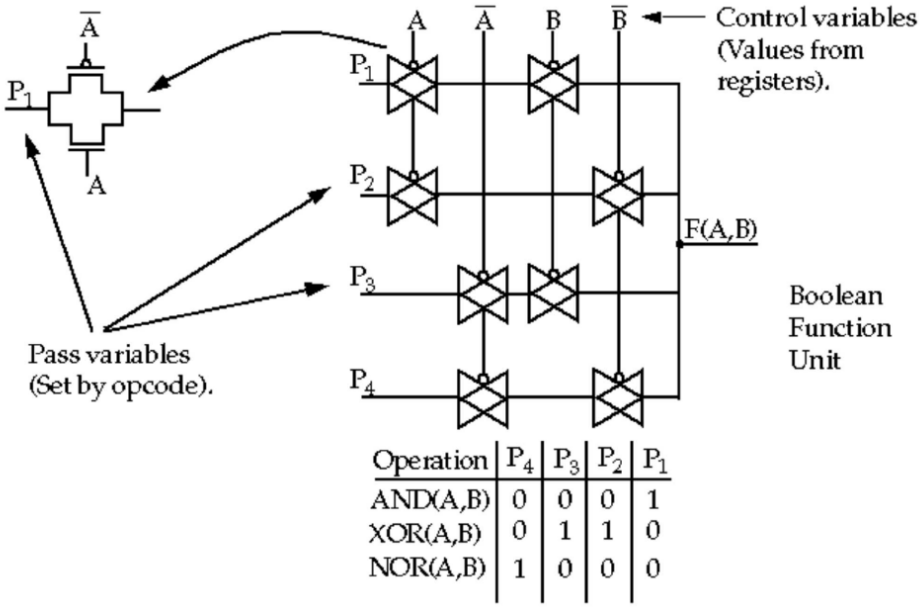
Since circuit is differential, complimentary inputs and outputs are available. Although generating differential signals require extra circuitry, complex gates such as XORs, MUXs and adders can be realized efficiently.

•CPL is a static gate, because outputs are connected to Vdd or GND through a low-resistance path (high noise resilience).

•Design is modular –all gates use same topology; only inputs are permuted. This facilitates the design of a library of gates.



Examples:



Operation	P_4	P_3	P_2	P_1
AND(A,B)	0	0	0	1
XOR(A,B)	0	1	1	0
NOR(A,B)	1	0	0	0

Question 6:

Answer: Implement 4:1 Multiplexer using Pseudo NMOS Logic

Answer:

Pseudo-NMOS Logic Circuits

- Despite many advantages, CMOS suffers from the increased area, and correspondingly increased capacitance and delay as the logic gates becomes more complex. Solution to this is use of Pseudo-NMOS Logic
- For pseudo-NMOS logic a p-device pull-up or load has its gate permanently grounded. An n-device pull-down or driver is driven with the input signal. This roughly equivalent to use of a depletion load is NMOS technology and is thus called 'Pseudo-NMOS'. The circuit is used in a variety of CMOS logic circuits.

Working:

- As shown in figure NMOS network connected in series behaves as AND Gate.
- AND gate has a property that if one of its input is high the other input will be the output of AND Gate. The working of above circuit is based on this principle.

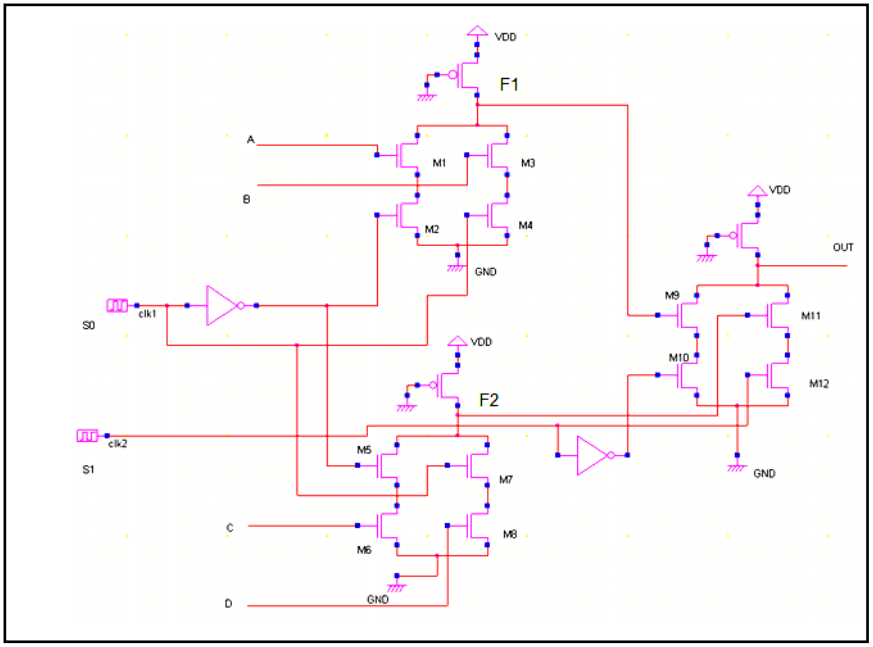


Fig: 6:1 Multiplexer using pseudo-NMOS logic.

Case1: When S1S0 = 00

- MOSFET M2 and M5 gets activated due to S0 = 0; and output F1 = A and F2 = C is selected.

- F1 and F2 are fed to MOSFET M9 and M11 respectively; but due to S1 = 0 MOSFET M10 is activated and output F1 = A is selected.

Case2: When S1S0 = 01

- MOSFET M4 and M7 gets activated due to S0 = 1; and output F1 = B and F2 = D is selected.
- F1 and F2 are fed to MOSFET M9 and M11 respectively; but due to S1 = 0 MOSFET M10 is activated and output F1 = B is selected.

Case3: When S1S0 = 10

- MOSFET M2 and M5 gets activated due to S0 = 1; and output F1 = A and F2 = C is selected.
- F1 and F2 are fed to MOSFET M9 and M11 respectively; but due to S1 = 1 MOSFET M12 is activated and output F2 = C is selected.

Case4: When S1S0 = 11

- MOSFET M4 and M7 gets activated due to S0 = 1; and output F1 = B and F2 = D is selected.
- F1 and F2 are fed to MOSFET M9 and M11 respectively; but due to S1 = 1 MOSFET M12 is activated and output F2 = D is selected.

Applications:

1. Multiplexers are used to send data from one location to another location.
2. Many tasks in communication control systems and computer systems can be performed by combinational logic circuits.
3. Multiplexer are used to design any digital combinational logic circuit.
4. Multiplexers are used in many applications such as: Cross bar switching, Logic function generator, Look up tables, Adders

Question 7: Implement 4:1 Multiplexer using Dynamic CMOS Logic.

Answer:

- Ratioed circuits reduce input capacitance by replacing PMOS transistor connected to the inputs with single resistive pull up.
- The drawbacks of ratioed circuits include slow rising transitions, contention on falling transitions, static power dissipation and a non-zero V_{OL}
- Dynamic circuits overcome these drawbacks by using a clocked pull-up transistor rather than PMOS that is always ON.
- Dynamic circuit operation is divided into two modes Precharge and Evaluation
- During precharge clock ϕ is '0' so the clocked PMOS is ON as a result output is high.
- During evaluation the clock is '1' and the clocked PMOS turns OFF. The output may remain high or may be discharged low through the pull-down network.

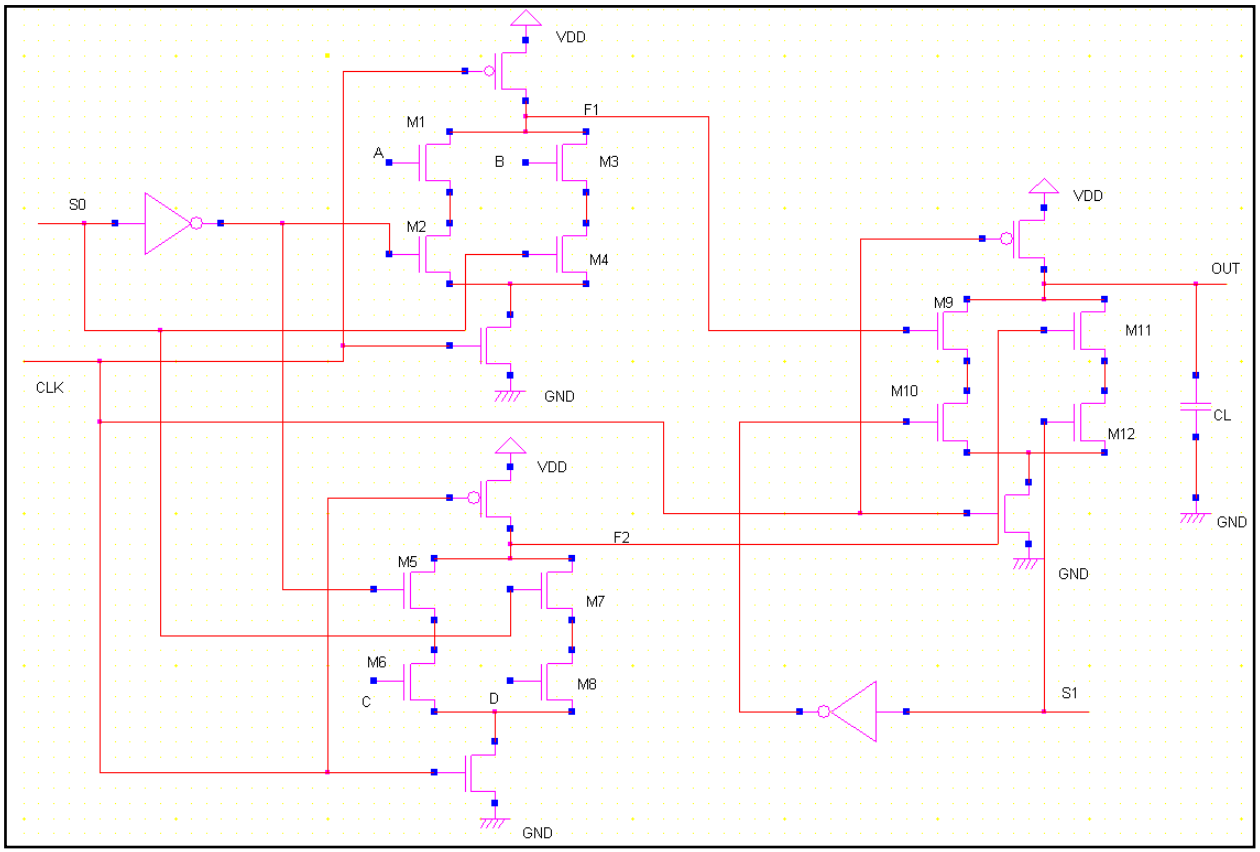


Fig: 4:1 MUX using Dynamic Logic

Working:

- As shown in figure NMOS network connected in series behaves as AND Gate.
- AND gate has a property that if one of its input is high the other input will be the output of AND Gate. The working of above circuit is based on this principle.
- When CLK = 0 PMOS is ON and output is high
- When CLK = 1 PMOS is OFF and the circuit works according to following cases.

Case1: When S1S0 = 00

- MOSFET M2 and M5 gets activated due to S0 = 0; and output F1 = A and F2 = C is selected.
- F1 and F2 are fed to MOSFET M9 and M11 respectively; but due to S1 = 0 MOSFET M10 is activated and output F1 = A is selected.

Case2: When S1S0 = 01

- MOSFET M4 and M7 gets activated due to S0 = 1; and output F1 = B and F2 = D is selected.
- F1 and F2 are fed to MOSFET M9 and M11 respectively; but due to S1 = 0 MOSFET M10 is activated and output F1 = B is selected.

Case3: When S1S0 = 10

- MOSFET M2 and M5 gets activated due to S0 = 1; and output F1 = A and F2 = C is selected.
- F1 and F2 are fed to MOSFET M9 and M11 respectively; but due to S1 = 1 MOSFET M12 is activated and output F2 = C is selected.

Case4: When S1S0 = 11

- MOSFET M4 and M7 gets activated due to S0 = 1; and output F1 = B and F2 = D is selected.
- F1 and F2 are fed to MOSFET M9 and M11 respectively; but due to S1 = 1 MOSFET M12 is activated and output F2 = D is selected.

Question 8: What is pull down device?

Answer:-

Pulldown - a network that provides a low resistance path to Gnd when output is logic '0' and provides a high resistance to Gnd otherwise.

A pull-down device when energized will pull-down the output to ground (i.e. "0").

NMOS is pull-down since it can provide a GOOD "0" i.e. (LOW).

NMOS can pull-down output to 0V but it can pull-up maximum to VDD-Vtn. So it is bad-1 and good-0.

whereVtn,Vtp are threshold voltage for NMOS and PMOS respectively.

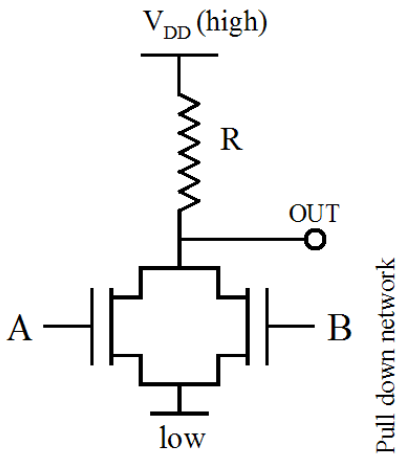


Fig7.

Question 9: What is pull up device?

Answer:

Pullup - a network that provides a low resistance path to Vdd when output is logic '1' and provides a high resistance to Vdd otherwise.

A pull-up device when energized will pull the ouput to supply(i.e "1") Usually PMOS is used for pull-up since it can provide GOOD "1" (HIGH) i.e VDD –Vtn. PMOS can pull-up output to VDD but it can pull-down to Vtp. So it is bad-0 but good-1. whereVtn,Vtp are threshold voltage for NMOS and PMOS respectively.

When the PMOS is used as a pull-up device:-

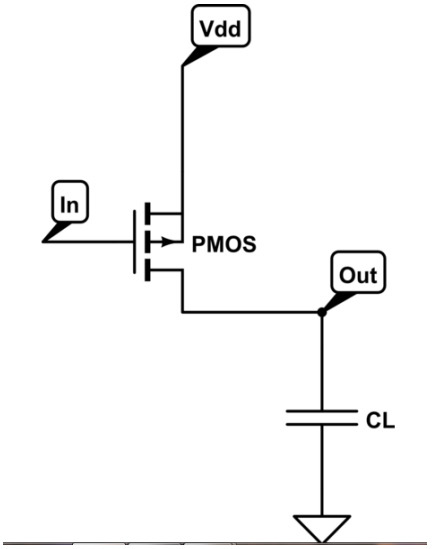


Fig 6.3

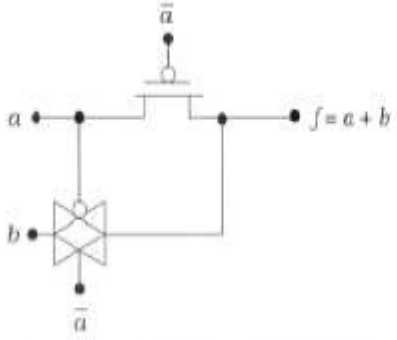
Initially the `Out` node is low and `In` is at Vdd. When `In` is lowered to gnd, the PMOS starts to

charge the load capacitor CL. At this initial moment, the source `S` is to Vdd, the gate `G` is to gnd, and the drain `D` is to gnd as well (the capacitor is initially discharged). With these voltages, the PMOS is in saturation region. It stays there until `Out` goes above `In` by exactly Vt, where Vt is the threshold voltage. Since `In` is to gnd, hence 0, the PMOS goes from saturation to linear region when `Out = Vt`. From now on, the PMOS behaves like a resistor, and keeps charging the capacitor till `Out = Vdd`. Note that throughout the whole time, the source to gate voltage of the PMOS, Vsg, is constant and equal to Vdd.

Question 10: Implement OR gate using Transmission gate.

Answer: OR gate using Transmission gate.

- TG based OR gate



$$f = a \cdot (\bar{\bar{a}}) + \bar{a} \cdot b$$
$$= a + \bar{a} \cdot b$$
$$= a + b$$

Figure A TG-based OR gate

Summary:

Now days, low power and low energy have become an important issue in consumer electronics and it is necessary to do research in combinational circuits. One of the important elements in digital circuits is a multiplexer or data selector for processing multiple inputs with a single output. Presently, multiplexers have become a universal logic element used to design any digital combinational logic circuits/systems in IC's, so it is needed to design or revise a multiplexer topology for low power consumption and high speed. In this paper, the different designs of multiplexer using complementary metal oxide semiconductor (CMOS) logic are analyzed in performance point of view.

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