Engineering Notebook

VOLUME 1

Basic Electronics EE2101

CONTRIBUTORs
Prof. A. B. Thatere
Prof. K. G. Pande
Prof. A. A. Peshattiwar
Prof. Ms. P. R. Chaudhari

DEPARTMENT OF ELECTRONICS ENGINEERING
YESHWANTRAO CHAVAN COLLEGE OF ENGINEERING,
(An autonomous institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University, Nagpur)
NAGPUR – 441 110

CONTENTS

UNIT NO. 1

Unit I: Number Systems and Codes
Introduction, Number System, Binary Number System, Signed Binary Numbers, Binary Arithmetic, 1's and 2's Complement Arithmetic, Octal Number System, Hexadecimal Number System, Codes-BCD code and Gray Code , BCD arithmetic.

Q. 1) *Explain Number System in detail.*
Answer : Number system defines a set of values used to represents quantity.
The different number systems are.

- Decimal Number system.
- Binary Number system.
- Octal Number system.
- Hexadecimal Number system.

Decimal Number System

The decimal number system is commonly used even though there are many other number systems like binary, octal, hexadecimal, etc. The decimal no. system contains 10 unique symbols 0,1,2,3,4,5,6,7,8 and 9.The number system having base or radix 10 is called as Decimal number system. Since counting in decimal involves 10 symbols, we say that its base or radix is 10.It is a positional weighted system. It means that the value attached to a symbol depends on its location with respect to the decimal point. Positional weights are 102, 101, 100, 10-1, 10-2 etc.In this system any number of any magnitudes can be represented by the use of these ten symbols only. Each symbol in the number is called digit.The leftmost digit in any number representation, which has the greatest positional weight out all the digits present in that number, is called the most significant digit (MSD) and the rightmost digit, which has the least positional weight out of all the digits present in that number, is called the least significant digit (LSD).

A collection of these digits makes a number which in general has two parts- INTEGER and FRACTIONAL, set apart by a radix point or decimal point (.), e.g.,

a) 1234 b) 210.36

In example (a) the number is an integer only and has no fractional part whereas in example (b) it is a mixed number having two parts- 210 is the integer and 36 is the fractional part.

In general any number can express as

(N)b = dn-1 dn-2 … di … d1d0 . d-1d-2 ... d-f …d-m

<--------Integer portion.--------> ↑ <---Fractional portion----->

Radix point

Where N is a number

b is radix or base of the number

n is number of digits in the integer portion

m is number of digits in the fractional portion

dn-1 is most significant digits (MSD) and d-m is least significant digits (LSD)

and $0 \leq (di \text{ or } df) \leq b-1$

Decimal number can be expressed in its positional weight as

1) $[1234]10 = 1*10^3 + 2*10^2 + 3*10^1 + 4*10^0 = 1234$

And so we say 4 is in units place, 3 is in tens place, 3 is in hundreds place, 1 is in thousands place.

2) $[210.36]10 = 2*10^2 + 1*10^1 + 0*10^0 + 3*10^{-1} + 6*10^{-2} = 210.36$

Binary Number system

The binary number system is the simplest number system as it consist of only two digits only.The number system having base or radix 2, is called as Binary number system.It has two independent symbols. The symbols used are 0 and 1.It is a positional weighted system. Positional weights are 2^2, 2^1, 2^0, 2^{-1}, 2^{-2} etc. A binary digit is called a bit. A binary number consist of a sequence of bits, each of which is either a 0 or 1. The binary point (.) separates the integer and fraction parts.The first bit to the left of the binary point has a weight of 2^0 and that column is called the unit's column. The second bit to the left has a weight of 2^1 and it is in the 2's column. The third bit to the left has a weight of 2^2 and it is in the 4's column, and so on.The first bit to the right of binary point has a weight of 2^{-1} and it is said to be in the ½'s column, the next right bit with a weight of 2^{-2} is in the ¼'s column and so on.

Decimal numbers and their corresponding binary numbers are listed in the table given below:

Decimal number	Binary number
0	0000
1	0001
2	0010
3	0011
4	0100
5	0101
6	0110
7	0111
8	1000
9	1001
10	1010
11	1011
12	1100
13	1101
14	1110
15	1111

A group of 8 bits is known as byte and group of 4 bits is known as nibble. The highest decimal number that can be represented by n-bits binary number is 2n -1(beginning with zero). Thus, with an 8- bit binary number, the highest decimal number that can be represented is 28 -1 = 255.
A Binary no. can be expressed as,
1) $[1010]2 = 1*2^3 + 0*2^2 + 1*2^1 + 0*2^0$
2) $[10.10]2 = 1*2^1 + 0*2^0 + 1*2^{-1} + 0*2^{-2}$

Octal Number system

The number system having base or radix 8, is called as octal number system.It has 8 independent symbols 0,1,2,3,4,5,6 and 7.It is a positional weighted system. Positional weights are 8^3, 8^2, 8^1, 8^0, 8^{-1}, 8^{-2}, 8^{-3} etc.Since its base 8 = 23, every 3-bit group of binary can be represented by an octal digit.An octal number is, thus, 1/3rd the length of the corresponding binary number.

Decimal number	Octal Number
0	0
1	1
2	2
3	3
4	4
5	5
6	6
7	7
8	10
9	11
10	12
11	13
12	14
13	15
14	16
15	17
16	20
17	21
18	22
19	23
20	24
21	25
22	26
23	27
24	30

$[23]8 = 2*8^1 + 3*8^0$

$[38.16]8 = 3*8^1 + 8*8^0 + 1*8^{-1} + 6*8^{-2}$

Hexadecimal Number system

Binary numbers are fine for machines but are too lengthy to be handled by human beings. So, there is a need to represent the binary numbers concisely. One number system developed with this objective is the hexadecimal number system.The number system having base or radix 16, is called as Hexadecimal no. system.It has 16 independent symbols 0,1,2,3,4,5,6,7,8,9,A,B,C,D.E and F.It is a positional weighted system. Positional weights are 16^3, 16^2, 16^1, 16^0, 16^{-1}, 16^{-2}, 16^{-3} etc.Since its base is 16 = 24, every 4 bit group can be represented by one hexadecimal digit. So, a hexadecimal number is ¼ the length of the corresponding binary number.

Decimal Number	Hexadecimal Number
0	0
1	1
2	2
3	3
4	4
5	5
6	6
7	7
8	8
9	9
10	A
11	B
12	C
13	D
14	E
15	F
16	10
17	11
18	12
19	13
20	14
21	15
22	16
23	17
24	18
25	19
26	1A
27	1B

$[9AB.\ D6]16 = 9*16^{2} + A*16^{1} + B*16^{0} + D*16^{-1} + 6*16^{-2}$

Q.2) *How to convert Binary number into decimal number system?*
Answer: Binary numbers may be converted to their decimal equivalents by the **positional weights method**. In this method, each binary digit of the number is multiplied by its position weight and the product terms are added to obtain the decimal number.
Whenever you look at the binary number, its decimal equivalent number can be found as follows:

1) Write the binary number.
2) Directly under the binary number write their respective weights 2^0, 2^1, 2^2, 2^3 from right to left.
3) Multiply that binary number with its respective positional weight.
4) Add the product terms to obtain final results.

Example 1. Convert 1011 to its decimal equivalent.

$[1011]_2 = [\ ]_{10}$
$[1011]_2 = 1*2^3 + 0*2^2 + 1*2^1 + 1*2^0$
$= 8 + 0 + 2 + 1$
$= 11$
$[1011]_2 = [\mathbf{11}]_{\mathbf{10}}$

Q.3) *How to convert Octal number into decimal number system?*
Answer: To convert an octal number to a decimal number, multiply each digit in the octal number by the weight of its position and add all the product terms.
Example: *Convert 27 into its equivalent decimal number.*

$[27]_8 = 2 \times 8^1 + 7 \times 8^0$
$= 16 + 7$
$= 23$
$[27]_8 = [\mathbf{23}]_{\mathbf{10}}$

Example: *Convert 23.23 into its equivalent decimal number.*

$[23.23]_8 = 2 \times 8^1 + 3 \times 8^0 + 2 \times 8^{-1} + 3 \times 8^{-2}$
$= 16 + 3 + 0.25 + 0.046875$
$= 19.29$
$[23.23]_8 = [\mathbf{19.29}]_{\mathbf{10}}$

Q.4) *How to convert Hexadecimal number into decimal number system?*
Answer: To convert a hexadecimal number into a decimal number, multiply each hexadecimal digit by its positional weight and add all the resulting product terms.
Example: *Convert 2F59 into its equivalent decimal number.*

$[2F59]_{16} = 2 \times 16^3 + F \times 16^2 + 5 \times 16^1 + 9 \times 16^0$
$= 2 \times 4096 + 15 \times 256 + 5 \times 16 + 9 \times 1$
$= 8192 + 3840 + 80 + 9$
$[2F59]_{16} = [\mathbf{12121}]_{\mathbf{10}}$

Example: *Convert A0F9.0EB into its equivalent decimal number.*

$[A0F9.0EB]_{16} = A \times 16^3 + 0 \times 16^2 + F \times 16^1 + 9 \times 16^0 + 0 \times 16^{-1} + E \times 16^{-2} + B \times 16^{-3}$
$= 10 \times 16^3 + 0 \times 16^2 + 15 \times 16^1 + 9 \times 16^0 + 0 \times 16^{-1} + 14 \times 16^{-2} + 11 \times 16^{-3}$
$= 40960 + 0 + 240 + 9 + 0 + 0.0546 + 0.0026$
$[A0F9.0EB]_{16} = [\mathbf{41209.0572}]_{\mathbf{10}}$

Q.5) *How to convert Decimal number into Binary number system?*
Answer: There are two methods to convert a decimal number to a binary number. These are the reverse processes of the two methods used to convert a binary number to a decimal number.
First Method**:** Express the given number as a sum of powers of 2 and the units 1s and 0s in the appropriate digit positions.
Example: *Convert 9 into corresponding binary number.*

$[9]_{10} = 8 + 0 + 0 + 1$
$= 1*2^3 + 0*2^2 + 0*2^1 + 1*2^0$
$= [\mathbf{1001}]_{\mathbf{2}}$

Example: *Convert 25 into corresponding binary number.*

$[25]_{10} = 16 + 8 + 0 + 0 + 1$
$= 1*2^4 + 1*2^3 + 0*2^2 + 0*2^1 + 1*2^0$
$= [\mathbf{11001}]_{\mathbf{2}}$

Second Method: In this method the decimal integer is converted to the binary integer by successive division by 2, and the decimal fraction is converted to binary fraction by successive multiplication by 2. This is known as *Double-dabble* method.
In the successive division by-2 method, the given decimal integer number is successively divided by 2 till the quotient is zero. The last remainder is the MSB. The remainders read from bottom to top give the equivalent binary integer.
In the successive multiplication by-2 method, the given decimal fraction is successively multiplied by 2, till the fraction part of the product is zero or till the desired accuracy is obtained. The first integer obtained is MSB. Thus the integers read from top to bottom give the equivalent binary

fraction.

Example: *Convert 52 to binary number*

	Quotient	Remainder	
52/2	26	0	(LSB)
26/2	13	0 ↑	
13/2	6	1 ↑	
6/2	3	0 ↑	
3/2	1	1 ↑	
1/2	0	1 ↑	(MSB)

$[52]_{10} = [\mathbf{110100}]_2$

Example: *Convert 0.65625 to an equivalent binary number.*

0.65625×2 = 1.31250 --------- 1 ↓ (MSB)
0.31250×2 = 0.62500 --------- 0 ↓
0.62500×2 = 1.2500 ---------- 1 ↓
0.2500×2 = 0.500 ------------ 0 ↓
0.500×2 = 1.000 ----------1 (LSB)

$[0.65625]_{10} = [\mathbf{10101}]_2$

Example: *Convert 25.5 to an equivalent binary number.*

a) Integer Part

	Quotient	Remainder
25/2	12	1
12/2	6	0 ↑
6/2	3	0 ↑
3/2	1	1 ↑
1/2	0	1 ↑

$[25]_{10} = [11001]_2$

b) Fractional part

0.500×2 = 1.000 ---------- 1

$[0.5]_{10} = [0.1]_2$

The result is $\mathbf{[25.5]_{10} = [11001.1]_2}$

Q.6) *How to convert Decimal number into Octal number system?*

Answer: To convert a decimal number to octal number, convert the integer and fraction parts separately. To convert the given decimal integer number to octal; successively divide the given number by 8 till the quotient is zero. The last remainder is the MSD. The remainders read from bottom to top give the equivalent octal integer.

To Convert the given decimal fraction to octal, successively multiply the decimal fraction by 8 till

the product is zero or till the required accuracy is obtained. The first integer from the top is the MSD. Thus the integers read from top to bottom give the equivalent octal fraction.

Example: *Convert 378.93 to its equivalent octal numbers.*

a) Integer part

	Quotient	Remainder
378/8	47	2
47/8	5	7 ↑
5/8	0	5 ↑

b) Fraction part

0.93×8 = 7.44 --------- 7 ↓
0.44×8 = 3.52 --------- 3 ↓
0.52×8 = 4.16 -------- 4 ↓
0.16×8 = 1.28 ---------1

$[378.93]_{10} = [572.\ 7341]_8$

Q.7) *How to convert Decimal number into Hexadecimal number system?*

Answer: To convert a decimal integer to hexadecimal, successively divide the given decimal number by 16 till the quotient is zero. The last remainder is MSB. The remainders read from bottom to top give the equivalent hexadecimal integer.

To convert a decimal fraction to hexadecimal, successively multiply the given decimal fraction by 16, till the product is zero or till the required accuracy is obtained. The first integer is the MSD and the integers read from top to bottom give the hexadecimal fraction.

Example: *Convert $[2598.675]_{10}$ into its equivalent hex number.*

a) Integer part- 2598

	Quotient	Remainder
2598/16	162	6
162/16	10	2 ↑
10/16	0	10 ↑

b) Fraction part

0.675 × 16 = 10.8 -------10 ↓
0.8 × 16 = 12.8 --------- 12 ↓
0.8 × 16 = 12.8 -------- 12 ↓
0.8 × 16 = 12.8 -------- 12 ↓

$[2598.675]_{10} = [A26.\ ACCC]_{16}$

Q.8) *How to convert Binary number into Octal number system?*

Answer: Binary number can be converted into its equivalent octal no. by making group of 3-bit, starting from LSB moving towards MSB for *integer part* & starting from MSB moving towards LSB for *fraction part* and then replacing each group of 3-bit by its octal representation.

Example: *Convert the binary 101010101011 to its equivalent octal number.*

$[101010101011]_2 = 101\ \ 010\ \ 101\ \ 011$

$= \mathbf{[5253]_8}$

Example. *Convert the binary 001010101.101010100 to its equivalent octal number.*

$[001010101.101010100]_2 = 001\ \ 010\ \ 101\ .\ 101\ \ 010\ \ 100$

$= \mathbf{[125.524]_8}$

Q.9) *How to convert Binary number into Hexadecimal number system?*
Answer: Binary number can be converted into its equivalent hexadecimal no. by making group of 4-bit, starting from LSB moving towards MSB for *integer part* & starting from MSB moving towards LSB for *fraction part* and then replacing each group of 4-bit by its hexadecimal representation.
Example: *Convert $[000111101010.101010101000]_2$ to its hexadecimal equivalent.*
$(111101010.101010101)_2$ = 0001 1110 1010 . 1010 1010 1000 = **$(1EA.AA8)_{16}$**

Q.10) *How to convert Octal number into Binary number system?*
Answer: To convert a given octal number to a binary, just replace each octal digit by its 3 bit binary equivalent.
Example: *Convert $(23)_8$ into its binary equivalent.*
$(23)_8$ = 010 011 = **$(010011)_2$**
Example: *Convert $(367.52)_8$ into its binary equivalent***.**
$(367.52)_8$ = 011 110 111 . 101 010 = **$(011110111.101010)_2$**

Q.11) *How to convert Hexadecimal number into Binary number system?*
Answer: To convert hexadecimal number to binary, replace each hex digit by its 4 bit binary group.
Example: *Convert $[ABC95.CDA]_{16}$ into its equivalent binary numbers.*
$(ABC95.CDA)_{16}$ = 1010 1011 1100 1001 0101 . 1100 1101 1010
= **$(10101011110010010101.110011011010)_2$**

Q.12) *How to convert Octal number into Hexadecimal number system?*
Answer: To convert a given octal number into hexadecimal number, first convert a given octal number to its equivalent binary number and then convert that binary into its equivalent hexadecimal number.
Example: *Convert $(367.52)_8$ into hexadecimal number.*
$(367.52)_8$ = 011 110 111 . 101 010 = **$(011110111.101010)_2$**
$(011110111.101010)_2$ = 1111 0111 . 1010 1000 = **$(F7.A8)_{16}$**

Q.13) *How to convert Hexadecimal number into Octal number system?*
Answer: To convert a given hexadecimal number into octal number, first convert a given hexadecimal number to its equivalent binary number and then convert that binary into its equivalent octal number.
Example: *Convert $(A27.BD)_{16}$ into hexadecimal number.*
$(A27.BD)_8$ = 1010 0010 0111 . 1011 1101 = **$(101000100111.10111101)_2$**
$(101000100111.10111101)_2$ = 101 000 100 111 . 101 111 010 = **$(5047.572)_8$**

Q. 14) *Find the base b if* $[525]_b = [305]_8$

Answer: Given: Base of the system is b

$(525)_b = 5 \times b^2 + 2 \times b^1 + 5 \times b^0$

$(525)_b = 5\ b^2 + 2\ b + 5$ --------- (1)

$[305]_8 = 3 \times 8^2 + 0 \times 8^1 + 5 \times 8^0$

$= 192 + 0 + 5$

$= [197]_{10}$ ---------- (2)

$5\ b^2 + 2\ b + 5 = [197]_{10}$

$5\ b^2 + 2\ b + 5 - 197 = 0$

$5\ b^2 + 2\ b - 192 = 0$

$5b^2 - 30\ b + 32b - 192 = 0$

$(b - 6)\ (5b + 32) = 0$

$b = 6,\ b = -32/5$

Hence, base of the system is 6.

Q. 15) *X and Y are two successive digits in a certain number system. When written as XY it becomes* $[25]_{10}$ *and when written as YX it becomes* $[31]_{10}$*. Find the base of the system and values of X and Y.*

Answer:

Given: $XY = [25]_{10}$ ---------- (1)

$YX = [31]_{10}$ ----------(2)

X and Y are two successive digits

If X= X then Y =X + 1 -----(3)

Let b = Base of the system

$[XY]_b = [25]_{10}$

$X \times b^1 + Y \times b^0 = 25$

$X \times b^1 + (X + 1) \times b^0 = 25$

$X\ b + X + 1 = 25$

$X\ b + X = 24$----------(4)

$[YX]_b = [31]_{10}$

$Y \times b^1 + X \times b^0 = 31$

$(X + 1) \times b^1 + X \times b^0 = 31$

$X \times b + b + X = 31$

$X\ b + X + b = 31$----------(5)

from (4) and (5)

$24 + b = 31$

b = 31 -24 = 7 --------- Ans 1

from (4)

X(b+1) = 24

X(7 + 1) = 24

X = 24 / 8 = 3 ---------- Ans 2

As Y = X + 1;

Y = 3 + 1 = 4 ---------- Ans 3

Q. 16) *P and Q are two successive digits in a certain number system. When written as PQ it becomes* $[41]_{10}$ *and when written as QP it becomes* $[49]_{10}$*. Find the base of the system and values of P and Q.*

Answer:

Given: $PQ = [41]_{10}$ ---------- (1)

$QP = [49]_{10}$ ----------(2)

P and Q are two successive digits

P = P and Q = P+1 -----(3)

let b = Base of the system

$[PQ]_b = [41]_{10}$

$P \times b^1 + Q \times b^0 = 41$

$P \times b^1 + (P + 1) \times b^0 = 41$

P b + P + 1 = 41

P b + P = 40----------(4)

$[QP]_b = [49]_{10}$

$Q \times b^1 + P \times b^0 = 49$

$(P+ 1) \times b^1 + P \times b^0 = 49$

$P \times b + b + P = 49$

P b + P + b = 49----------(5)

from (4) and (5)

40 + b = 49

b = 49 -40 =9 --------- Ans 1

from (4)

P (b+1) = 40

P (9 + 1) =40

P= 40 /10 = 4---------- Ans 2

As Q = P + 1;

Q= 4 + 1 = 5 ---------- Ans 3

Q 17) *The equation $5x^2+50x+125=0$ has the root -8,-5. Find the base of the system.*
Answer:
$125 = 1\times b^2 + 2\times b^1 + 5\times b^0 = b^2 + 2b + 5$
$50x = (5\times b^1 + 0\times b^0)x = (5b)x$
$5x^2 = (5\times b^0)x^2 = 5x^2$
Hence,
$5x^2 + 5bx + b^2 + 2b + 5 = 0$
For x = -8
$5(-8)^2 + 5b(-8) + b^2 + 2b + 5 = 0$
$b^2 - 38b + 325 = 0$
b = 25, b = 13
For x = -5
$5(-5)^2 + 5b(-5) + b^2 + 2b + 5 = 0$
b = 10, b = 13
Therefore the base of the system which satisfies the given roots is 13.

Q 18). *Find the base which will make following operator valid:*
i.$\sqrt{41} = [5]_{10}$, ii. 41 / 3 = 13, iii. (302) / 20 = 12.1

i.$\sqrt{41} = [5]_{10}$
Answer:
Let b be the base of the number system
$[\sqrt{41}]_b = [5]_{10}$
$\sqrt{(4\times b^1 + 1\times b^0)} = 5$
$\sqrt{(4b+1)} = 5$
Squaring both sides,
4b + 1 = 25
b = 6

ii. 41 / 3 = 13
Answer:
Let b be the base of the number system
$[41]_b / [3]_b = [13]_b$
$(4\times b^1 + 1\times b^0) / (3\times b^0) = 1\times b^1 + 3\times b^0$

$(4b + 1) / 3 = b + 3$
$4b + 1 = 3b + 9$
$b = 8$

iii.(302) / 20 = 12.1
Answer:
Let b be the base of the number system
$[302]_b / [20]_b = [12.1]_b$
$(3\times b^2 + 0\times b^1 + 2\times b^0) / (2\times b^1 + 0\times b^0) = 1\times b^1 + 2\times b^0 + 1\times b^{-1}$
$(3b^2 + 2) / 2b = b + 2 + b^{-1}$
$(3b^2 + 2) / 2b = (b^2 + 2b + 1) / b$
$3b^2 + 2 = 2b^2 + 4b + 2$
$b^2 - 4b = 0$
$b=0$ or $b=4$
Base can not be 0, therefore 4 is the base that makes the operator valid.

Q 19) *Perform following conversions*
i. $(110101.010)_2 = (?)_{10} = (?)_{16}$, *ii.* $(56.56)_{10} = (?)_2 = (?)_8$

i. $(110101.010)_2 = (?)_{10} = (?)_{16}$
Answer:
1) Real part: $(110101)_2$
$= 1 \times 2^5 + 1 \times 2^4 + 0 \times 2^3 + 1 \times 2^2 + 0 \times 2^1 + 1 \times 2^0$
$= 32 + 16 + 0 + 4 + 0 + 1$
$= (53)_{10}$
2) Fractional Part: 010
$= 0 \times 2^{-1} + 1 \times 2^{-2} + 0 \times 2^{-3}$
$= 0 + 0.25 + 0$
$= (0.25)_{10}$
Hence, $(110101.010)_2 = [53.25]_{10}$
Now, $(110101.010)_2 = 0011\ 0101.\ 0100 = (35.4)_{16}$

ii. $(56.56)_{10} = (?)_2 = (?)_8$

Answer:

a) Integer Part

Quotient	Remainder		
	56/2	28	0
	28/2	14	0 ↑
	14/2	7	0 ↑
	7/2	3	1 ↑
	3/2	1	1 ↑
	1/2	0	1 ↑

$[56]_{10} = [1110001_2$

b) Fractional part

$0.56 \times 2 = 1.12$ ---------- 1 ↓

$0.12 \times 2 = 0.24$ ---------- 0 ↓

$0.24 \times 2 = 0.48$ ---------- 0

$[.56]_{10} = [1001_2$

The result is $[56.56]_{10} = [111000.100]_2$

Now,

a) Integer Part

Quotient	Remainder		
	56/8	7	0
	7/8	0	7 ↑

$[56]_{10} = [70]_8$

b) Fractional part

$0.56 \times 8 = 4.48$ ---------- 4 ↓

$0.48 \times 8 = 3.84$ ---------- 3 ↓

$0.84 \times 8 = 6.72$ ---------- 6

$[.56]_{10} = [436]_8$

The result is $[56.56]_{10} = [70.436]_8$

Q.20) *How to Perform Binary Arithmetic operation?*
Answer: 1) BINARY ADDITION
The rules for binary addition are following:

Augend	Addend	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Example: *Add the binary numbers 1101.101 and 111.011.*
Solution:
1 1 0 1 . 1 0 1
+ 1 1 1 . 0 1 1
_____
1 0 1 0 1 . 0 0 0

2) BINARY SUBTRACTION
The Binary subtraction is performed in a manner similar to that in decimal subtraction. The rules for binary subtraction are:

Minuend	Subtrahend	Difference	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Example: *Subtract 001 from 100*
100
- 001

011

0-1 = 1; with borrow of 1 from next column

0 -1 (borrow) - 0 = 1, with borrow of 1

Example: *Subtract 111.111 from 1010.01*
Solution:
1 0 1 0 . 0 1 0
+ 1 1 1 . 1 1 1
_____
0 0 1 0 . 0 1 1

3) BINARY MULTIPLICATION

The rules for binary multiplication are:

$0 \times 0 = 0$; $1 \times 1 = 1$; $1 \times 0 = 0$; $0 \times 1 = 0$

This method is similar to the multiplication of decimal number on paper. Multiply the multiplicand with each bit of the multiplier, and add the partial products. The partial product is the same as the multiplicant if the multiplier bit is a 1 and is 0 if the multiplier bit is 0.

Example: *Multiply 1101 by 110*

Solution: The LSB of the multiplier is a 0 so, the first partial product is a 0. The next two bits of the multiplier are 1s. So, the next two partial products are equal to the multiplicand itself. The sum of the partial products gives the answer.

```
        1 1 0 1
        × 1 1 0
-------------------------
        0 0 0 0
      1 1 0 1
    1 1 0 1
-------------------------
1 0 0 1 1 1 0
```

Example: *Multiply 1011.101 by 101.01*

Solution:

```
          1 0 1 1 . 1 0 1
          × 1 0 1 . 0 1
 ---------------------------------
            1 0 1 1 1 0 1
          0 0 0 0 0 0 0
        1 0 1 1 1 0 1
      0 0 0 0 0 0 0
    1 0 1 1 1 0 1
-----------------------------------
1 1 1 1 0 1.0 0 0 0 1
```

4) BINARY DIVISION

In this method, long-division procedures similar to those in decimal are used.

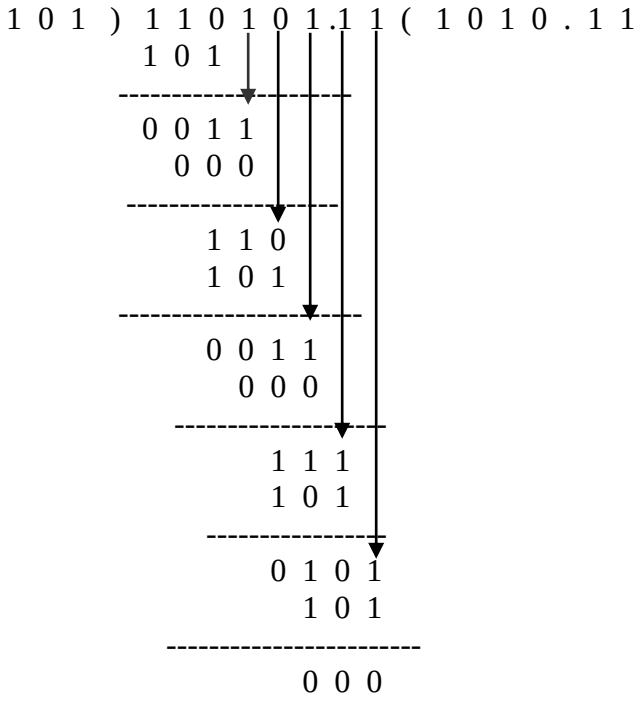
Example: *Divide 101101 by 110.*

Solution: Divisor 110 cannot go in the first three bits of the dividend, i.e., in 101. So, consider the first 4 bits 1011 of the dividend. 110 can go in 1011, one time with a remainder of 101. Next, 110 can go in 1010, one time with a remainder of 100. Next, 110 can go in 1001, one time with a remainder of 11. Finally, 110 can go in 110 with a remainder of 0.

```
1 1 0  )  1 0 1 1 0 1  (  1 1 1 . 1
            1 1 0
        ----------------------
            1 0 1 0
              1 1 0
        ----------------------
              1 0 0 1
                1 1 0
          ----------------------
                    1 1 0
                    1 1 0
               ----------------------
                    0 0 0
```

Therefore, 101101 ÷ 110 = 111.1

Example: *Divide 110101.11 by 101.*
Solution:



Therefore, 110101.11 ÷ 101 = 1010.11

Q 21) *Perform following using binary arithmetic.*
$(6AF.CD)_{16}$ + $(272.15)_8$ = $(?)_{10}$
Answer: $(6AF.CD)_{16} = (0110\ 1010\ 1111\ .\ 1100\ 1101)_2$
$(272.15)_8 = (010\ 111\ 010\ .\ 001\ 101)_2$

```
        011010101111 . 11001101
+       000010111010 . 00110100
-----------------------------------------
        011101101010 . 00000001
```

$(1*2^{10} + 1*2^9 + 1*2^8 + 1*2^6 + 1*2^5 + 1*2^3 + 1*2^1 + 1*2^{-8}) = (1898.0039)_{10}$

Q 22) *Perform following using binary arithmetic.*

$(9AB.1D)_{16} - (671.75)_8 = (?)_{10}$

Answer: $(9AB.1D)_{16} = 100110101011.00011101$

$(671.75)_8 = 000110111001.11110100$

011111110001.00101001

$(1*2^{10} + 1*2^9 + 1*2^8 + 1*2^7 + 1*2^6 + 1*2^5 + 1*2^4 + 1*2^1 + 1*2^{-3} + 1*2^{-5} + 1*2^{-8}) = (2033.1601)_{10}$

Q.23) *What is BCD Code? How to perform BCD arithmetic operation?*

Answer: BCD CODE:

The Binary Coded Decimal (BCD) is a combination of four binary bits that represent decimal numbers. It is weighted as well as sequential code. For example, the 8421 code is a type of binary coded decimal. It has 4 bits and represents the decimal digits 0 to 9. The numbers 8421 indicate the binary weights of the four bits. The ease of conversion between 8421 code numbers and the familiar decimal numbers is the main advantage of this code. To express any decimal number in BCD, each decimal digit should be replaced by the appropriate four-bit code.

Table gives the binary and BCD codes for the decimal number 0 to 15.

DECIMAL	BINARY	BCD
0	0000	0000
1	0001	0001
2	0010	0010
3	0011	0011
4	0100	0100
5	0101	0101
6	0110	0110
7	0111	0111
8	1000	1000
9	1001	1001

10	1010	0001 0000
11	1011	0001 0001
12	1100	0001 0010
13	1101	0001 0011
14	1110	0001 0100
15	1111	0001 0101

There are six illegal combinations **1010, 1011, 1100, 1101, 1110** and **1111.**

Example: *Give the BCD code for the Decimal number 874*

Solution: Decimal number 874

BCD code 1000 0111 0100

Hence $[874]_{10}$ = [**100001110100**]**BCD**

BCD ARITHMETIC

A) BCD ADDITION

The rule for addition of two BCD numbers is given below.

(i) Add the two numbers using the rules for binary addition.

(ii) If a four-bit sum is equal to or less than 9, it is a valid BCD number.

(iii) If a four-bit sum is greater than 9, or if a carry-out of the group is generated, it is an invalid result. Add 6 $(0110)_2$ to the four-bit sum in order to skip the six invalid states and return the code to BCD. If a carry results when 6 is added, add the carry to the next four-bit group.

Example: *Add the following BCD numbers: 1001 and 0100*

Solution

1 0 0 1	9
+ 0 1 0 0	+ 4
1 1 0 1 → Invalid BCD number	$[13]_{10}$
+ 0 1 1 0 → Add 6	
0 0 0 1 0 0 1 1 → Valid BCD number	

Example: *Add the following BCD numbers: 00011001 and 00010100*

0 0 0 1	1 0 0 1	19
+ 0 0 0 1	0 1 0 0	+ 14
0 0 1 0	1 1 0 1 → Right group is invalid	
	+ 0 1 1 0 → Add 6	
0 0 1 1 (3)	0 0 1 1 (3) → Valid BCD number	$[33]_{10}$

Example: *Add the following BCD numbers: 10011000 and 01111000*

	1 0 0 1 1 0 0 0	98
	+ 0 1 1 1 1 0 0 0	78
	1	
0 0 0 1	0 0 0 1 0 0 0 0 → carry is propagated	
	+ 0 1 1 0 + 0 1 1 0 → Add 6	
0 0 0 1 (1)	0 1 1 1 (7) 0 1 1 0 (6) → Valid BCD number	$[+ 176]_{10}$

B) BCD SUBTRACTION

The rule for subtraction of two BCD numbers is given below.

(i) Subtract the digits of each 4-bit group of the subtrahend from the corresponding 4-bit group of the minuend in binary starting from LSD.

(ii) If there is no borrow from the next higher group then no correction is required.

(iii) If there is borrow from the next higher group, then 6 $(0110)_2$ is subtracted from the difference term of this group.

Example: *Subtract the following BCD numbers: $(206.7)_{10} – (147.8)_{10}$*

Solution

	0 0 1 0	0 0 0 0	0 1 1 0 . 0 1 1 1	
-	0 0 0 1	0 1 0 0	0 1 1 1 . 1 0 0 0	
	1 ↙	1 ↙	1 ↙	
	0 0 0 0	1 0 1 1	1 1 1 0 . 1 1 1 1	→ Borrow taken
-		0 1 1 0	0 1 1 0 0 1 1 0	
	0 0 0 0 (0)	0 1 0 1 (5)	1 0 0 0 (8) . 1 0 0 1 (9)	→ Valid BCD number

Q 24) *Perform following using BCD arithmetic.*

$(8B4.1D)_{16} + (377.15)_8 = (?)_{10}$

Answer: $(8B4.1D)_{16} = (2228.113)_{10}$ = 0010001000101000.000100010011

$(377.15)_8 = (255.203)_{10}$ = 0000001001010101.001000000011

```
                    ------------------------------------------------
                      0010010001111101.001100010110
                    +                 0110
                   ------------------------------------------------
                      0010010010000011.001100010110
```

Ans :- $(2483.316)_{10}$

Q 25) *Perform following using BCD arithmetic.*

$(7E4.24)_{16} - (401.24)_8 = (?)_{10}$

Answer: $(7E4.24)_{16} = (2020.14)_{10}$ = 0010000000100000.00010100

$(401.24)_8 = (257.31)_{10}$ = 0000001001010111.00110001

```
                        ----------------------------------------
                          0001110111001000.11100011
                    -           011001100110 0110
                   ----------------------------------------------------
                          0001011101100010.10000011
```

ANS :- $(1762.83)_{10}$

Q. 26) *What is Gray Code? How to convert Binary Number into Gray code and Vice Versa?*

Answer: GRAY CODE:

Gray code is another non-weighted code, because the bit positions in the code group do not have any specific weight assigned to them. Hence it is not suitable for any arithmetic operations. It is a very useful code in which a decimal number is represented in binary form in such a way so that each gray code number differs from the preceding and the succeeding number by a single bit. As only one bit changes at a time, the gray code is called as a "Unit distance" code. The gray code is a cyclic code.

For example, the gray code for decimal number 5 is 0111 and for 6 is 0101. These two codes differ by only one bit position.

DECIMAL	BINARY	GRAY CODE
0	0000	0000
1	0001	0001
2	0010	0011
3	0011	0010
4	0100	0110
5	0101	0111
6	0110	0101
7	0111	0100
8	1000	1100
9	1001	1101
10	1010	1111
11	1011	1110
12	1100	1010
13	1101	1011
14	1110	1001
15	1111	1000

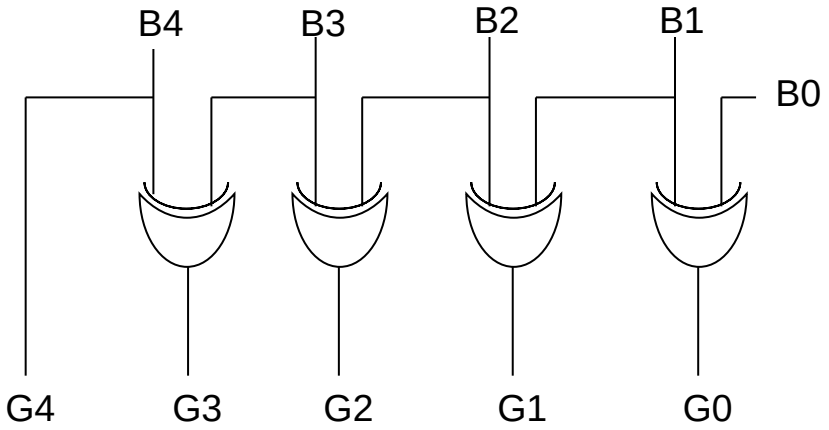
BINARY TO GRAY CONVERSION

Binary number can be converted into its equivalent gray code by following process.

a) The MSB of gray code is same as MSB of binary number.
b) Moving from left to right, remaining bits of gray code are obtained by "EXCLUSIVE ORing" the adjacent pairs of binary bits.
c) If binary number is represented as $B_4B_3B_2B_1B_0$ and corresponding gray code is represented as $G_4G_3G_2G_1G_0$, then

$G_4 = B_4$
$G_3 = B_4 \oplus B_3$
$G_2 = B_3 \oplus B_2$
$G_1 = B_2 \oplus B_1$
$G_0 = B_1 \oplus B_0$

Logic diagram for binary to gray code conversion is shown in fig.



EXAMPLE: *Convert the binary 1001 to the gray code.*

Solution: BINARY 1 ⊕ 0 ⊕ 0 ⊕ 1

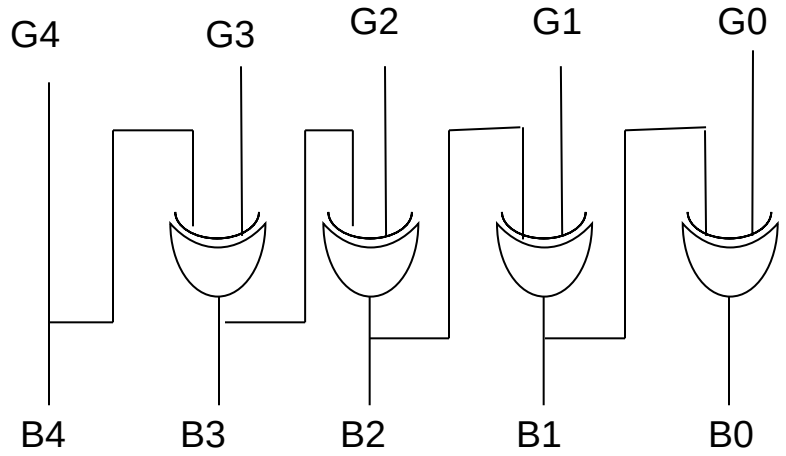
GRAY **1** **1** **0** **1**

GRAY TO BINARY CONVERSION

For this conversion following process is adopted:

a) MSB of binary code is same as MSB of Gray code.
b) Moving from left to right, remaining bits of binary code are obtained by "EXCLUSIVE ORing" the output gray with next binary input.
c) If gray code is given by $G_4G_3G_2G_1G_0$, and equivalent binary code is given by $B_4B_3B_2B_1B_0$, then
   $B_4 = G_4$
   $B_3 = B_4 \oplus G_3$
   $B_2 = B_3 \oplus G_2$

$B_1 = B_2 \oplus G_1$
$B_0 = B_1 \oplus G_0$
Logic diagram for gray to binary conversion is shown in fig.



EXAMPLE: *Convert the Gray code 11101 to the binary code.*
Solution:

G_4	G_3	G_2	G_1	G_0
1	**1**	**1**	**0**	**1**
1	**0**	**1**	**1**	**0**
B_4	B_3	B_2	B_1	B_0

$[11101]_G$ = **$[10110]_2$**

Q 27) *Convert*
1) $(56.15)_{10} = (?)_{Gray}$
2) $(1011010.1101)_{Gray} = (?)_{10}$
1) $(56.15)_{10} = (?)_{Gray}$
Answer: $(56.15)_{10} = (111000.001)_2$
$(111000.001)_2 = (100100.001)_{Gray}$

2) $(1011010.1101)_{Gray} = (?)_{10}$
Answer: $(1011010.1101)_{Gray} = (1101100.1001)_2$
$(1101100.1001)_2 = (108.56)_{10}$

Q. 28) *How to represent Binary number in 1's and 2's complement form?*

Answer: 1) 1's COMPLEMENT REPRESENTATION

In a binary number, if each 1 is replaced by 0 and each 0 by 1, the resulting number is known as the 1's complement of the first number. In fact, both the numbers are complement of each other. If one of these numbers is positive, then the other number will be negative with the same magnitude and vice-versa.

For example, $(0101)_2$ represents $(+5)_{10}$, whereas $(1010)_2$ represents $(-5)_{10}$ in this representation. This method is widely used for representing signed numbers. In this representation also, MSB is 0 for positive numbers and 1 is for negative numbers.

Example 1: *Find 1's complement of the following binary numbers.*

a) 0100111001 b) 11011010

Sol: a) 1011000110 b) 00100101

Example 2: *Represent the following decimal numbers in 1's complement form using 8-bits.*

a) -67 b) 102

Sol: a) $(67)_{10} = (1000011)_2$

Using 8-bit representations, $(01000011)_2$

Using 1's complement, $\mathbf{(10111100)_2 = (-67)_{10}}$

b) $(102)_{10} = (1100110)_2$

Using 8-bit representations, $\mathbf{(01100110)_2}$

The 1's complement of the positive number is same as the sign-magnitude representation of the positive number.

Example 3: *Find decimal equivalent of the following binary numbers represented in 1's complement form. a) $(10100111)_2$ b) $(01010011)_2$*

Sol: a) The MSB of a given number is 1; the sign is negative.

Hence 1's complement of a number is $(01011000)_2$

Decimal equivalent, $(01011000)_2 = 0+64+0+16+8+0+0+0 = \mathbf{(-88)_{10}}$

b) The MSB of a given number is 0; the sign is positive.

Decimal equivalent, $(01010011)_2 = 0+64+0+16+0+0+2+1 = \mathbf{(+83)_{10}}$

2) 2's COMPLEMENT REPRESENTATION

If 1 is added to LSB of 1's complement of a binary number, the resulting number is known as the 2's complement of the binary number. The 2,s complement operation on a signed number will change a positive number to a negative number and vice versa. In this representation also, MSB is 0 for positive numbers and 1 is for negative numbers. For example, 2's complement of 0101 is 1011.

Example 1: *Find the 2's complement of the binary numbers.*

a) 01001110 b) 00110101

Sol:	**a) Number**	0 1 0 0 1 1 1 0	**b) Number**	0 0 1 1 0 1 0 1
	1's complement	1 0 1 1 0 0 0 1	**1's complement**	1 1 0 0 1 0 1 0
	Add 1	1	**Add 1**	1
		----------		----------
		1 0 1 1 0 0 1 0		**1 1 0 0 1 0 1 1**

Example 2: *Represent the following decimal numbers in 2's complement using 8-bits.*

a) -44 b) 64

Sol: a) $(44)_{10} = (101100)_2$

Using 8-bit representation, $(00101100)_2$

2's complement, $\mathbf{(11010100)_2 = (-44)_{10}}$

b) $(64)_{10} = (1000000)_2$

Using 8-bit representation, $\mathbf{(01000000)_2}$

The 2's complement of the positive number is same as the sign-magnitude representation of the positive number.

Example 3: *Find decimal equivalent of the following binary numbers represented in 2's complement form. a) $(10011001)_2$ b) $(01100111)_2$*

Sol: a) The MSB of a given number is 1; the sign is negative.

Hence 2's complement of a number is $(01100111)_2$

Decimal equivalent, $(01100111)_2 = 0+64+32+0+0+4+2+1 = \mathbf{(-103)_{10}}$

b) The MSB of a given number is 0; the sign is positive.

Decimal equivalent, $(01100111)_2 = 0+64+32+0+0+4+2+1 = \mathbf{(+103)_{10}}$

Q. 29) *How to Perform 1's and 2's complement arithmetic for unsigned number?*
Answer: Subtraction of a number from another can be accomplished by adding the complement of the subtrahend to the minuend. The exact difference can be obtained with minor manipulations.
1'S COMPLEMENT SUBTRACTION
Subtraction of binary numbers using the 1's complement method allows subtraction only by addition.
A) To subtract a smaller number from a larger number, the 1's complement method is as follows:

(i) Determine the 1's complement of the smaller number.
(ii) Add this to the larger number.
(iii) There is always a carry.
(iv) Remove the carry and add it to the result. This carry is called as **end-around-carry.**

Example: *Subtract $(1010)_2$ from $(1111)_2$ using the 1's complement method. Also subtract using direct method and compare.*

Sol: Direct subtraction

```
   1 1 1 1
 - 1 0 1 0
 ----------
   0 1 0 1
```

1's Complement method

```
                        1 1 1 1
1's Complement →        0 1 0 1     (+)
                     -----------
Carry          →      1 0 1 0 0
Add Carry      →              1
                     -----------
                        0 1 0 1
```

B) Subtraction of a larger number from a smaller one by the 1's complement method involves the following steps:

(i) Determine the 1's complement of the larger number.
(ii) Add this to the smaller number.
(iii) There is no carry.
(iv) To get an answer in true form. Take the 1's complement and change the sign.
(v)

Example: *Subtract $(1010)_2$ from $(1000)_2$ using the 1's complement method. Also subtract using direct method and compare.*

Sol: Direct subtraction

```
   1 0 0 0
 - 1 0 1 0
 ----------
 - 0 0 1 0
```

1's Complement method

```
                        1 0 0 0
1's Complement →        0 1 0 1     (+)
                     -----------
                        1 1 0 1
```

As MSB is 1, result is negative. To get true result, take 1's complement of the result and change the sign.

1's complement: **- (0010)**

2'S COMPLEMENT SUBTRACTION

Subtraction of binary numbers using the 2's complement method allows subtraction only by addition. The 2's complement of a binary number can be obtained by adding 1 to its 1's complement.

A) Subtraction of a smaller number from a larger one by the 2's complement method involves following steps:

(i) Determine the 2's complement of the smaller number.
(ii) Add this to the larger number.
(iii) There is always a carry.
(iv) Omit the carry.
(v)

Example: *Subtract $(1010)_2$ from $(1111)_2$ using the 2's complement method. Also subtract using direct method and compare.*

Sol: Direct subtraction

```
  1 1 1 1
- 1 0 1 0
---------
  0 1 0 1
```

2's Complement →

1's Complement method

```
  1 1 1 1
  0 1 1 0   (+)
-----------
1 0 1 0 1
```

Carry → **1**

The carry is discarded. Thus, the answer is $(0101)_2$.

B) The 2's complement method for subtraction of a larger number from a smaller one is as follows:

(i) Determine the 2's complement of the larger number.
(ii) Add the 2's complement to the smaller number.
(iii) There is no carry. The result is in 2's complement form and is negative.
(iv) To get an answer in true form. Take the 2's complement and change the sign.

Example: *Subtract $(1010)_2$ from $(1000)_2$ using the 2's complement method. Also subtract using direct method and compare.*

Sol: Direct subtraction

```
  1 0 0 0
- 1 0 1 0
---------
- 0 0 1 0
```

2's Complement →

2's Complement method

```
  1 0 0 0
  0 1 1 0   (+)
-----------
  1 1 1 0
```

As MSB contain 1, the result is negative. To get true result, take 2's complement of the result and change the sign.

2's complement: **- (0010)**

The Advantage in 2's Complement method is that the end-around carry operation present in the 1's complement method is not involved here. The 2's Complement method is particularly useful in arithmetic logic circuits because subtraction can be accomplished with the help of an adder.

Comparison between 1's and 2's Complement (Arithmetic)

1) The 1's complement can be easily obtained using an inverter. The 2's complement has to be arrived at by first obtaining the 1's complement and then adding one (1) to it.

2) The advantage in 2's complement system is that only one arithmetic operation is required, the 1's complement requires two operations.

3) While 1's complement is often used in logical manipulations for inversion operation, the 2's complement is used only for arithmetic applications.

Q. 30) *Perform following using 1's compliment method*

i) subtract $(10110)_2$ from $(110)_2$

ii) Subtract $(11)_2$ from $(101101)_2$

Answer : i) take 1s compliment of 10110 = 01001

Add with 110 = 00110

01001

01111

Take 1s compliment of result = -(10000)

ii) take 1s compliment of 000011 = 111100

Add with 101101 = 101101

111100

1101001

1

101010

Q. 31) *Perform following using 2's compliment method*
i) subtract $(111011)_2$ from $(1010)_2$
ii) Subtract $(1101)_2$ from $(1101101)_2$
Answer: i) take 2s compliment of 111011 = 000101
Add with 1010 = 000101
001010

001111
Take 2s compliment of result = $-(110001)_2$

ii) take 2s compliment of 0001101 = 1110011
Add with 1101101 = 1101101
1110011

11100000

Q. 32) *How to Perform 2's complement arithmetic for signed number?*
Answer: Binary numbers are represented with a separate sign bit along with the magnitude, as shown below. For example, in an 8-bit binary number, the MSB is the sign bit and the remaining 7 bits correspond to magnitude. The magnitude part contains true binary equivalent of the number for positive numbers, while 2's complement form of the number for negative numbers. For example, +13, 0, -46 are represented as follows:

	Sign	Magnitude
+13	0	000 1101
0	0	000 0000
-46	1	010 1110

It is important to note that the number zero is assigned with the sign bit '0'. Therefore, the range of numbers that can be represented using 8-bit binary number is -128 to +127. In general, the range of numbers that can be represented by an n-bit number is (-2^{n-1}) to $(+-2^{n-1}-1)$.

A) ADDITION IN THE 2'S COMPLEMENT SYSTEM

Addition can be explained with four possible cases:

CASE I: Two Positive numbers

Example: *$[+29]_{10}$ + $[+19]_{10}$ using 2's complement method*

Sol:

```
+29 --------  0   001   1101   (augend)
+19 --------  0   001   0011   (addend)
              ----------------------
              0   011   0000   ( Sum = 48 )
              ↑
          Sign bit
```

The sign bits of both augend and addend are zero and the sign bit of the sum is 0, indicating that when the sum is positive they have the same number of bits.

CASE II: Positive Augend number and Negative Addend number

Example: *$[+39]_{10}$ + $[-22]_{10}$ using 2's complement method*

Sol: -22 will be in its 2's complement form. Therefore, +22 [00010110] must be converted to -22 [11101010].

```
+39 --------  0   010   0111   (Augend)
-22 --------  1   110   1010   (addend)
              ----------------------
1             0   001   0001   ( Result = +17)
↑             ↑
Carry      Sign bit
```

This carry is neglected. Sign bit is 0, hence result is positive.

CASE III: Negative Augend number and Positive Addend number

Example: *$[-47]_{10}$ + $[+29]_{10}$ using 2's complement method*

Sol: -47 will be in its 2's complement form. Therefore, +47 [00101111] must be converted to -47 [11010001].

```
 -47 --------  1   101   0001   (augend)
+29 --------  0   001   1101   (addend)
              ----------------------
              1   110   1110   ( Result = -18 )
              ↑
          Sign bit
```

As sign bit is 1, result is negative number and is in the 2's complement form. The true magnitude of the result can be found by taking the 2's complement of 1101110; the result is 10010 (+18).

CASE IV: Two negative numbers

Example: *$[-32]_{10}$ + $[-44]_{10}$ using 2's complement method*

Sol: -32 and -44 will be in its 2's complement form. Therefore, +32 [00100000] must be converted to -32 [11100000] and +44 [00101100] must be converted to -44 [11010100].

```
-32 --------  1   110   0000   (augend)
-44 --------  1   101   0100   (addend)
              ----------------------
 1            1   011   0100   ( Result = -76 )
 ↑            ↑
Carry      Sign bit
```

The carry is discarded. As sign bit is 1, result is negative number and is in the 2's complement form. The true magnitude of the result can be found by taking the 2's complement of 0110100; the result is 1001100 (+76).

B) SUBTRACTION IN THE 2'S COMPLEMENT SYSTEM

Subtraction by the 2's complement system involves addition.

Subtraction can be explained with four possible cases:

CASE I: Two Positive Numbers

Example: *$[+28]_{10}$ - $[+19]_{10}$ using 2's complement method*

Sol: It is equivalent to $[+28]_{10} + [-19]_{10}$

-19 will be in its 2's complement form. Therefore, +19 [00010011] must be converted to -19 [11101101].

```
+28 --------  0   001   1100   (Minuend)
 -19 --------  1   110   1101   (Subtrahend)
              ----------------------
1             0   000   1001   ( Result = +9 )
↑             ↑
Carry      Sign bit
```

Carry is discarded. As sign bit is 0, result is positive.

CASE II: Positive Minuend and Negative Subtrahend number

Example: *$[+39]_{10}$ - $[-21]_{10}$ using 2's complement method*

Sol: -21 will be in its 2's complement form. Again (-21) has negative sign, hence find its 2's complement. Therefore, +21 [00010101] is same as –(-21) [00010101].

```
+39 --------  0   010   0111   (Minuend)
+21 --------  0   001   0101   (Subtrahend)
              -----------------------
              0   011   1100   ( Result = +60 )
              ↑
          Sign bit
```

Carry is discarded. As sign bit is 0, result is positive.

CASE III: Negative Minuend and Positive Subtrahend number

Example: *$[-19]_{10}$ - $[+43]_{10}$ using 2's complement method*

Sol: It is equivalent to $[-19]_{10} + [-43]_{10}$

-19 and -43 will be in its 2's complement form. Therefore, +19 [00010011] must be converted to -19 [11101101] and +43 [00101011] must be converted to -43 [11010101].

```
-19 --------  1   110   1101   (Minuend)
-43 --------  1   101   0101   (Subtrahend)
              -----------------------
  1           1   100   0010   ( Result = -62 )
  ↑           ↑
Carry     Sign bit
```

The carry is discarded. As sign bit is 1, result is negative number and is in the 2's complement form. The true magnitude of the result can be found by taking the 2's complement of 1000010; the result is 0111110 (+62).

CASE IV: Two Negative Numbers

Example: *$[-57]_{10}$ - $[-33]_{10}$ using 2's complement method*

Sol: -57 will be in its 2's complement form. Therefore, +57 [00111001] must be converted to -57 [11000111]. -33 will be in its 2's complement form. Again (-33) has negative sign, hence find its 2's complement. Therefore, +33 [00100001] is same as –(-33) [00100001].

```
   -57 --------  1   100   0111   (Minuend)
-(-33) --------  0   010   0001   (Subtrahend)
              -----------------------
              1   110   1000   (Result = -24 )
              ↑
          Sign bit
```

As sign bit is 1, result is negative number and is in the 2's complement form. The true magnitude of the result can be found by taking the 2's complement of 1101000; the result is 0011000 (+24).

Q.33) *Perform using sign number arithmetic*

i) $[+25]_{10} + [-56]_{10}$

ii) $[-62]_{10} - [+32]_{10}$

Answer : i) [+25] = 00011001

\+

[-56] = 11001000

[-31] 11100001

ii) [-62] = 11000010

[+32] = 00100000

[-[+32]] = 11100000

\+

[-62] = 11000010

[-94] ⊥10100010

Q.34) *Perform using sign number arithmetic*

i) $[-45]_{10} + [-62]_{10}$

ii) $[-24]_{10} - [-92]_{10}$

Ans: i) $[-45]_{10} + [-62]_{10}$

$[-45]_{10}$ = 11010011

\+

$[-62]_{10}$ = 11000010

[-107] ⊥10010101

ii) $[-24]_{10} - [-92]_{10}$

$[-24]_{10}$ = 11101000
+
$-[-92]_{10}$ = 01011100

[+68] = ~~1~~01000100

Reference:

"Modern Digital Electronics" by R. P. Jain, 4th Edition, McGraw Hill Education Private Limited, published in 2015

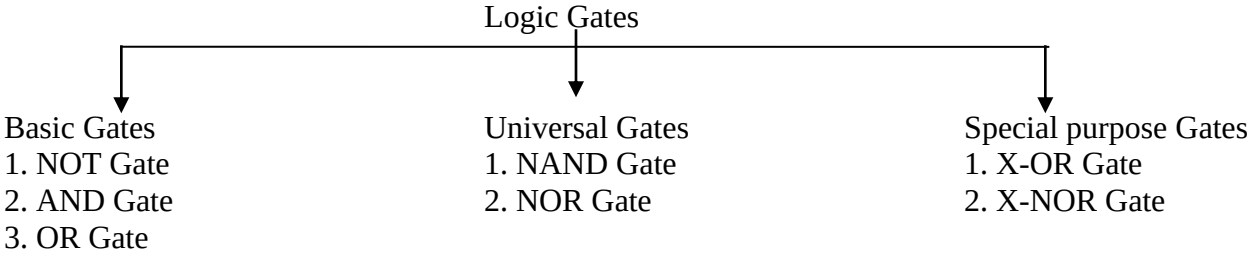
UNIT NO. 2

***Unit II*: Digital Principles and Logic Design**
Logic Gates, Boolean Laws & Algebras, Sum of Product & Product of Sum, Combinational Logic Design - Half & Full Adder, Half & Full Subtractor, Sequential Logic Circuits – Flip-flops

Q. 1) *What is Logic gates? Draw Truth table and symbol of all logic gates.*
Answer:
Logic gates are the fundamental building blocks of digital system. Logic gates are electronic circuits because they are made up of a number of electronic devices and components.

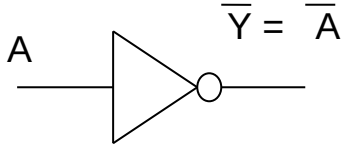
It is an electronic circuit having one or more than one inputs and only one output. The name logic gates is derived from the ability of such a device to make decisions, in the sense that it produces one output level when some combination of input levels are present, and the different output level when other combinations of input levels are present. Each gate is dedicated to a specific logic operation. They are constructed in a wide variety of forms. Inputs and outputs of logic gates can occur only in two levels. These two levels are termed HIGH and LOW, or TRUE and FALSE, or ON and OFF, or simply 1 and 0.

There are just three basic types of gates- AND, OR and NOT.



A) NOT Gate (INVERTER) :
NOT Gate is the basic gate which has only one input and only one output. It is a device whose output is always the complement of its input. That is the output of a NOT gate assumes the logic 1 states when its input is in logic 0 state and assumes the logic 0 state when its input is in logic 1 state. The Boolean expression for NOT gate is Y = A. The logic symbol and truth table for NOT gate is shown below

INPUT Y = A	OUTPUT $\overline{A}$
0	1
1	0

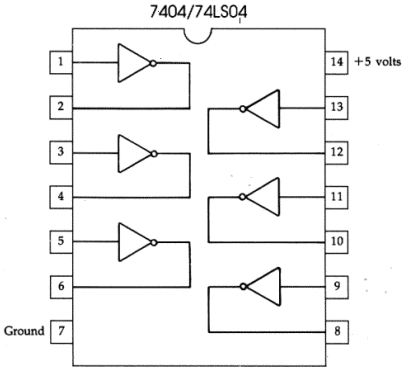


From the truth table, it is observed that when input is 1, output is 0. And when input is 0, output is 1. Hence the NOT gate is also called as INVERTER or COMPLEMENTARY Gate.

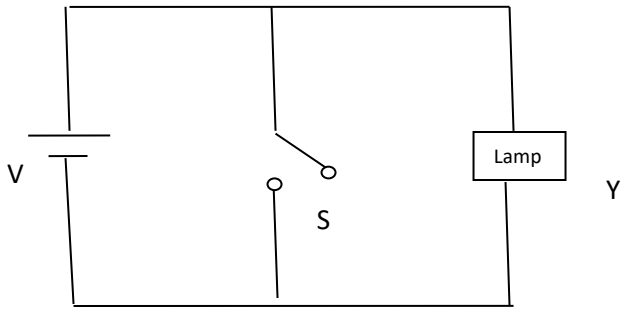
SWITCHING CIRCUIT: -

When power supply is given and switch is closed that is A = 1, then current will pass through switch and no current will conduct through lamp. Therefore lamp does not glow that is Y = 0.

When switch 'S' is open (A = 0), then current will conduct through the lamp and lamp will glow, that is Y = 1.



IC diagram for NOT gate (IC 7404)



B) AND Gate:-

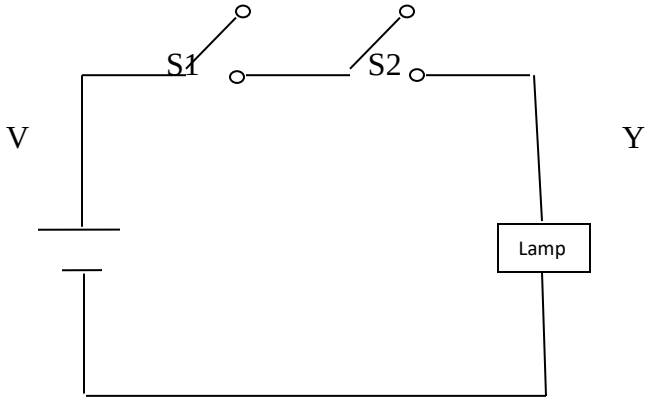
The AND Gate is a basic gate, it has two or more than two inputs and only one output.

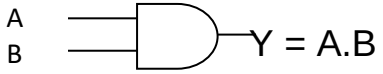
It performs logical "ANDing" operation. The Boolean expression for two input AND gate is Y = A.B which is read as A AND B. The logic symbol of two input AND gate and its truth table is shown below.

INPUTS		OUTPUT
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

From the truth table it is observed that, output of AND Gate is logic 1, when all the inputs are logic 1, otherwise output is 0. Hence the AND Gate is also called an *all* or *nothing* gate.

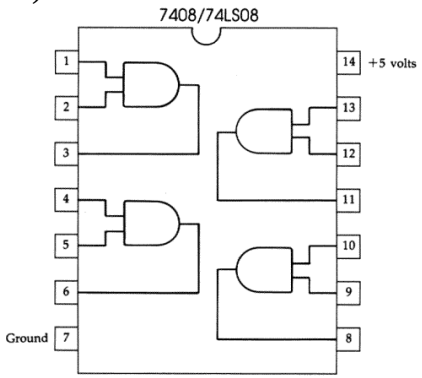
SWITCHING CIRCUIT:-





When both switches are closed that is S1 = S2 = 1, the current will conduct through the circuit. Hence lamp will glow that is Y = 1.When S1 = open and S2 = close, no current will conduct through lamp. Hence lamp does not glow that is Y = 0.When S2 = open and S1 = close, no current will conduct through lamp. Hence lamp does not glow that is Y = 0.When both switches are open that is S1 = S2 = 0, no current will conduct through the circuit. Hence lamp will not glow that is Y = 0.

IC Diagram for AND gate (IC 7408)



C) OR Gate:

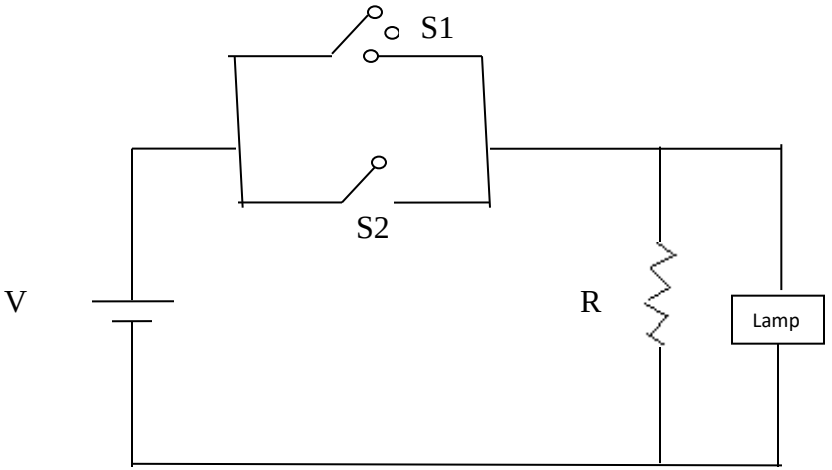
The OR Gate is a basic gate; it has two or more than two inputs and only one output. It performs logical "ORing" or addition operation. The Boolean expression for two input OR gate is given by Y = A + B which is read as A OR B.

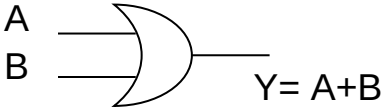
The logic symbol of two input OR gate and its truth table is shown below.

INPUTS		OUTPUT
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

From the truth table it is observed that, output of OR Gate is logic 1, when any one input or all the inputs are logic 1, otherwise output is 0. Hence the OR Gate is also called an *any* or *all gate*.

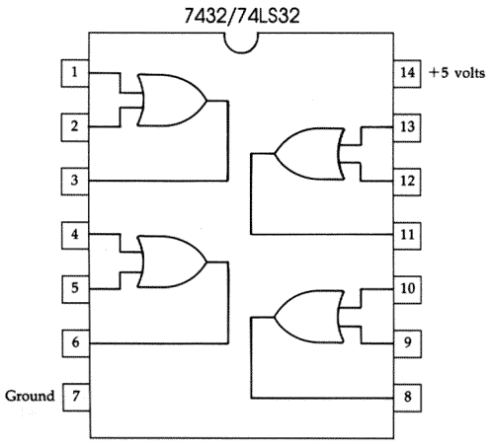
SWITCHING CIRCUIT:-





When both switches are open that is S1 = S2 = 0, no current will conduct through the circuit. Hence lamp will not glow that is Y = 0.When S1 = open and S2 = close, current will conduct through lamp. Hence it will glow that is Y = 1.When S2 = open and S1 = close, current will conduct through lamp. Hence again the lamp will glow that is Y = 1.When both switches are closed that is S1 = S2 = 1, again current complete its path and lamp will glow that is Y=1.

IC diagram for OR Gate (IC 7432)



UNIVERSAL GATES

Though logic circuits of any complexity can be realized by using only the three basic gates, there are two universal gates (NAND and NOR), each of which can also realize logic circuit single-handedly. The NAND and NOR gates are therefore, called universal building blocks. Both NAND and NOR gates can perform all the three basic logic functions (AND, OR and NOT).

NAND Gate:-

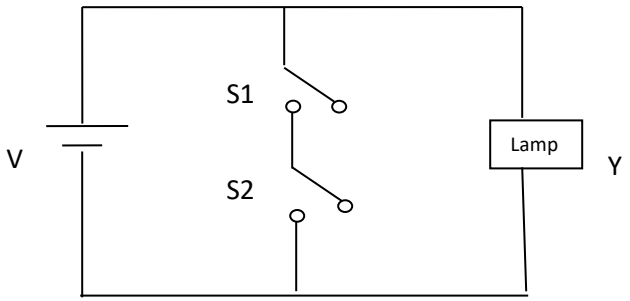
NAND means NOT-AND, that is the AND output is NOTed. So, a NAND gate is a combination of an AND Gate and a NOT Gate. It has two or more than two inputs and only one output. The Boolean expression for NAND gate is $Y = \overline{A.B}$

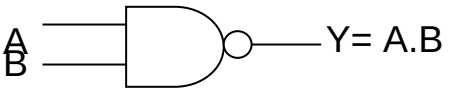
Logic symbol for two inputs NAND Gate and its truth table is shown below.

INPUTS		**OUTPUT**
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

From truth table it is observed that when any one input or all the inputs of NAND Gate are 0 then output of NAND Gate is 1 otherwise output is 0.

SWITCHING CIRCUIT:-

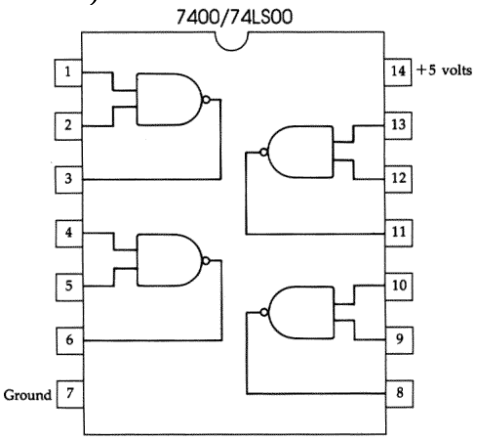




When both switches are open that is S1 = S2 = 0, current will conduct through the circuit. Hence lamp will glow that is Y = 1.When S1 = open and S2 = close, current will conduct through lamp. Hence it will glow that is Y = 1.When S2 = open and S1 = close, current will conduct through

lamp. Hence again the lamp will glow that is Y = 1.When both switches are closed that is S1 = S2 = 1, no current will conduct through the lamp, hence it will not glow that is Y = 0.

IC diagram for NAND Gate (IC 7400)



NOR Gate:-

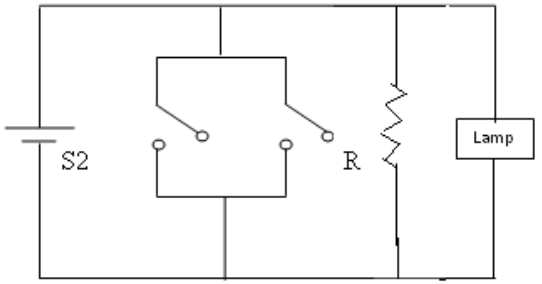
NOR means NOT-OR, that is the OR output is NOTed. So, a NOR gate is a combination of an OR Gate and a NOT Gate. It has two or more than two inputs and only one output. The Boolean expression for NOR gate is $Y = \overline{A + B}$

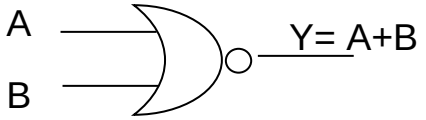
Logic symbol for two inputs NOR Gate and its truth table is shown below.

INPUTS		OUTPUT
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

From truth table it is observed that when both the inputs of NOR gates are logic 0 then the output is logic 1 otherwise output is 0.

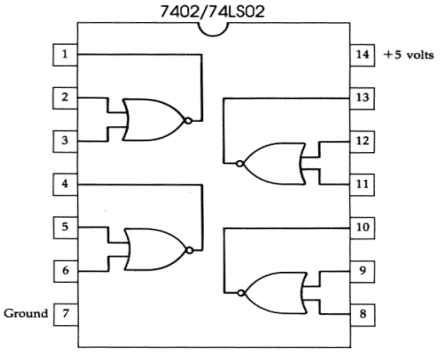
SWITCHING CIRCUIT:-





When both switches are open that is S1 = S2 = 0, current will conduct through the circuit. Hence lamp will glow that is Y = 1. When S1 = open and S2 = close, current will not conduct through lamp. Hence it will not glow that is Y = 0. When S2 = open and S1 = close, current will not conduct through lamp. Hence the lamp will Not glow that is Y= 0.When both switches are closed that is S1 = S2 = 1, no current will conduct through the lamp, Hence it will not glow that is Y = 0.

IC diagram for NOR Gate (IC 7402)



SPECIAL PURPOSE GATES:-

EXCLUSIVE-OR GATE (X-OR):-

It has two or more than two inputs and only one output. The Boolean expression for two input X-OR gate is given by $Y = A \oplus B = \bar{A} B + A \bar{B}$.

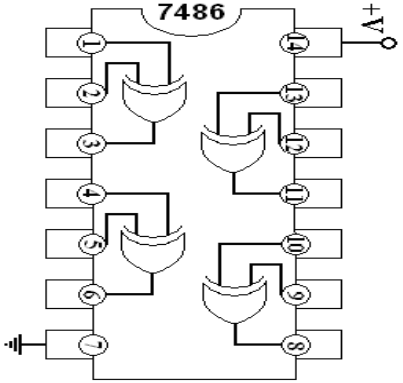
The logic symbol and truth table of X-OR gate is shown below.

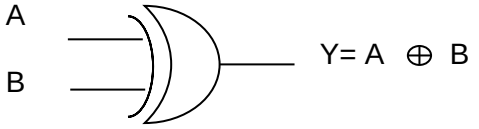
INPUTS		OUTPUT
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

From the truth table it is observed that, when both the inputs are equal, output is 0. The output is 1 when A is not equal to B.

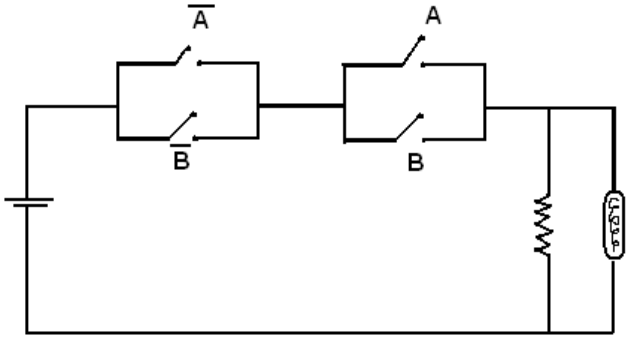
The name exclusive OR is derived from the fact that its output is a 1, only when exclusively one of its input is a 1.

The IC diagram of X-OR gate (IC 7486)





SWITCHING CIRCUIT:-



EXCLUSIVE-NOR GATE (X-NOR):-

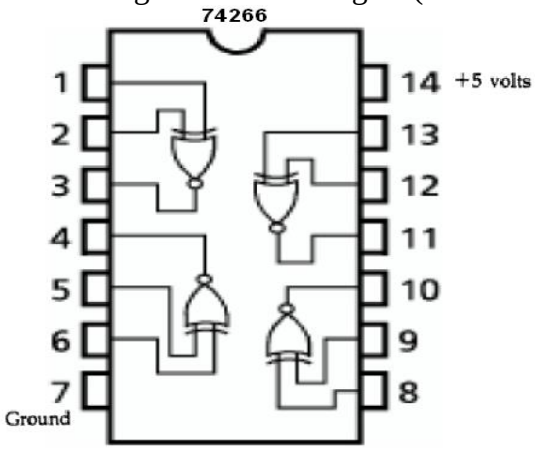
It has two or more than two inputs and only one output. The Boolean expression for two inputs X-NOR gate is given by $Y = A \overline{\oplus} B = \bar{A}\,\bar{B} + A\,B$.

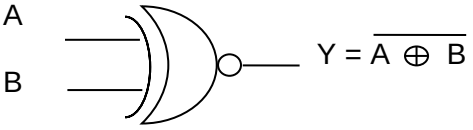
The logic symbol and truth table of X-NOR gate is shown below.

INPUTS		OUTPUT
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

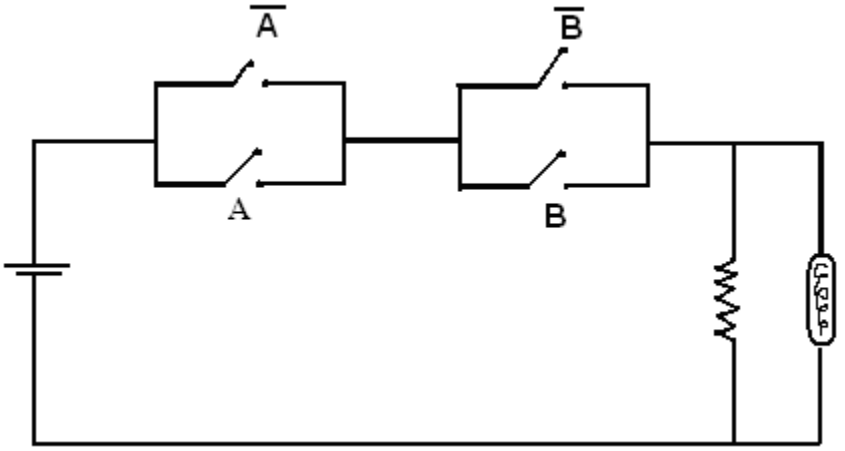
From the truth table it is observed that, when both the inputs are equal, output is 1. The output is 0 when A is not equal to B.

The IC diagram of X-NOR gate (IC 74266)





SWITCHING CIRCUIT:-



Q. 2) *Explain Laws of Boolean Algebra.*

Answer: In the modern mathematics of set theory and logic, George Boole introduced a new concept in 1854, which is known as Boolean algebra. Boolean algebra is a system of mathematical logic. It is an algebraic system consisting of the set of elements (0,1), two binary operators called OR and AND and one unary operator called NOT. In Boolean algebra, there are no fractions, decimals, negative numbers, square roots, cube roots etc. It is the basic mathematical tool in the analysis and synthesis of switching circuits. It is a way to express logic functions algebraically.

In Boolean algebra, every variable is called as a Boolean variable. It takes any one of the two different values, which are associated with two events. These two events can be recognized as TRUE or FALSE, YES or NO, ON or OFF. The Boolean algebras are governed by certain well-developed rules and laws.

AXIOMS AND LAWS OF BOOLEAN ALGEBRA

Axioms or *postulates* of Boolean algebra are a set of logical expressions that we accept without proof and upon which we can build a set of useful theorems. Each axiom can be interpreted as the outcome of an operation performed by a logic gate.

AND operation	**OR operation**	**NOT operation**
Axiom 1: 0.0 = 0	Axiom 5: 0+0 = 0	Axiom 9: $\overline{1} = 0$
Axiom 2: 0.1 = 0	Axiom 6: 0+1 = 1	Axiom 10: $\overline{0} = 1$
Axiom 3: 1.0 = 0	Axiom 7: 1+0 = 1	
Axiom 4: 1.1 = 1	Axiom 8: 1+1 = 1	

COMPLEMENTARY Laws

The term *complement* means to invert, i.e. to change 0s to 1s and 1s to 0s. The five laws of complementation are as follows:

Law 1: $\overline{0} = 1$

Law 2 : $\overline{1} = 0$

Law 3: If A = 0, Then $\overline{A} = 1$

Law 4: If $\overline{A} = 1$, Then $\overline{A} = 0$

Law 5: $\overline{\overline{A}} = A$ (double complementation law)

AND Laws

The four AND laws are as follows:

Law 1: $A \cdot 0 = 0$ (Null law)

Law 2: $A \cdot 1 = A$ (Identity law)

Law 3: $A \cdot \overline{A} = A$

Law 4: $A \cdot \overline{A} = 0$

OR Laws

The four OR laws are as follows:

Law 1: $A + 0 = A$ (Null law)

Law 2: $A + 1 = 1$ (Identity law)

Law 3: $A + \overline{A} = A$

Law 4: $A + \overline{A} = 1$

COMMUTATIVE Laws

Commutative laws allow change in position of AND or OR variables.

Law 1: A + B = B + A

This law states that, A OR B is the same as B OR A, i.e. the order in which the variables are ORed is immaterial. This means that it makes no difference which input of an OR gate is connected to A and which to B. We give below the truth tables illustrating this law.

A	B	A + B
0	0	0
0	1	1
1	0	1
1	1	1

=

B	A	B + A
0	0	0
0	1	1
1	0	1
1	1	1

This law can be extended to any number of variables. For example,

A+B+C = B+C+A = C+A+B = B+A+C

Law 2: **A . B = B . A**

This law states that A AND B is the same as B AND A, i.e. the order in which the variables are ANDed is immaterial. This means that it makes no difference which input of an AND gate is connected to A and which to B. The truth tables given below illustrate this law.

A	B	A . B
0	0	0
0	1	0
1	0	0
1	1	1

=

B	A	B . A
0	0	0
0	1	0
1	0	0
1	1	1

This law can be extended to any number of variables. For example,
A.B.C = B.C.A = C.A.B = B.A.C

ASSOCIATIVE Laws

The associative laws allow grouping of variables. There are two associative laws.

Law 1: **(A + B) + C = A + (B + C)**

A OR B ORed with C is the same as A ORed with B OR C. This law states that the way the variables are grouped and ORed is immaterial. The truth tables given next illustrate this law.

A	B	C	A +	**(A + B) +**
0	0	0	0	0
0	0	1	0	1
0	1	0	1	1
0	1	1	1	1
1	0	0	1	1
1	0	1	1	1
1	1	0	1	1
1	1	1	1	1

=

A	B	C	B + C	**A + (B +**
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	1	1
1	0	0	0	1
1	0	1	1	1
1	1	0	1	1
1	1	1	1	1

This law can be extended to any number of variables. For example,
A + (B + C + D) = (A + B + C) + D = (A + B) + (C + D)

Law 2: (A . B) . C = A . (B . C)

A AND B ANDed with C is the same as A ANDed with B AND C.

This law states that the way the variables are grouped and ANDed is immaterial. See the truth tables below:

A	B	C	A . B	**(A . B) .**
0	0	0	0	0
0	0	1	0	0
0	1	0	0	0
0	1	1	0	0
1	0	0	0	0
1	0	1	0	0
1	1	0	1	0
1	1	1	1	1

=

A	B	C	B . C	**A . (B .**
0	0	0	0	0
0	0	1	0	0
0	1	0	0	0
0	1	1	1	0
1	0	0	0	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

This law can be extended to any number of variables. For example,

A . (B . C . D) = (A . B . C) . D = (A . B) . (C . D)

DISTRIBUTIVE Laws

The distributive laws allow factoring or multiplying out of expressions. There are two distributive laws.

Law 1: **A (B + C) = AB + AC**

This law states that ORing of several variables and ANDing the result with a single variable is equivalent to ANDing that single variable with each of the several variables and then ORing the products. The truth table given below illustrates this law.

A	B	C	B + C	**A (B + C)**
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	1	0
1	0	0	0	0
1	0	1	1	1
1	1	0	1	1
1	1	1	1	1

=

A	B	C	AB	AC	**AB + AC**
0	0	0	0	0	0
0	0	1	0	0	0
0	1	0	0	0	0
0	1	1	0	0	0
1	0	0	0	0	0
1	0	1	0	1	1
1	1	0	1	1	1
1	1	1	1	1	1

This law applies to single variables as well as combination of variables. For example,

ABC(D+E) = ABCD + ABCE

AB(CD+EF) = ABCD + ABEF

Law 2: A + BC = (A + B) (A + C)

This law states that ANDing of several variables and ORing the result with a single variable is equivalent to ORing that single variable with each of the several variables and then ANDing the

sums. The truth table given below illustrates this law.

A	B	C	B C	**A + BC**
0	0	0	0	0
0	0	1	0	0
0	1	0	0	0
0	1	1	1	1
1	0	0	0	1
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

=

A	B	C	A + B	A +	**(A+B) (A+C)**
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	1	0	0
0	1	1	1	1	1
1	0	0	1	1	1
1	0	1	1	1	1
1	1	0	1	1	1
1	1	1	1	1	1

ABSORPTION Laws

There are four laws:

Law 1: A + A . B = A

This law states that ORing of a variable (A) with the AND of that variable (A) and another variable (B) is equal to that variable itself (A).

A	B	AB	**A + AB**
0	0	0	0
0	1	0	0
1	0	0	1
1	1	1	1

Algebraically, we have

$$A+A.B = A(1+B) = A.(1) = A$$

Law 2: **A (A + B) = A**

This law states that ANDing of a variable (A) with the OR of that variable (A) and another variable (B) is equal to that variable itself (A).

Algebraically, we have

A(A+B) = A.A+A.B = A+AB = A(1+B) = A.1 = A

A	B	A + B	**A(A + B)**
0	0	0	0
0	1	1	0
1	0	1	1
1	1	1	1

Law 3: $A + \overline{A} . B = A + B$

This law states that ORing of a variable with the AND of the complement of that variable with another variable, is equal to the ORing of the two variables.

A	B	$\bar{A}$.B	**$A + \bar{A}B$**	**A+B**
0	0	0	0	0
0	1	1	1	1
1	0	0	1	1
1	1	0	1	1

Algebraically, we have

$$A+\bar{A}.B = (A+\bar{A})\ (A+B) = 1.\ (A+B) = A+B$$

Law 4: **A (A + B) = AB**

This law states that ANDing of a variable with the OR of the complement of that variable with another variable is equal to the ANDing of the two variables.

Algebraically, we have

$$A(\bar{A}+B) = A.\bar{A}+A.B = 0+AB = AB$$

A	B	**$A(\bar{A} + B)$**	**AB**
0	0	0	0
0	1	0	0
1	0	0	0
1	1	1	1

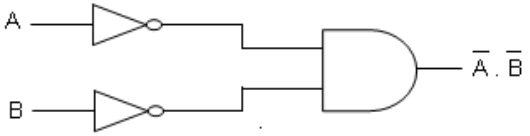
Q. 3) *State and prove Demorgan's theorem.*

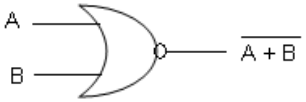
Ans: DE MORGAN'S FIRST THEOREM: -

This law states that the complement of a sum of variables is equal to the product of their individual complements. What it means is that the complement of two or more variables ORed together, is the same as the AND of the complements of each of the individual variables.

If the variables are A and B, then

$$\overline{A + B} = \overline{A} \cdot \overline{B}$$





A	B	A+B	L.H.S $\overline{A+B}$	$\overline{A}$	$\overline{B}$	R.H.S $\overline{A} \cdot \overline{B}$
0	0	0	1	1	1	1
0	1	1	0	1	0	0
1	0	1	0	0	1	0
1	1	1	0	0	0	0

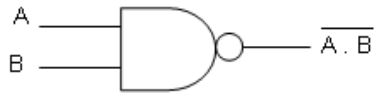
It shows that the NOR gate is equivalent to a bubbled AND gate. This has also been shown quite simply by truth tables.

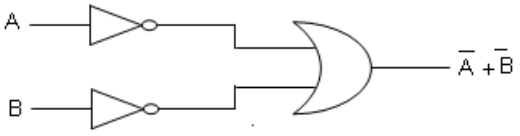
DE MORGAN'S SECOND THEOREM: -

This law states that the complement of the product of variables is equal to the sum of their individual complements. That is, the complement of two or more variables ANDed together, is equal to the sum of the complements of each of the individual variables.

If the variables are A and B, then

$$\overline{A.B} = \overline{A} + \overline{B}$$





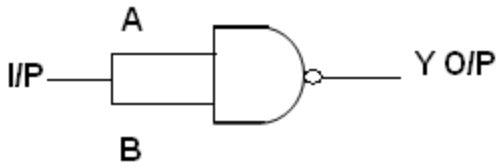
A	B	A.B	L.H.S	$\overline{A}$	$\overline{B}$	R.H.S
			$\overline{A.B}$			$\overline{A} + \overline{B}$
0	0	0	1	1	1	1
0	1	0	1	1	0	1
1	0	0	1	0	1	1
1	1	1	0	0	0	0

It shows that the NAND gate is equivalent to a bubbled OR gate. This has also been shown quite simply by truth table.

Q. 4) *Why NAND and NOR gates are universal Gate? Design all basic gates using Universal Gates.*
Ans: NOT gate using NAND gate
Fig. shows realization of NOT gate using NAND gate.As both the inputs of NAND are connected together we can write that,

Input, $A = B = A$.So output is given by,

$Y = A \cdot B = A \cdot A = A$

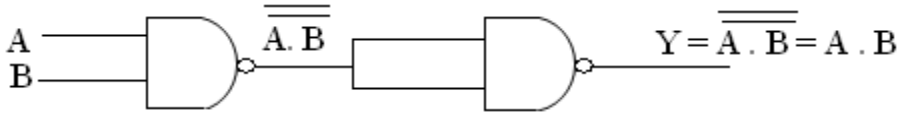


AND gate using NAND gate
Boolean expression for AND gate is

$Y = A \cdot B$

Taking double inversion, $Y = \overline{\overline{A \cdot B}}$

Above equation can be realize using NAND gate only.



OR gate using NAND gate

1) Boolean expression for OR gate is

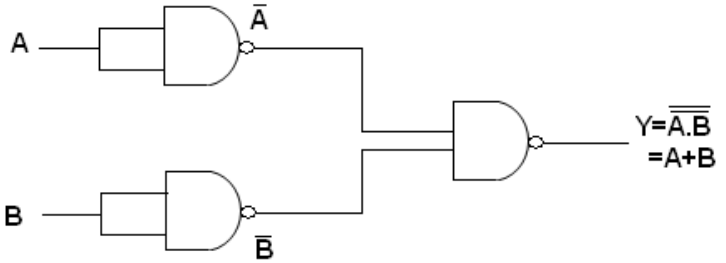
$$Y = A + B$$

Taking double inversion

$$Y = \overline{\overline{A + B}}$$

$$Y = \overline{A} \cdot \overline{B}$$

2) Above equation can be realize with NAND gate as follows



NOT gate using NOR gate

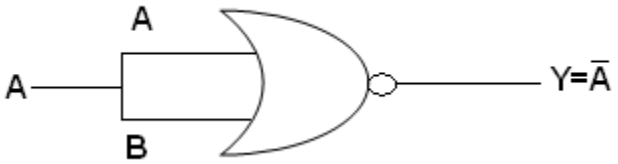
Figure shows realization of NOT gate using NOR gate. As both the inputs of NOR gate connected together,

$A = B = A$

So output of NOR gate is

$$Y = \overline{A + B} = \overline{A + A}$$

$$Y = \overline{A}$$



OR gate using NOR gate

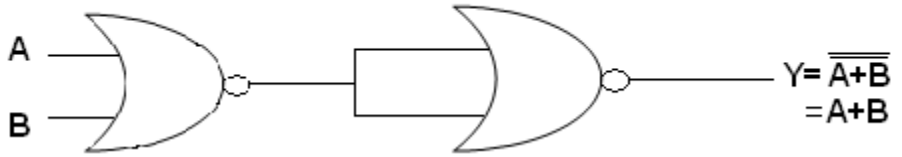
Boolean equation for OR gate is

$Y = A + B$

Taking double inversion

$= \overline{\overline{A + B}}$

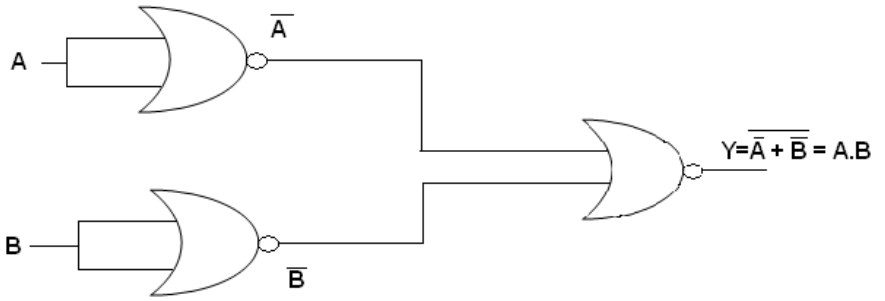
This is the required expression,



AND gate using NOR gate

Boolean equation for AND gate is

$Y = A \cdot B = \overline{A \cdot B} = \overline{\overline{A} + \overline{B}}$

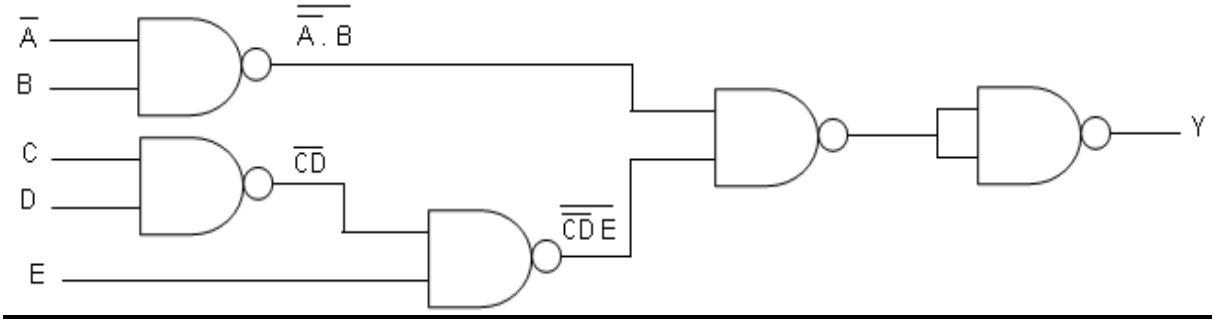


Q. 5) *Implement the function using only NAND gates: Y = (A + B'). (CD + E')*

Ans: To implement the expression using only NAND Gates the expression should be in terms of only product terms.

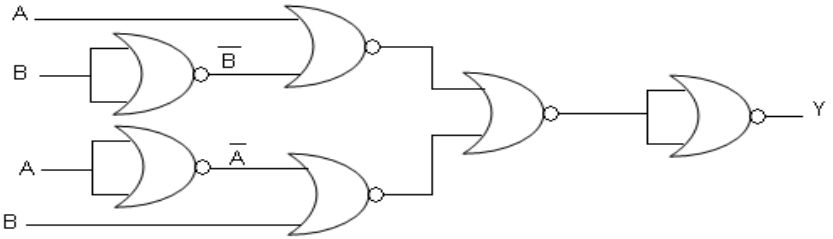
$Y = (A + B') \cdot (CD + E') = (A + B'')' \cdot (CD + E'')'$

$= (A'. B)' \cdot (CD' \cdot E)$

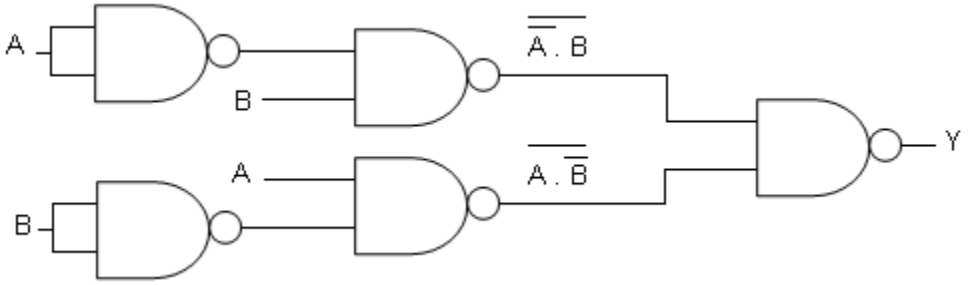


Q. 6) *Realize Ex-OR gate using NOR Gate*
Ans: A X-OR B = A.B' + A'B
To implement the expression using only NOR gates, the expression should have only sum terms.

= (A.B')'' + (A'B)''
= (A' + B)' + (A + B')'



Q.7) *Realize Ex-OR gate using NAND gate only.*
Answer:



Q. 8) *Simplify the following expression:*

A = XY + (XZ)' + XY'Z(XY + Z)

Ans: A = XY + (XZ)' + XXY'YZ + XY'ZZ --------- Distributive 1st law

= XY + (XZ)' + XY'Z --------- And law

= X(Y + Y'Z) + (XZ)'

= X(Y + Z) (Y + Y') + (XZ)' --------- Distributive 2nd law

= XY + XZ + (XZ)' --------- Or law

= XY + 1 ---------- Or law

= 1 ---------- Or law

Q. 9) *Reduce the expression*

F = (B+BC) (B+B'C) (B+D)

Ans: F = (B+BC) (B+B'C) (B+D)

= (B) (B+C) (B+D) ---------- Absorption law

= (B+BC) (B+D) ---------- AND law

= (B) (B+D) ---------- Absorption law

= B + BD ---------- AND law

= **B** ---------- Absorption law

Q. 10) *Reduce the expression*

$F = \overline{XY} + XYZ + \overline{X(Y + XY)}$

Ans: $F = \overline{X(\overline{Y} + YZ)} + XY + X\overline{Y}$ ---------- Distributive law

$= \overline{X(\overline{Y} + Z) + X(Y + \overline{Y})}$ ---------- Absorption law

$= \overline{X\overline{Y}} + XZ + X$ ---------- OR law

$= (X\overline{Y} + XZ) \cdot \overline{X}$ ---------- DeMorgan's First Theorem

= 0 ---------- AND law

Q. 11) *Show that (A + B) (A + BC) + A' . B' + A' . C' = 1*

Ans: LHS = (A + B) (A + BC) + A' . B' + A' . C'

= A + ABC + AB + BC + A' . B' + A' . C' ---------- Distributive law

= A(1 + BC + B) + BC + A' . B' + A' . C'

= A + BC + A' . B' + A' . C' ---------- OR law

= (A + A') (A + B') + BC + A' . C' ---------- Distributive law

= A + B' + BC + A' . C' ---------- OR law

= (A + A') (A + C') + (B' + B) (B' + C) ---------- Distributive law

= A + C' + B' + C' ---------- OR law

= 1 + A + B' ---------- OR law

= 1 ---------- OR law

Q. 12) *How to represent Logical Functions in Standard form?*

Answer: Boolean expressions are also known as logic expressions. Logical functions are expressed in terms of logical variables. The value assumed by logical variables is in binary form. The logical functions can be represented in two forms,

(i) Sum of Products (SOP) form

(ii) Product of Sum (POS) form

Product Term:

The AND function is referred to as a Product.The logic product of several variables on which function depends is considered to be a product term.The variable in product term can be appeared in complement/uncomplimentary form.

E.g. $Y = \overline{A}\,B\,C + A\,\overline{B}\,C + B\,C$

Each term is product term. Where A, B, C are literals.

Sum Term:

The OR function is referred to as a Sum.The logic sum of several variables on which function depends is considered to be a sum term.The variable in sum term can be appeared in complement/uncomplimentary form.

E.g. $Y = (\overline{A} + B + C) + (\overline{A} + \overline{C}) + (B + A)$

Each term is sum term & A, B, C are literals.

1) SUM OF PRODUCTS (SOP)

The *logical sum* of two or more logical *product terms* is called sum of products expression.It is basically an **OR** operation of **AND** operated variables.Each AND term consists of one or more variables appearing in either complemented or uncomplemented form.

e.g. Y = AB + $\underline{BC}$ + ABC, where Y is OR of three AND terms.
Y = AB + $\overline{BC}$, where Y is OR of two AND terms.

MINTERMS

A *product term* containing all the variables of a function in either complemented or uncomplemented form is called minterm.In the minterm, a variable appear either in *complemented* form, if it contains a value of 0 or in *uncomplemented* form, if it contains a value of 1.A 2 variable function has four possible combinations i.e., A'B', A'B, AB' & AB. These product terms are called minterms. For three binary inputs variables function there are 8 minterm, for 4 variable function 16 minterm, so on. The main property of minterm is that it possesses the value 1 for only one combination of 'k' input variables. That is for 'k' variables function of the 2^k of minterm, only 1 minterm will have the value 1, while remaining $[2^k - 1]$ minterm will have value 0.

- For ex. For input combination 010, only $\bar{A}B\bar{C}$ = 1, remaining 0.

A	B	C	MINTERMS
0	0	0	$\bar{A}\bar{B}\bar{C}$
0	0	1	$\bar{A}\bar{B}C$
0	1	0	$\bar{A}B\bar{C}$
0	1	1	$\bar{A}BC$
1	0	0	$A\bar{B}\bar{C}$
1	0	1	$A\bar{B}C$
1	1	0	$AB\bar{C}$
1	1	1	ABC

CANONICAL SOP EXPRESSION

- A logical expression is said to be in canonical/standard SOP form, if each product term consist of all the literals in complementary/uncomplimentary form.
- Standard SOP form, Y = A $\overline{B}$ $\overline{C}$ + A $\overline{B}$ C + A B C
  Each product term contain all the literals in complimentary/uncomplimentary form
- Non-canonical form, Y = AB + BC + AC (Each product term does not contain all the literals)

Conversion of a logical expression to Standard SOP

Step 1: For each term find the missing literals.

Step 2: Multiply the product term by $(X + \overline{X})$ for each literal X that is missing.

2) PRODUCTS OF SUM (POS)

- The *logical product* of two or more logical *sum terms* is called product of sum expression.
- It is basically an AND operation of OR operated variables.
- Each OR term consists of one or more variables appearing in either complemented or uncomplemented form.
- Ex. $Y = (\overline{A} + B + \overline{C}) . (\overline{A} + B + C)$ where Y is AND of two OR terms

MAXTERMS

A *Sum term* containing all the variables of a function in either complemented or uncomplemented form is called **maxterm**.In the maxterm, a variable appear either in *complemented* form, if it contains a value of 1 or in *uncomplemented* form, if it contains a value of 0.A 2 variable function has four possible combinations i.e., $(\overline{A}+\overline{B})$, $(A+\overline{B})$, $(\overline{A}+B)$ & $(A+B)$. These product terms are called maxterms. For three binary inputs variables function there are 8 maxterm, for 4 variable function 16 maxterm, so on. The main property of maxterm is that it possesses the value 0 for only one combination of 'k' input variables. That is for 'k' variables function of the 2^k of maxterm, only 1 maxterm will have the value 0, while remaining $[2^k – 1]$ maxterm will have value 1.

For ex. For input combination 010, only $A+\overline{B}+C = 0$, remaining 1.

A	B	C	MINTERMS
0	0	0	$A+B+C$
0	0	1	$A+B+\bar{C}$
0	1	0	$A+\bar{B}+C$
0	1	1	$A+\bar{B}+\bar{C}$
1	0	0	$\bar{A}+B+C$
1	0	1	$\bar{A}+B+\bar{C}$
1	1	0	$\bar{A}+\bar{B}+C$
1	1	1	$\bar{A}+\bar{B}+\bar{C}$

CANONICAL POS EXPRESSION

A logical expression is said to be in canonical/standard POS form, if each **sum term** consist of **all the literals** in complementary/uncomplimentary form.

Standard SOP form, **Y =** $(A \bar{+} B \bar{+} C) . (A \bar{+} B + C) . (A + B \bar{+} \bar{C})$

Each sum term contain all the literals in complimentary/uncomplimentary form

- Non-canonical form, **Y = (A+B) (B+C) (A+C)** (Each sum term does not contain all the literals)

Conversion of a logical expression to Standard POS

Step 1: For each term find the missing literals.

Step 2: Add $(X.\bar{X})$ to the sum term, for each literal X that is missing.

Q. 13) *Obtain the canonical SOP form of the function Y = A + BC*

Ans: Y = A + BC → Missing literal B & C

$Y = A(B + \bar{B})(C + \bar{C}) + BC(A + \bar{A})$

$= ABC + AB\bar{C} + A\bar{B}C + A\bar{B}\bar{C} + \bar{A}BC + \bar{A}\bar{B}C$

$= ABC + AB\bar{C} + A\bar{B}C + A\bar{B}\bar{C} + \bar{A}BC$

$= \sum m\,(7, 6, 5, 4, 3)$

Q. 14) *Obtain the canonical POS form of the function Y = A + BC*

Ans: Y = A + BC

The given equation is in SOP form.

So, first converting it into POS form, we get

Y = (A+B) (A+C) ---------- Distributive law

→ Missing literal B

→ Missing literal C

$Y = (A + B + C\bar{C})(A + C + B\bar{B})$

$= (A+B+C)(A+B+\bar{C})(A+\bar{B}+C)(A+\bar{B}+C)$

$= (A+B+C)(A+B+\bar{C})(A+\bar{B}+C)$

$= \Pi m\,(0, 1, 2)$

Q. 15) *Convert A(A+B) (A+B+C) into canonical SOP and POS form.*

Ans: The given expression is a 3-variable function in the POS form.

For Canonical SOP:

$A(\bar{A}+B)(\bar{A}+B+\bar{C})$

$A\bar{A}\bar{A} + A\bar{A}B + A\bar{A}\bar{C} + AB\bar{A} + ABB + AB\bar{C}$

$0 + 0 + 0 + 0 + A\bar{B} + AB\bar{C}$

$AB(C+\bar{C}) + AB\bar{C}$

$ABC + AB\bar{C} + AB\bar{C}$

$\sum m(7,6)$

For Canonical POS:

$=A(\bar{A}+B)\ (A+B+\bar{C})$

$=(A+\bar{B}B+CC)\ (\bar{A}+B+\bar{C}C)\ (\bar{A}+B+\bar{C})$

$=(A+\bar{B}B+\bar{C})\ (A+\bar{B}B+\bar{C})\ (A+B+C)\ (\bar{A}+B+\bar{C})\ (\bar{A}+B+\bar{C})$

$=(A+B+C)\ (A+\bar{B}+C)\ (A+B+\bar{C})\ (A+\bar{B}+\bar{C})\ (\bar{A}+B+C)\ (\bar{A}+B+\bar{C})\ (\bar{A}+B+\bar{C})$

$=(A+B+C)\ (A+\bar{B}+C)\ (A+B+\bar{C})\ (A+\bar{B}+\bar{C})\ (\bar{A}+B+C)\ (\bar{A}+B+\bar{C})$

$\Pi m(0,2,1,3,4,5)$

Q. 16) *What is combinational logic circuit?*

Ans: Logic circuits for digital systems may be combinational or sequential. The output of a combinational circuit depends on its present inputs only. Combinational circuits perform a specific information processing operation fully specified logically by a set of Boolean function. A combinational circuit consists of input variables, logic gates, and output variables. The logic gates accept signals from the inputs and generate signals to the outputs. This process transforms binary information from the given input data to the required output data. Obviously both input and output data are represented by signals, i.e. they exist in two possible values, one representing logic–1 and the other logic 0. The block diagram of combinational circuit is shown in fig. The n input binary variables come from an external source and the m output variables go to an external destination. For n input variables, there are 2^n possible combination of binary input values. For each possible input combination, there is one and only one possible output combination. A combinational circuit can be described by m Boolean functions one for each output variable. Each output function is expressed in terms of the n input variables. Usually the inputs come from flip flops and outputs go to flip flops. So both the variables and its compliment are assumed to be available.

Fig. The Block Diagram of Combinational Circuit

Q. 17) *Design Half Adder circuit.*

Answer: The simplest combinational circuit which performs the arithmetic addition of two binary digits is called a half-adder. As shown in fig., the half-adder has two inputs and two outputs. The two inputs are the two 1-bit numbers A and B, and the two outputs are the sum (S) of A and B and carry bit denoted by C. from the truth table of the half-adder shown in Table, one can understand that the sum output is 1 when either of the inputs (A or B) is 1, and the carry output is 1 when both the inputs (A or B) are 1.

Inputs		Outputs	
Augend A	Added B	Sum S	Carry C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

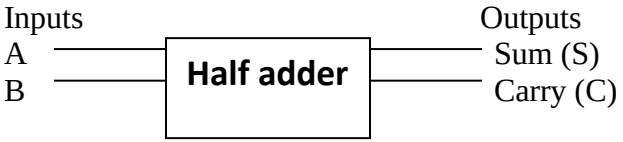


Fig. Logic Symbol

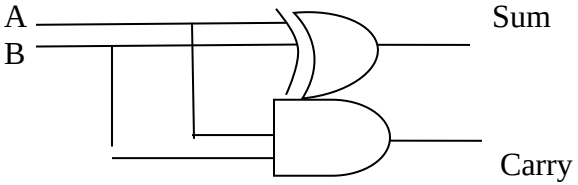


Fig. Logic Diagram

From Table, the logic expression for the Sum output can be written as a Sum of Product expression by summing up the input combination for which the sum is equal to 1. In the truth table, the sum

output is 1 when AB = $0\overline{1}$ and A$\overline{B}$ = 10. Therefore, the expression for sum is

$$S = \overline{A}\,B + A\,\overline{B}$$

Now, this expression can be simplified as

$$S = A \oplus B$$

Similarly, the logic expression for Carry output can be expressed as a Sum of Product expression by summing up the input combinations for which the carry is equal to 1. In truth table, the carry is 1 when AB = 11. Therefore,

$$C = AB$$

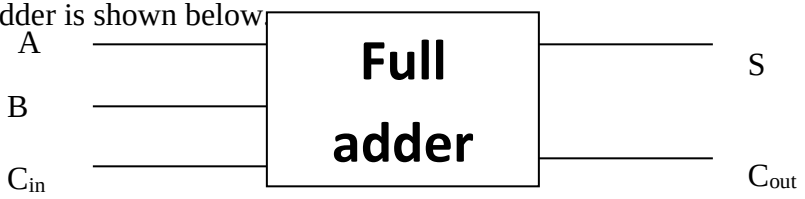
Q. 18) *Design Full Adder using Logic gates*.

Ans: FULL ADDER

A half adder has only two inputs and there is no provision to add a carry coming from the lower order bits when multibit addition is performed. For this purpose, a full adder is designed. A full adder is a combinational circuit that performs the arithmetic sum of three input bits and produces a sum output and a carry.

Design Steps:

1. The full-adder has three inputs and two outputs. The three inputs are the two 1-bit numbers A, B, and carry-in C_{in} and the two outputs are the sum (S) and carry bit denoted by C_{out}. The block diagram of the full-adder is shown below.



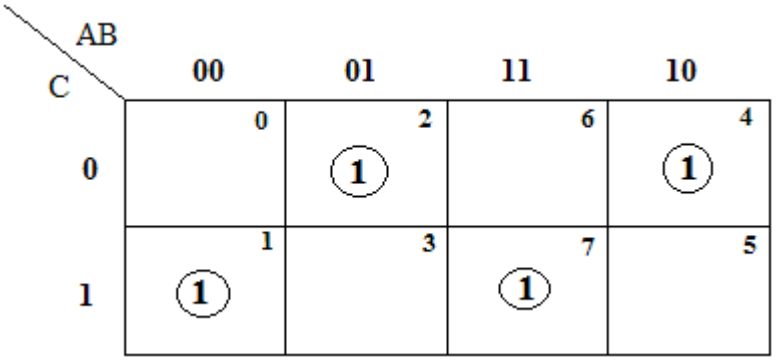
2. The truth table for the full-adder circuit is shown in Table. The binary variable S gives the value of the LSB of the sum, and the binary variable C_{out}, gives the output carry.

Inputs			Outputs	
Augend A	Addend B	Carry input C_{in}	Sum S	Carry C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

As shown in Table, there are eight possible input combinations for the three inputs and for each case the S and C_{out} values are listed. When all the bits are 0s, the output is 0. The S output is equal to 1 when only 1 input is equal to 1 or when all the inputs are equal to 1. The C_{out} has a carry of 1 if two or three inputs are equal to 1.

3. The switching expression for sum and carry can be derived by using K-map,

Sum (S) = Σm (1,2,4,7)

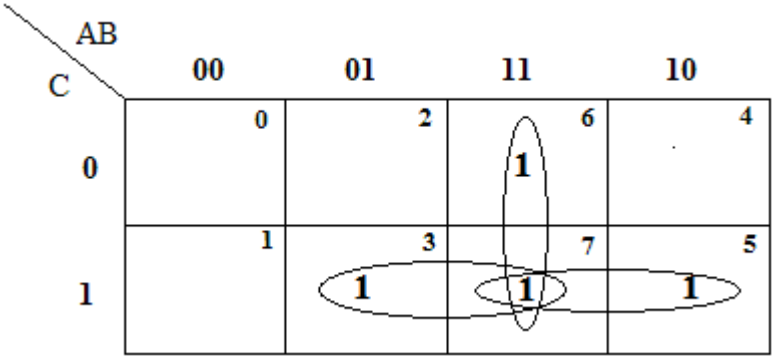


$S = \bar{A}.\bar{B}.C_{in} + \bar{A}.B.\bar{C}_{in} + A.\bar{B}.\bar{C}_{in} + A.B.C_{in}$

$= \bar{A}(\bar{B}.C_{in} + B.\bar{C}_{in}) + A(\bar{B}.\bar{C}_{in} + B.C_{in})$

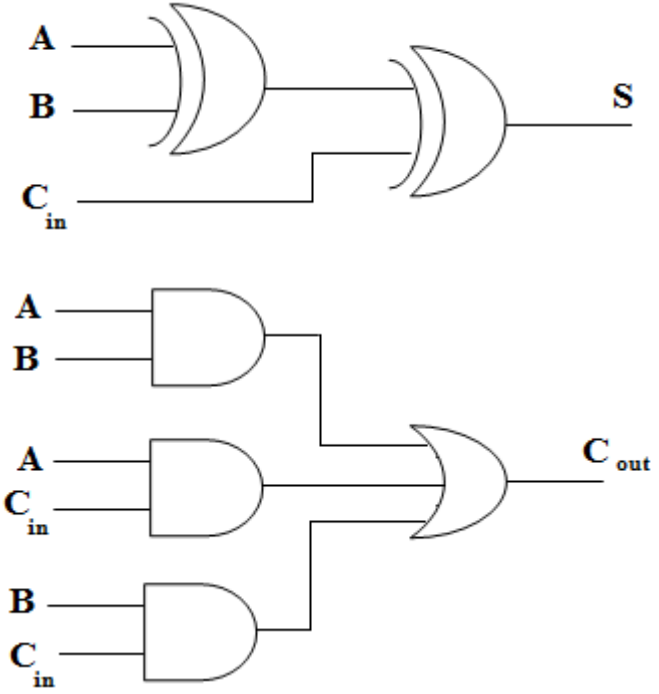
$= (A \oplus B \oplus C_{in})$

Carry (C_{out}) = Σm (3,5,6,7)

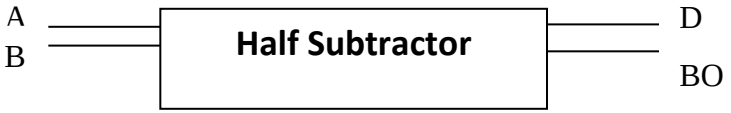


$$C_{out} = AB + BC_{in} + AC_{in}$$

4. The Sum term of the full-adder is the X-OR of A, B, and C_{in}, i.e. the sum bit is the modulo sum of the data bits in that column and the carry from the previous column. The logic diagram of the full-adder using two X-OR gates and the two AND gates and one OR gate is shown in fig.



Q. 19) *Design Half Subtractor using Logic gates.*
Ans: HALF SUBTRACTOR
The half-subtractor is a combinational circuit which is used to perform subtraction of two bits.
Design Steps:
1. The half-subtractor has two inputs and two outputs. The two inputs are the two 1-bit numbers A and B, and the two outputs are the difference (D) of A and B and borrow bit denoted by BO. The block diagram of half-subtractor is shown below.



2. The truth table of the half-subtractor is shown in the table.

Inputs		**Outputs**	
Mineund A	**Subtrahend B**	**Difference D**	**Borrow BO**
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

From the truth table of the half-subtractor, it is clear that the difference output is 0 if A = B and 1 if A ≠ B; the borrow output BO is 1 whenever A < B. if A is less than B, then subtraction is done by borrowing 1 from the next higher order bit.
3. From Table, the logic expression for the difference output can be written as a Sum of Product (SOP) expression by summing up the input combination for which the difference is equal to 1. In the truth table, the difference output is 1 when AB = 01 and AB = 10. Therefore, the expression for the difference is

$$D = \overline{A}\,B + A\,\overline{B}$$

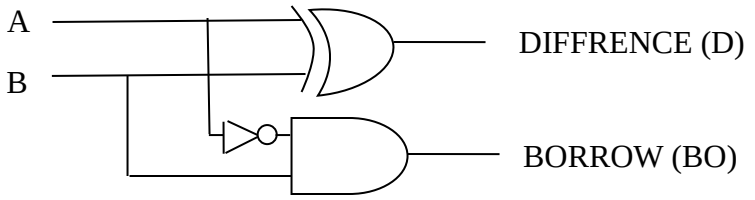
Now, this expression can be simplified as

$$D = A \oplus B$$

Similarly, the logic expression for Borrow output can be expressed as a SOP expression by summing up the input combinations for which the borrow is equal to 1. In truth table, the borrow is 1 when AB = 01. Therefore,

$C = \bar{A}.B$

4. A half-subtractor can, therefore, be realized by using one X-OR, one AND gate and one NOT gate as shown in fig.



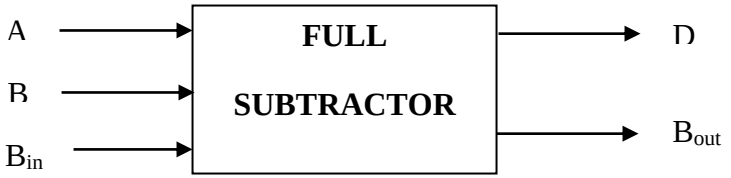
Q. 20) *Design Full Subtractor using Logic gates.*

Ans.: FULL SUBTRACTOR

The half-subtractor can be used only for LSB subtraction. If there is a borrow during the subtraction of the LSBs, it affects the subtraction in the next higher column; the subtrahend bit is subtracted from the minuend bit, considering the borrow from that column used for the subtraction in the preceding column. Such a subtraction is performed by a full-subtractor.

Design steps

1. It has three inputs, A (minuend), B (subtrahend) and B_{in} (borrow from previous stage), and two outputs D (difference) and B_{out} (borrow out). The block diagram of full Subtractor is shown below.



2. The truth table of full Subtractor is shown below.

The binary variable D gives the value of the LSB of the difference, and the binary variable B_{out}, gives the output borrow. As shown in table, there are eight possible input combinations for the three inputs and for each case the D and B_{out} values are listed. When all the bits are 0s, the output is 0. The D output is equal to 1 when only 1 input is equal to 1 or when all the inputs are equal to 1.

Inputs			Outputs	
Minuend A	**Subtrahend B**	**Borrow in B_{in}**	**Difference D**	**Borrow out B_{out}**
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

3. From table, the Sum of Product expression for the difference (D) output can be written as:

$$D = \overline{A}\,\overline{B}\,B_{in} + \overline{A}\,B\,\overline{B}_{in} + A\,\overline{B}\,\overline{B}_{in} + A\,B\,B_{in}$$

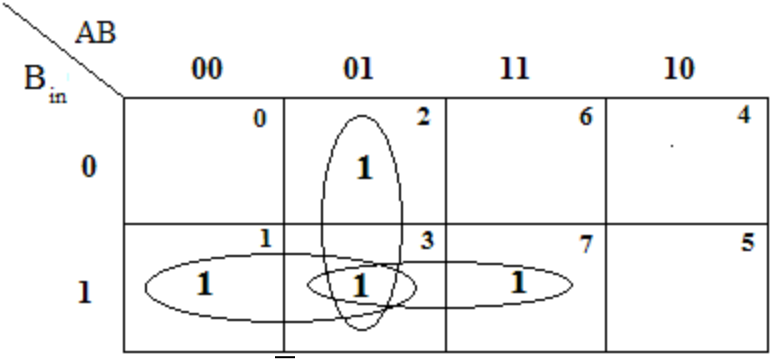
$$D = \overline{A}\,(\overline{B}\,B_{in} + B\,\overline{B}_{in}) + A\,(\overline{B}\,B_{in} + B\,\overline{B}_{in})$$

$$= (B \oplus B_{in})\,\overline{A} + (B \oplus B_{in})\,A$$

$$D = A \oplus B \oplus B_{in}$$

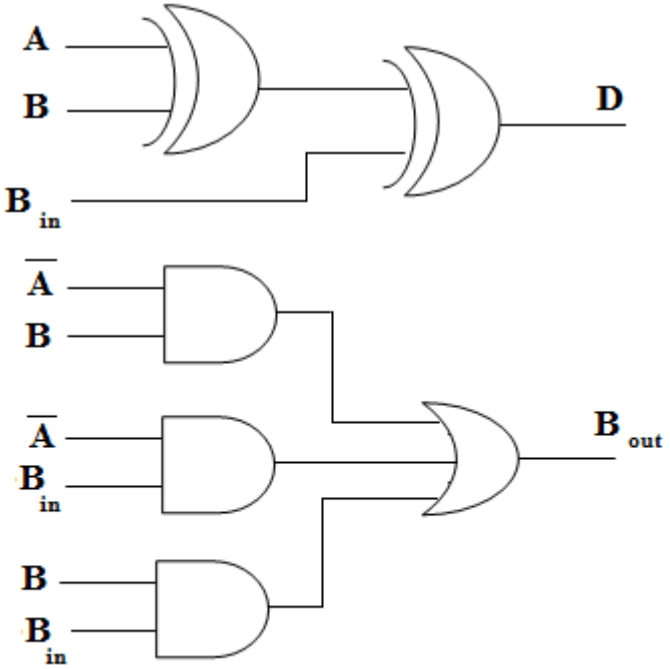
Similarly, the sum of product expression for B_{out} can be written from the truth table as:

$$\text{Borrow } (B_{out}) = \Sigma m\,(1,2,3,7)$$

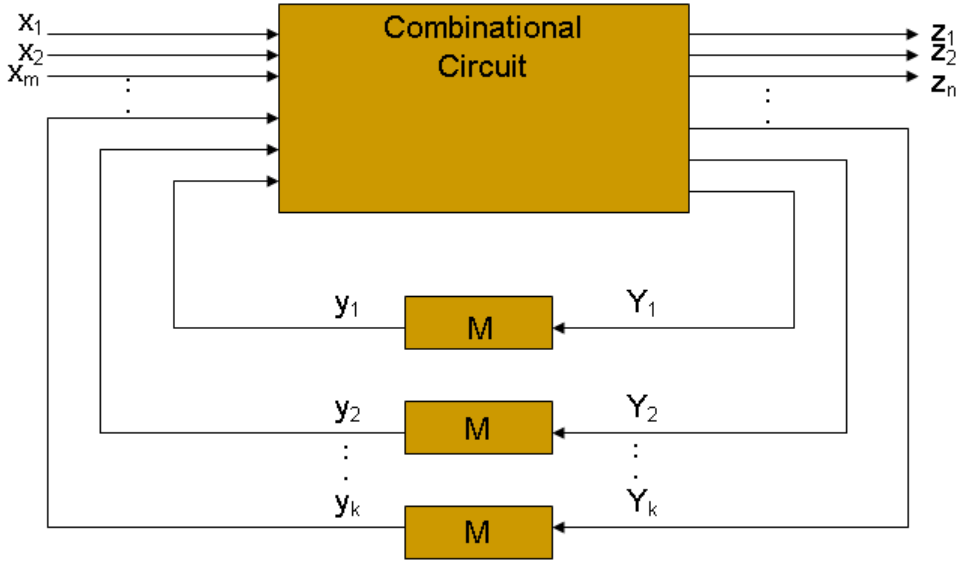


$$B_{out} = \overline{A}\,B + A\,B_{in} + B\,B_{in}$$

4. The Difference term of the full-subtractor is the X-OR of A, B, and B_{in}, i.e. the difference bit is the modulo difference of the data bits in that column and the borrow from the previous column. The logic diagram of the full-subtractor using two X-OR gates, two AND gates, one NOT gate and one OR gate is shown in fig.



Q. 21) *What is sequential logic circuit?*
Ans: SEQUENTIAL LOGIC DESIGN
Sequential circuits are the one, whose output levels at any instant of time are dependant not only on the present input but also on the past input and output. It requires the past history of inputs to know the output of the system. The Past history is provided by *feedback* from the output back to the input. It means that sequential circuits have memory. Hence it is made of Combinational circuits and memory elements. It follows time sequence in addition to a proper combination of inputs for operation of a system. Examples are FlipFlops, Registers, Counters etc.



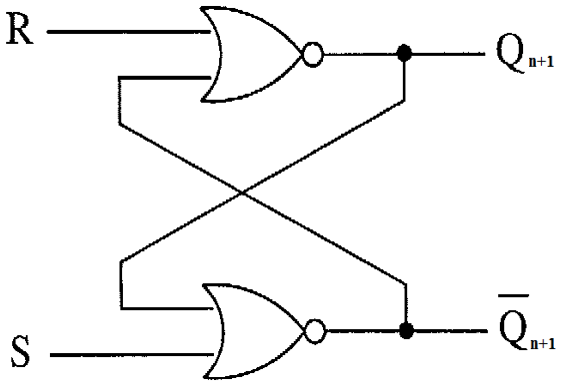
M = Memory elements
$X_1, X_2, \ldots X_m$ = Data inputs
$Z_1, Z_2, \ldots Z_n$ = Data outputs
$y_1, y_2, \ldots y_k$ = Present states
$Y_1, Y_2, \ldots Y_k$ = Next states

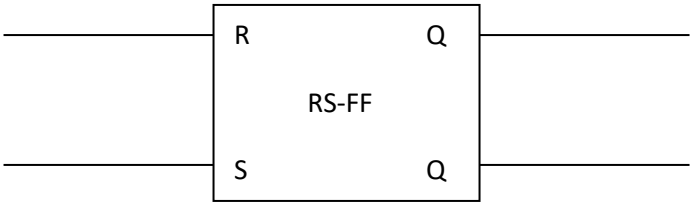
The information stored in the memory element at any given interval of time defines the present state of the sequential circuit. The present state and the external inputs determine the outputs and the next state of the sequential circuits. Thus, sequential circuit is a sequence of external inputs (present state and next state) and outputs. We will use suffix ***n*** for present state and ***n+1*** for next state.

Q. 22) *Compare Combinational Logic Circuit with Sequential logic Circuit.*
Answer:

Combinational Circuits	**Sequential Circuits**
1. In combinational circuits, the output variables at any instant of time are dependent only on the present input variables.	1. In sequential circuits, the output variables at any instant of time are dependent not only on present input, but also on the past state of the system.
2. The memory unit is not required.	2. The memory unit is required to store the past history of the input variables.
3. It is faster than sequential circuit.	3. It is slower than combinational circuit.
4. Combinational circuits are easy to design.	4. Sequential circuits are comparatively harder to design.
5. Adder, Subtractors, Encoders, Decoders, Code converters etc. are examples of combinational circuits.	5. Counters, Shift registers, Serial Adders, Sequence generators, Logic function generators, are example of sequential circuits.

Q.23) *Explain S-R Latch using NAND and NOR gate.*
Answer: 1) Using NOR Gates (Active High Latch)
Circuit diagram
Here, two NOR gates are connected back to back. The feedback connection is provided. The output of each gate is connected to one of the inputs of the other gate.





Logic Symbol

Truth Table

Inputs			Output	Action
S	**R**	**Q_n**	**Q_{n+1}**	
0	0	0	**0**	No Change
0	0	1	**1**	
0	1	0	**0**	Reset
0	1	1	**0**	
1	0	0	**1**	Set
1	0	1	**1**	
1	1	0	**?**	Forbidden
1	1	1	**?**	

1. S = 0, R = 0

This is the normal resting state of the NOR latch and it has no effect on the output state. Q_{n+1} will remain in the same state in which it was, prior to the application of inputs. This condition is called as NO CHANGE condition.

2. S = 0, R = 1

This will always reset $Q_{n+1} = 0$, where it will remain even after RESET turns to 0.

3. S = 1, R = 0

This will always set $Q_{n+1} = 1$, where it will remain even after SET returns to 0.

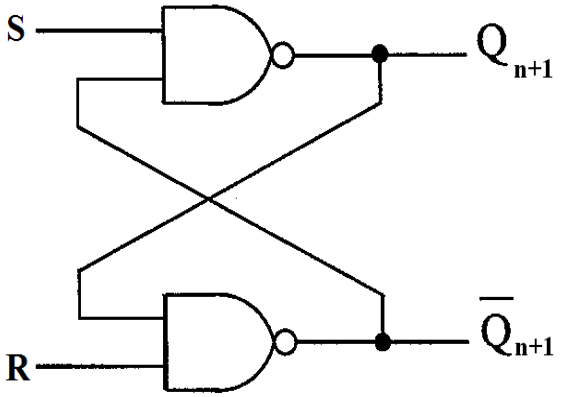
4. S = 1, R = 1

The output is unpredictable, i.e. both Q_{n+1} and Q_{n+1}' may be HIGH, or both may be LOW or any one of them may be HIGH and the other LOW. This condition is described as invalid or forbidden condition.

2) Using NAND Gates (Active Low Latch)

Circuit diagram

Here, two NAND gates are connected back to back. The feedback connection is provided. The output of each gate is connected to one of the inputs of the other gate.



Logic Symbol

Truth Table

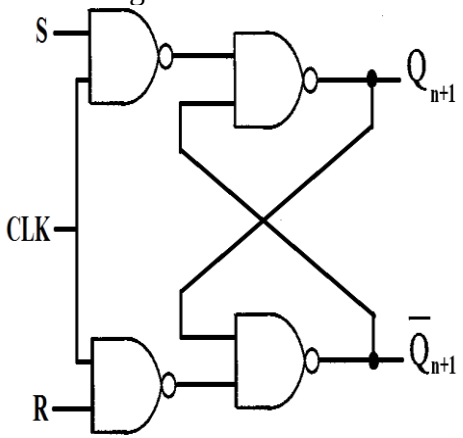
Inputs			Output	Action
S	**R**	**Q_n**	**Q_{n+1}**	
0	0	0	**?**	Forbidden
0	0	1	**?**	
0	1	0	**1**	Set
0	1	1	**1**	
1	0	0	**0**	Reset
1	0	1	**0**	
1	1	0	**0**	No Change
1	1	1	**1**	

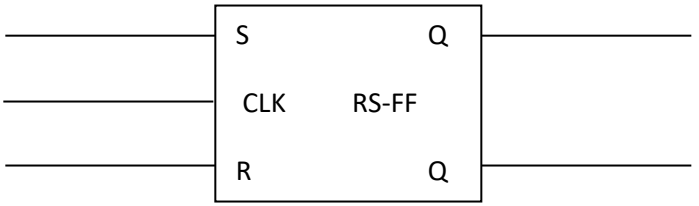
1. S = 0, R = 0
The output is unpredictable, i.e. both Q_{n+1} and Q_{n+1}' may be HIGH, or both may be LOW or any one of them may be HIGH and the other LOW. This condition is described as invalid or forbidden condition.
2. S = 0, R = 1
This will always set $Q_{n+1} = 1$, where it will remain even after SET returns to 0.
3. S = 1, R = 0
This will always reset $Q_{n+1} = 0$, where it will remain even after RESET turns to 0.
4. S = 1, R = 1
This is the normal resting state of the NOR latch and it has no effect on the output state. Q_{n+1} will remain in the same state in which it was, prior to the application of inputs. This condition is called as NO CHANGE condition.

Q.24) *Design S-R Flip-flop using NAND gates only.*

S – R FLIP-FLOP (SET-RESET)
The simplest type of flip-flop is called an S-R FF. It has two inputs S (set) and R (reset) and two outputs Q_{n+1} and Q_{n+1}'.A clocked S-R FF requires an extra control input called 'CLOCK (CLK)' input. Its S and R inputs will control the state of the flip-flop only when the CLOCK is HIGH.
When CLOCK is LOW, the inputs become ineffective and no change of state can takes place.

Circuit diagram





Logic Symbol

Truth Table

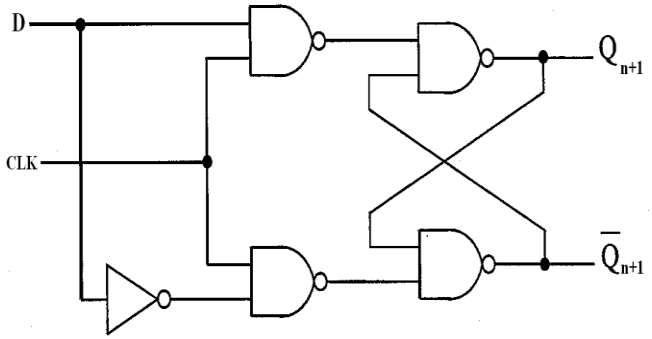
Inputs				Output	Action
CLK	**S**	**R**	**Q_n**	**Q_{n+1}**	
0	0	0	0	**0**	No Change
0	0	0	1	**1**	
0	0	1	0	**0**	No Change
0	0	1	1	**1**	
0	1	0	0	**0**	No Change
0	1	0	1	**1**	
0	1	1	0	**0**	No Change
0	1	1	1	**1**	
1	0	0	0	**0**	No Change
1	0	0	1	**1**	
1	0	1	0	**0**	Reset
1	0	1	1	**0**	
1	1	0	0	**1**	Set
1	1	0	1	**1**	
1	1	1	0	**?**	Forbidden
1	1	1	1	**?**	

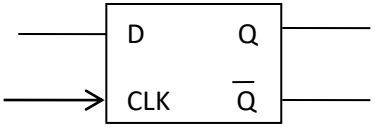
S = 0, R = 0, This is the normal resting state and it has no effect on the output state. Q_{n+1} will remain in the same state in which it was, prior to the application of inputs. This condition is called as NO CHANGE condition.
S = 0, R = 1, This will always reset $Q_{n+1} = 0$, where it will remain even after RESET turns to 0.
S = 1, R = 0, This will always set $Q_{n+1} = 1$, where it will remain even after SET returns to 0.
S = 1, R = 1, The output is unpredictable, i.e. both Q_{n+1} and Q_{n+1}' may be HIGH, or both may be LOW or any one of them may be HIGH and the other LOW. This condition is described as invalid or forbidden condition.

Q. 25) *Design D Flip-flop using NAND gates only.*
Ans: D FLIP-FLOP (Delay)
In many applications, it is not necessary to have separate S and R inputs to a latch. If the input combinations S = R = 0 and S = R = 1 are never needed, the S and R are always the complement of

each other. This FF has only one input referred as data input. In this FF, input data appears at output at the end of clock pulse. This means that transfer of data from input to output is delayed and hence the name D-FF. The D flip-flop has only one input called the Delay (D) input and two outputs Q_{n+1} and Q_{n+1}'. It can be constructed from S-R flip-flop by inserting an *inverter* in between S and R and assigning the symbol D to the S input.

Circuit Diagram





Truth Table

Inputs			Output	Action
CLK	**D**	**Q_n**	**Q_{n+1}**	
0	0	0	**0**	No Change
0	0	1	**1**	
0	1	0	**0**	No Change
0	1	1	**1**	
1	0	0	**0**	Reset
1	0	1	**0**	
1	1	0	**1**	Set
1	1	1	**1**	

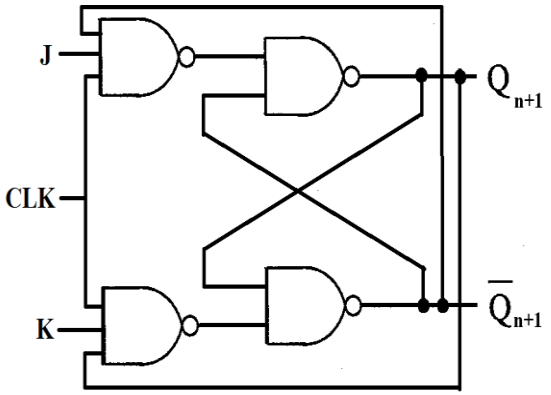
When the CLK input is LOW, the D input has no effect, since the set and reset inputs of the NAND flip-flop are kept HIGH. When the CLK goes HIGH, the Q_{n+1} output will take on the value of the D input.

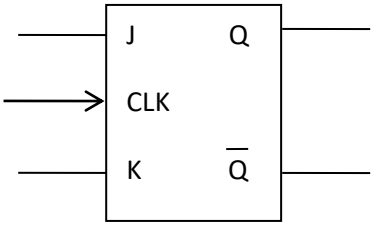
Q. 26) *Design J-K Flip-flop using NAND gates only.*

Ans: J - K FLIP-FLOP (Jack Kilby)

The J-K FF is very versatile and also the most widely used. The functioning of the J-K FF is identical to that of the S-R FF, except that it has no invalid states. Inputs J and K behave like the inputs S and R respectively, to SET and RESET the circuits. The forbidden condition is not occurred in J-K FF. It can be constructed from S-R FF by assigning J to S input and K to R input. To remove forbidden condition, another feedback connection is provided. Output Q_{n+1} is connected back to input of first NAND gate and output Q_{n+1}' is connected back to input of second NAND gate.

Circuit Diagram





Truth Table

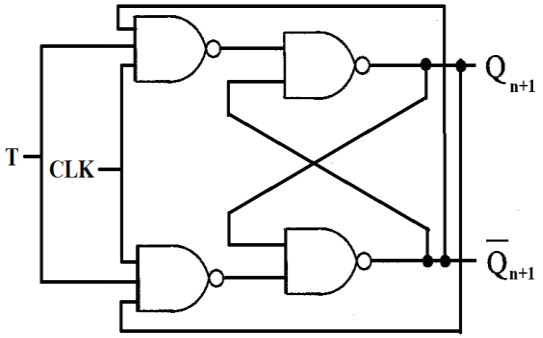
Inputs				Output	Action
CLK	**J**	**K**	**Q_n**	**Q_{n+1}**	
0	0	0	0	**0**	No Change
0	0	0	1	**1**	
0	0	1	0	**0**	No Change
0	0	1	1	**1**	
0	1	0	0	**0**	No Change
0	1	0	1	**1**	
0	1	1	0	**0**	No Change
0	1	1	1	**1**	
1	0	0	0	**0**	No Change
1	0	0	1	**1**	

1	0	1	0	**0**	Reset
1	0	1	1	**0**	
1	1	0	0	**1**	Set
1	1	0	1	**1**	
1	1	1	0	**1**	Toggle
1	1	1	1	**0**	

When J = K = 0, no change of states take place even if a clock pulse is applied.
When J = 0 and K = 1, the flip-flop resets at the end of clock pulse.
When J = 1 and K = 0, the flip-flop sets at the end of clock pulse.
When J = K = 1, the flip-flop toggles, i.e. next state will be complement of present states ($Q_{n+1} = Q_n'$) at the end of clock pulse.

Q. 27) *Design T Flip-flop using NAND gates only.*
Ans: T FLIP-FLOP (Toggle)
A T-FF has a single control input, labeled T for toggle. The T-type flip-flop is obtained from a J-K flip-flop by connecting its J and K inputs together. The designation T comes from the ability of the flip-flop to "toggle" or complement its state. When T is HIGH, the FF toggles on every new clock pulse. When T is low, the FF remains in whatever state it was before.

Circuit Diagram:



Truth Table:

Inputs			Output	Action
CLK	**T**	**Q_n**	**Q_{n+1}**	
0	0	0	**0**	No Change
0	0	1	**1**	
0	1	0	**0**	No Change
0	1	1	**1**	
1	0	0	**0**	No Change
1	0	1	**1**	
1	1	0	**1**	Toggle
1	1	1	**0**	

When the T input is in the 0 state (i.e. J=K=0) prior to a clock pulse, the Q output will not change with clocking. When the T input is at a 1(i.e. J=K=1) level prior to clocking, the output will be in the Q state after clocking. In other words, if the T input is a logical 1 and the device is clocked, the output will change state regardless of what output was prior to clocking. This is called toggling hence the name T flip-flop.

Reference:

"Modern Digital Electronics" by R. P. Jain, 4th Edition, McGraw Hill Education Private Limited, published in 2015

UNIT NO. 3

Unit III: **Electronic Devices and its Applications**
Introduction, operation and Characteristics of Diode, BJT and FET, Application of Diode as a Rectifier, BJT as a Switch and Amplifier.

Q. 1) *Explain energy band theory.*
Answer: The smallest element of a particle is known as atom. Atom consists of positive protons, negative electrons and neutrons. The number of electrons is equal to the number of protons whereas the mass of electron is 1/1840 of mass of protons.Number of electrons = number of protons = Atomic number.Atom consists of nucleus which contains protons and electrons revolved around nucleus in the form of shell (orbit). The number of electrons present in each shell is given by the formula $2n^2$, where n= number of shell.Consider a Silicon atom which consists of 14 protons and 14 electrons. Its first shell consist of 2 electrons while the second shell consist of maximum capacity i.e. 8 electrons. The remaining 4 electrons are in the last i.e. outermost shell. The 4 electrons located in the farthest shell which are loosely held by the nucleus and hence are called *valence electrons*.

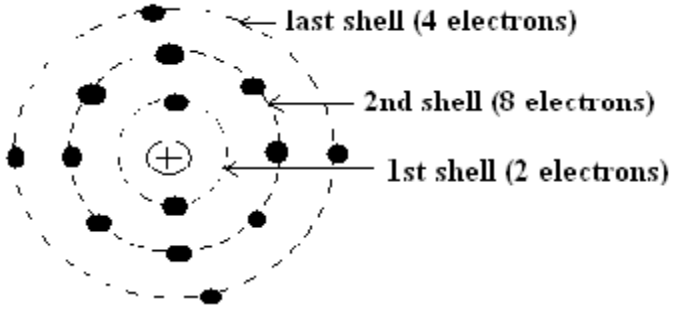


Figure 1: Silicon Atom
We have seen that every shell is associated with an **energy level**. An electron orbiting very close to the nucleus in the first shell is very much tightly bound to the nucleus and possesses only a small amount of energy. Hence first shell has lowest energy level. Greater the distance of an electron from the nucleus, the greater is its energy. Hence the energy level of the outermost shell is highest. Due to such high energy, the valence electrons in the outermost shell can be easily extracted out and hence such electrons take part in chemical reactions and in bonding the atoms together. Now this discussion is related to the electrons and shells of one isolated atom only.

In solid, atoms are brought close together. In such a case, outer shell electrons are shared by more than one atom. So these electrons come under the influence of forces from other atoms too. The

valence electrons are shared by forming a bond with the valence electrons of an adjacent atom. Such bonds are called **covalent bonds**. Thus the valence electrons are not free under normal conditions, as they are shared by the adjacent atoms. Now the valence electrons possess highest energy level. When such electrons form the covalent bonds due to the coupling between the valence electrons, the energy levels associated with the valence electrons merge into each other. This merging forms an *energy band*.

Out of all the energy bands, three bands are most important to understand the behavior of solids. These bands are,

1) Valence band, 2) Conduction band, 3) Forbidden band or gap

The energy band formed due to merging of energy levels associated with the *valence electrons* i.e. electrons in the last shell is called **valence band**.

The energy band formed due to merging of energy levels associated with the *free electrons* is called **conduction band**.

Under normal condition, the conduction band is empty and once energy is imparted, the valence electrons jump from valence band to conduction band and become free electron. While jumping from valence band, the electrons have to cross an energy gap.

This energy gap which is present separating the conduction band and the valence band is called **forbidden band** or **forbidden gap**.

The energy imparted to the electrons must be greater than the energy associated with the forbidden gap, to extract the electrons from valence band and transfer them to conduction band. The energy associated to forbidden band is denoted as $\mathbf{E_G}$. The electrons cannot exist in the forbidden gap.

The graphically representation of the energy bands in a solid is called energy band diagram.

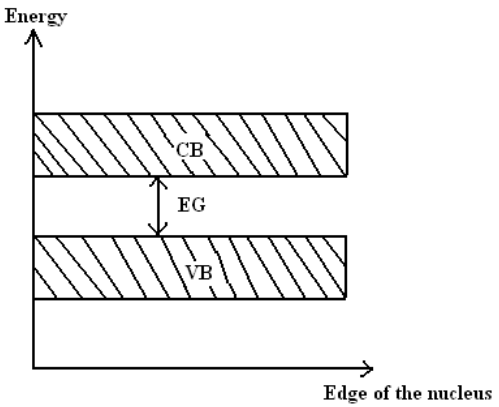


Figure 2: Energy Band Diagram

The electrons in various orbits revolving around the nucleus occupy a various band including fully or partly occupied valence band. The conduction band which is normally empty carries the electrons which get drifted from valence band. These electrons present in the conduction band are free electrons and they drift about in the spaces between the atoms.

Q. 2) *Explain types of Materials with energy band diagram.*

Answer: Based on the ability of various materials to conduct current, the materials are classified as conductors, insulators and the semiconductors.

CONDUCTORS

A material which is very good carriers of electricity is called **conductor**.The copper and aluminum are the good examples of a conductor.

A material having large number of free electrons can conduct very easily. For example, copper has $8.5 * 10^{28}$ free electrons per cubic meter, which is a very large number. Hence copper is good conductor. In fact, in the metals like copper, aluminium, there is *no forbidden gap* between valence band and conduction band. The two bands *overlap*. Hence even at room temperature (300° K), a large number of electrons are available for conduction. So without any additional energy such metals contain a large number of free electrons and hence called good conductors. An energy band diagram for a conductor is shown in the fig.

INSULATORS

A very poor conductor of electricity is termed as **insulator**. The glass, wood, mica, diamonds are the examples of an insulator which does not conduct current.

An insulator has an energy band diagram as shown in the fig.The *forbidden gap is very wide*, approximately of about 7 eV is present in insulators. For a diamond, which is insulator, the forbidden gap is about 6 eV. In case of such insulating material, it is impossible for an electron to jump from the valence band to conduction band. Hence such material cannot conduct and called insulators. Such materials may conduct only at very high temperature or if they are subjected to high voltage. Such conduction is rare and is called breakdown of an insulator.

SEMICONDUCTORS

A metal having conductivity in between conductor and an insulator is called **semiconductor**.

The silicon and germanium are the examples of a semiconductor which does not conducts current at low temperatures but as temperature increase, these materials behave as good conductors.

The forbidden gap in such materials is *very narrow* as shown in fig. The forbidden gap is about 1 eV. In such materials, the energy provided by heat at room temperature is sufficient to lift the electrons from valence bond to conduction band. Therefore **at room temperature**, semiconductors are capable of **conduction**. But at **0ºK or absolute zero** (-273^{o} C), all the electrons of semiconductor materials

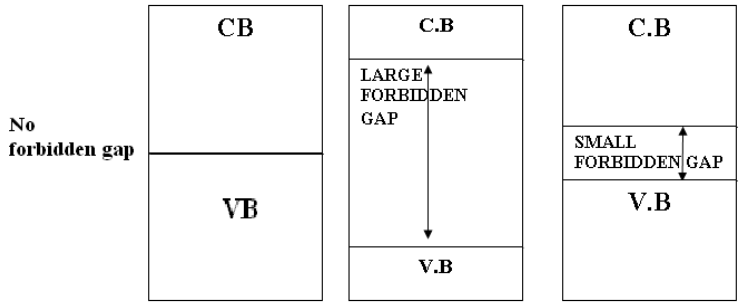
find themselves locked in the valence band. Hence at 0^oK, the semiconductor materials behave as **perfect insulators**. In case of semiconductors, forbidden gap energy depends on the temperature. For silicon and germanium, this energy is given by,

$E_G = 1.21 – 3.6 \times 10^{-4} \times T$ eV (for Silicon)

$E_G = 0.785 – 2.23 \times 10^{-4} \times T$ eV (for Germanium)

Where T = Absolute temperature in ^oK

Assuming room temperature to be 27^o C i.e. 300^oK, the forbidden gap energy for Si and Ge can be calculated from the above equations. The forbidden gap for germanium is 0.72 eV while for silicon it is 1.12 eV at room temperature.



Conductor Insulator Semiconductor

Figure 3:Energy Band Diagram of Conductor, Insulator, Semiconductor

Q. 3) *What is p type and n type semiconductors?*

Answer:

N – type Semiconductor

When a small amount of *pentavalent impurity* is added to a pure semiconductor, it is called n-type semiconductor.The pentavalent impurity has five valence electrons. Examples are arsenic, bismuth, phosphorous and antimony. Such an impurity is called **donor impurity**.

CRYSTAL STRUCTURE

Consider the formation of n-type material by adding phosphorous (P) into silicon (Si). The P atom has five valence electrons. A P atom fits in the silicon crystal in such a way that its four valence electrons form covalent bonds with four adjacent silicon atoms. The fifth electron has no chance of forming a covalent bond. These spare electrons enter the conduction band as a *free electron*. This means that each P atom added into Si atom gives *one free electron*. Since the free electrons have negative charges, the material is known as n-type material and an impurity donates a free electron hence called donor impurity.

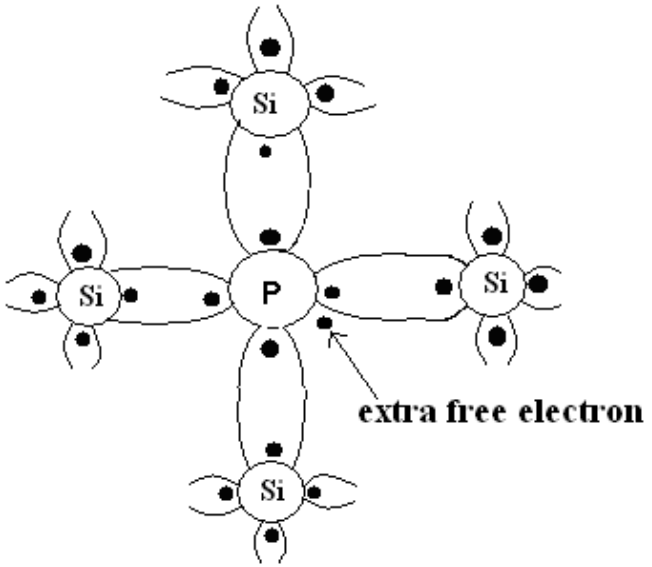


Figure 4: Crystal Structure of N type Semiconductor

CHARGE CARRIERS

Every P atom added into silicon atom gives one free electrons. Hence at absolute zero temperature, n-type semiconductor contains electron as a majority charge carriers. At room temperature, the number of valence electrons absorbs the thermal energy, due to which they *break the covalent bond* and become free electrons and then drift to the *conduction band*.

Hence at room temperature, the n-type semiconductor contains free electrons as well as holes. *The concentration of free electrons is always greater than holes in extrinsic semiconductor*. Thus in an n-type semiconductors, *free electrons* are called **majority carriers** while the *holes* are called **minority carriers**.

CONDUCTIVITY

When a voltage is applied to the n-type semiconductor, the free electrons move in a direction of positive terminal of voltage applied. This constitutes an *electron current*. While the holes moves in a direction of negative terminal of voltage applied. This constitutes *hole current.* Thus the conduction is dominant by free electrons.

The holes are less in number hence electron current is dominant over the hole current.

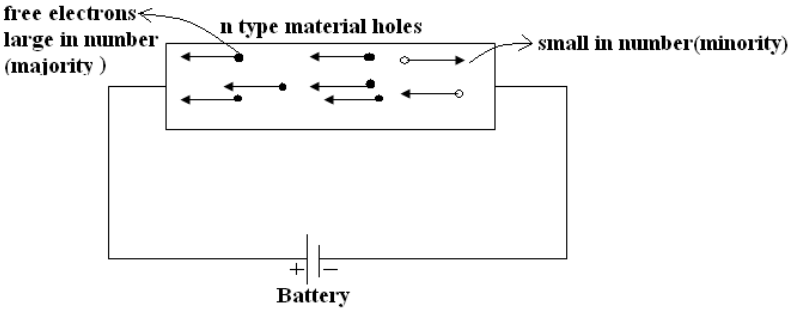


Figure 5: Biased N type Semiconductor

ENERGY BAND DIAGRAM

In n-type semiconductor, a donor impurity is added. Each donor atom donates one free electron and there is large number of free electrons available in the conduction band. The donor energy level E_D is just below the conduction band and its distance is 0.01 eV below the conduction band in germanium while it is 0.05 eV for silicon. Due to abundant free electrons, the probability of occupying the energy level by the electrons towards the conduction band is more. So in n-type material, the Fermi level E_F gets shifted towards the conduction band. But it is below the donor energy level.

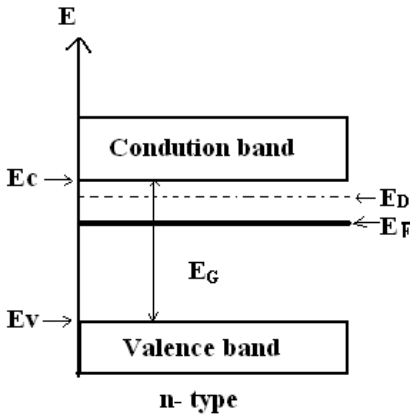


Figure 6: Energy Band diagram of N-type Semiconductor

P – type Semiconductor

When a small amount of *trivalent impurity* is added to a pure semiconductor, it is called p-type semiconductor. The trivalent impurity has three valence electrons. Examples are gallium, boron and indium. Such an impurity is called **acceptor impurity**.

CRYSTAL STRUCTURE

Consider the formation of p-type material by adding gallium (Ga) into silicon (Si). The Ga atom has three valence electrons. A Ga atom fits in the silicon crystal in such a way that its three valence electrons form covalent bonds with three adjacent silicon atoms. Being short of one electron, the fourth covalent bond in the valence shell is incomplete. The resulting vacancy is called a *hole*.

This means that each Ga atom added into Si atom gives one hole. Since the holes have positive charges, the material is known as p-type material and an impurity accepts a free electron hence called acceptor impurity.

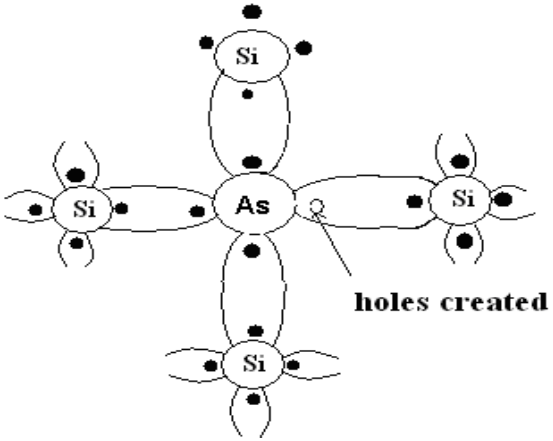


Figure 7: Crystal Structure of P type Semiconductor

CHARGE CARRIERS

Every **As** atom added into silicon atom gives one holes. Hence at absolute zero temperature, p-type semiconductor contains holes as a majority charge carriers. At room temperature, the number of valence electrons absorbs the thermal energy, due to which they *break the covalent bond* and become free electrons and then drift to the *conduction band*.

Hence at room temperature, the p-type semiconductor contains holes as well as free electrons. *The concentration of holes is always greater than free electrons in extrinsic semiconductor*. Thus in a p-type semiconductors, *holes*are called **majority carriers** while the *free electrons* are called **minority carriers**.

CONDUCTIVITY

When a voltage is applied to the p-type semiconductor, the holes move in a direction of negative terminal of voltage applied. This constitutes a *hole current*. While the free electrons moves in a direction of positive terminal of voltage applied. This constitutes *an electron current.* Thus the conduction is dominant by holes.

The free electrons are less in number hence hole current is dominant over the electron current.

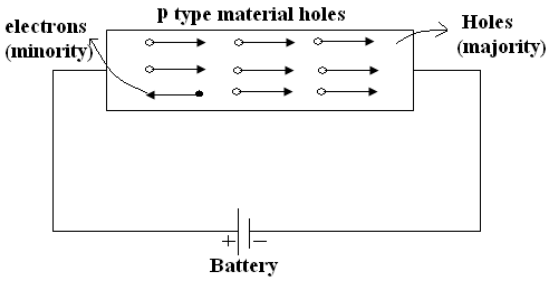


Figure 8: Biased P type Semiconductor

ENERGY BAND DIAGRAM

In p-type semiconductor, an acceptor impurity is added. Each acceptor atom accepts one free electron and hence there are large number of holes get created in the valence band. The acceptor energy level E_A is just above the valence band. Due to abundant holes, the probability of occupying the energy level by the holes towards the valence band is more. So in p-type material, the Fermi level E_F gets shifted towards the valence band. But it is above the acceptor energy level.

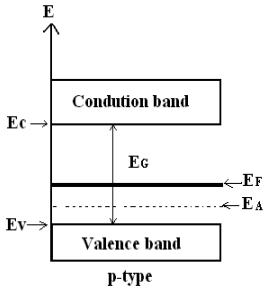


Figure 9: Energy Band diagram of P-type Semiconductor

Q. 4) *Explain Unbiased P-N junction in detail***.**
Answer: When a p-type semiconductor is joined to n-type semiconductor, the contact surface is called *p-n junction*.

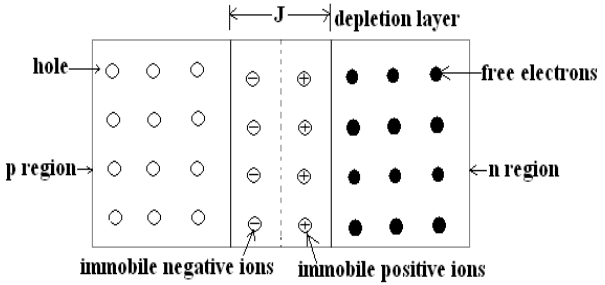


Figure 10: Unbiased P-N junction
When a p-n junction is formed,

The *free electrons* from n-region start diffusing into p-region. Similarly the *holes* from p-side diffuse across the junction into n-region. In p-region, there are acceptor atoms, having holes and the electrons diffusing from n-region fill these holes and become *negatively charged ions*. Hence near the junction there is an accumulation of such negative charges in p-region. Similarly in n-region, there are donor atoms, having free electrons and the holes diffusing from p-region recombine with these electrons and become *positively charged ions*. Hence near the junction there is an accumulation of such positive charges in n-region.

As more and more electron recombine in p-region and holes in n-region, more charges get formed near the junction. When sufficient negative charge gets accumulated in p-region near the junction, the electrons experiences a force of repulsion, while diffusing from n-region to p-region. Hence *diffusion stops*. Same happens in n-region. Hence there exists a layer of negative charges in p-region and positive charges in n-region, near the junction. This region, which consists of negative and positive charges i.e. immobile ions and the region, is without any free electrons and holes is called *depletion region* or depletion layer. The potential across depletion region is called *barrier potential* or *cut-in voltage* (V_γ).
V_γ =0.7 V for Si & 0.3 V for Ge.

The depletion layer is practically extremely thin and being of the order of 0.5 to 1 micron where 1 micron is 10^{-6} m.

Q. 5) *Explain PN junction diode with its characteristics*
Answer: Biasing of any electronic device means the application of external D.C voltage.The primary

usefulness of a diode is its ability to allow current in only one direction. This is essentially controlled by way of biasing adiode.

Depending upon the polarity of the D.C voltage externally applied to it,the biasing is classified as Forward biasing and Reverse biasing.

FORWARD BIAS:-

When a p-side is connected to positive terminal and n-side is connected to negative terminal of battery, then this condition is called Forward biasing.

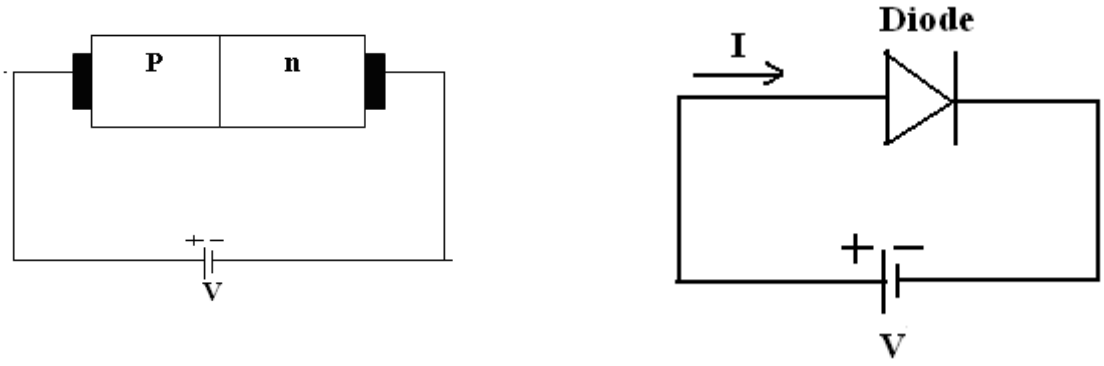


Figure 11: Forward biased PN junction Diode

P region contains holes which are repelled due to positive terminal of battery, move toward the junction. Whereas, n-contains electrons which are repelled due to negative terminal of battery, move toward the junction. Due to applied forward voltage V_F, width of depletion region becomes smaller. At a voltage greater than cut-in voltage, depletion region gets almost collapsed. Hence electrons from n-region cross the junction reach p-region, constituting electron current and holes from p-region cross the junction and reach n-region, constituting hole current. Thus the ***forward current*** **(I_F)** is formed due to both types of current.

Forward current is always measured in mili-amperes (mA).

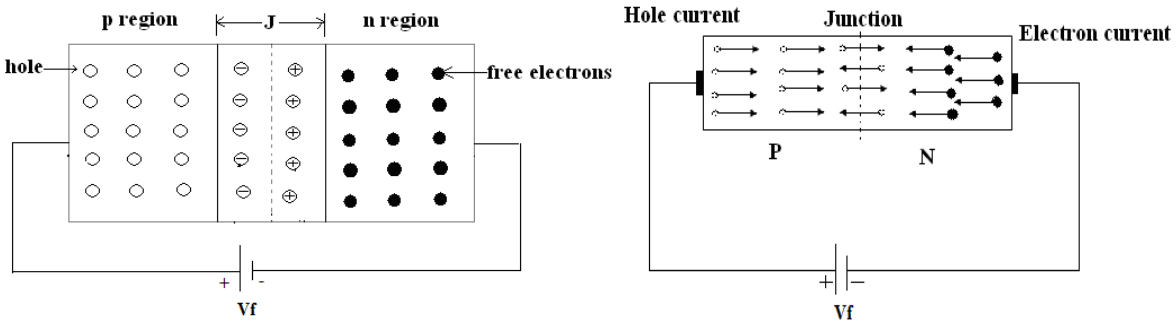


Figure 12: Forward biased PN junction Diode

REVERSED BIAS:-

When a p-region is connected to negative terminal and n-region is connected to positive terminal of battery, then this condition is called Reverse biasing.

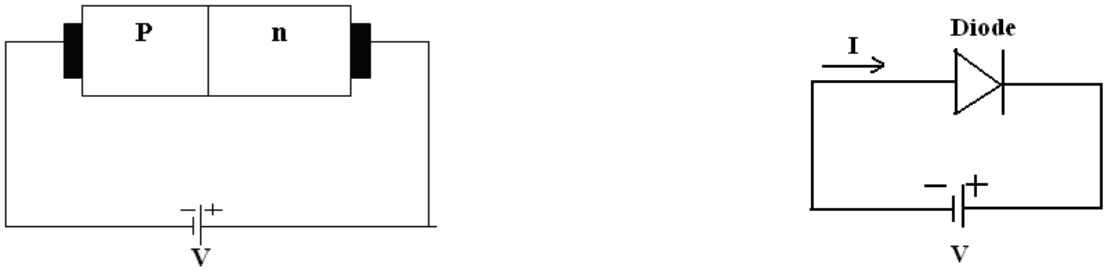


Figure 13: Reversed biased PN junction Diode

p region contain holes which gets attracted towards negative terminal of battery hence holes move away from the junction. n-region contain electrons which gets attracted towards positive terminal of battery, hence electron moves away from the junction. Due to applied reverse voltage V_R, this depletion region widens. As depletion region widens, barriers potential across the junction also increases. As no majority carriers crossing the junction, ***reverse current*** (**I_R**) is essentially *zero* (ideally). Hence small minority carriers (holes in n-region and electrons in p-region) cross the junction due to polarity of battery. Hence a small current result due to the movement of such minority carriers. This small current is called ***reverse saturation current*****(I_0)**. As generation of minority charge carriers depends upon temperature, hence reverse saturation current is dependent on temperature and it is practically independent on reverse voltage.

Reverse current is measured in uA.

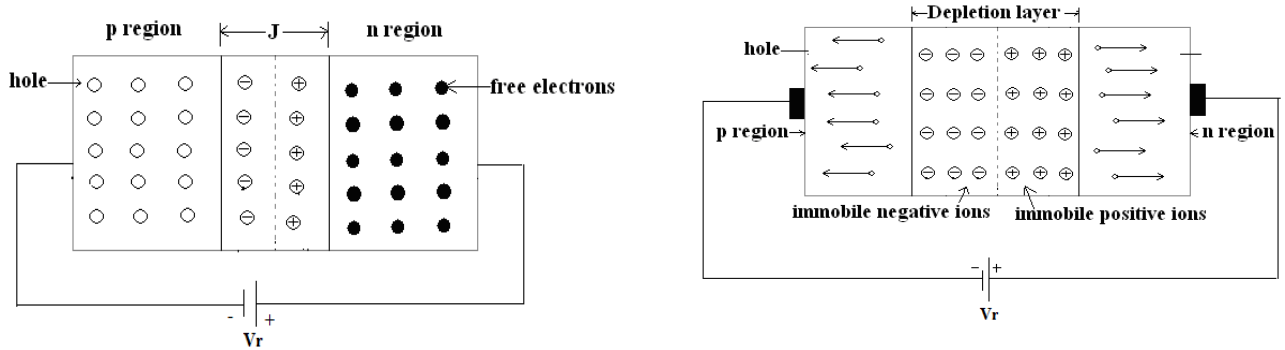


Figure 14: Reversed biased PN junction Diode

V-I CHARACTERISTICS

It is a graph plotted in between Voltage and current for a p-n junction diode. As there are two types of biasing modes, V-I characteristic is again of two types:

Forward Characteristics:

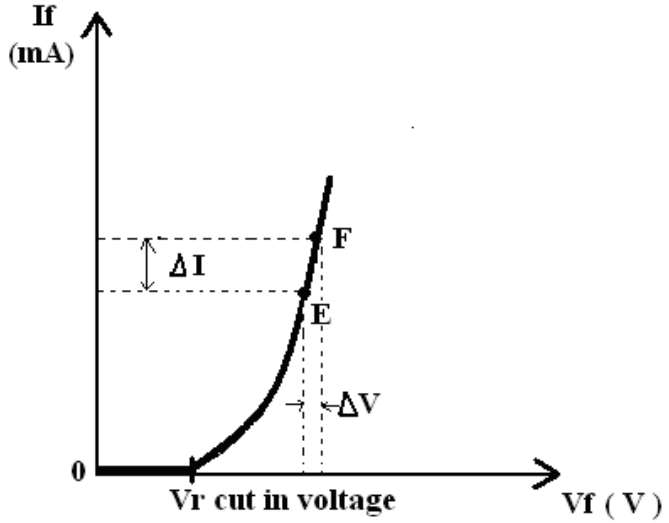


Figure 15: Forward Characteristics

Here, the applied voltage is denoted as $\mathbf{V_f}$ and the forward current is $\mathbf{I_f}$. The graph of I_f against V_f is called forward characteristics of diode.

As long as the forward voltage (V_f) is less than the barrier potential **(V_r)**, there is no forward current, so I_f is zero. Once forward voltage (V_f) is greater than barrier potential (V_r), the forward current (I_f) starts flowing. Once the depletion layer collapses, the current I_f increases drastically. The nature of the forward characteristics is *exponential*.

The forward current is the conventional current, hence it is treated as positive and the forward voltage treated as positive. Hence the forward characteristic is plotted in *first quadrant*.
The resistance offered by p-n junction is called *forward resistance*.
The current equation is given by,

$$\mathbf{I = I_0 \left(e^{V / \eta Vt} - 1\right)}$$

Where, I = Output current (I_f = forward current and I_r = reverse current)
I_0 = Reverse saturation current
V = applied voltage (V_f= forward voltage and V_r = reverse voltage)
η = intrinsic coefficient (1 for Ge and 2 for Si)
Vt = Voltage equivalent of temperature = K.T
At 300°K, Vt = 26mV
For forward characteristics, V = V_F = positive & I = I_F = positive,
As exponential index has positive sign, hence $e^{Vf/\eta VT} >> 1$
Neglecting 1,

$$\mathbf{I_F = Io\ e^{Vf/\eta VT}}$$

Because of exponential term, forward characteristic is exponential in nature.

Reverse Characteristics:

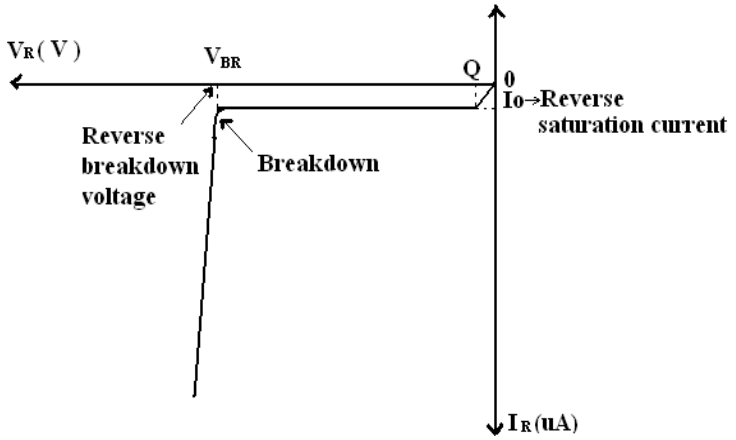


Figure 16: Reverse Characteristics
Here, the applied voltage is denoted as $\mathbf{V_R}$ and the reverse current is $\mathbf{I_R}$. The graph of reverse current

I_R against the applied reverse voltage **V_R** is called reverse characteristics of diode. As reverse voltage is increased initially but after a certain voltage, the current remains constant equal to the reverse saturation current (Io) through reverse voltage is increased. Reverse voltage is taken negative. The reverse saturation is due to minority carriers is opposite to forward current, hence taken as negative. Hence this characteristic is plotted in *third quadrant*. The resistance offered in reverse bias condition is called reverse resistance.

The current equation is given by

$I = Io (e^{V/nVT} - 1)$

For reverse characteristics, $V = V_R$ = negative & $I = I_R$ = negative,

As exponential index has negative sign, hence $e^{Vr/\eta VT} << 1$.

Neglecting exponential term,

$I_R = Io (-1) = -Io$

Indicates that under reversed biased condition, the current is reverse saturation current which is negative and it flows in opposite direction to that of forward current & almost constant. As, Io is due to minority carriers generated due to thermal energy, hence it is temperature dependent while V_T is also temperature dependent. Hence we can say that entire V – I characteristics is dependent on the temperature.

Q.6) *What is Rectifier? Explain half wave Rectifier with Input Output Waveform and derive the equation for I_{dc}, $V_{dc}$and Efficiency.*

Answer: A Rectifier is a device which converts AC voltage to pulsating DC voltage, using one or more p-n junction diodes.

HALF WAVE RECTIFIER

In half wave rectifier, rectifying element conducts only during positive half cycle of input AC supply. The negative half cycles of AC supply are eliminated from the output.

Construction:

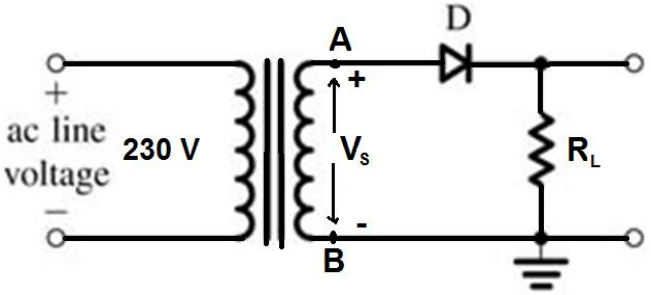


Figure 17: Circuit Diagram of Half wave rectifier

This rectifier circuit consists of resistive load (R_L), rectifying element i.e. p-n junction diode, and the source of AC voltage, all connected in series. Usually, the rectifier circuits are operated from AC mains supply. To obtain the desired DC voltage across the load, the AC voltage is applied to rectifier circuit using suitable step-up or step-down transformer, mostly a step-down one, with necessary turn's ratio. The input voltage to the half- wave rectifier circuit is a sinusoidal AC voltage, having a frequency which is the supply frequency, 50 Hz. The transformer decides the peak value of the secondary voltage. If the N_1 are primary number of turns and N2 are secondary number of turns and E_{PM} is the peak value of the primary voltage then

$(N_1/N_2) = (E_{SM}/E_{PM})$

Where E_{SM} is the peak value of the secondary AC voltage.

Operation:

During the *positive half cycle* of secondary AC voltage (V_S), terminal (A) becomes positive with respect to terminal (B). The diode is forward biased and the current flows in the circuit in the clockwise direction, as shown in fig. The current will flow for almost full positive half cycle. This current is also flowing through load resistance R_L hence denoted as $\mathbf{I_L}$, the load current and load voltage $\mathbf{V_L}$ is obtained. During *negative half cycle*, when terminal (A) is negative with respect to terminal (B), diode becomes reverse biased. Hence no current flows through the circuit, hence no load voltage is obtained across R_L. The load voltage, being the product current and load resistance, will also be in the form of half sinusoidal pulse. The different waveforms are illustrated in fig.

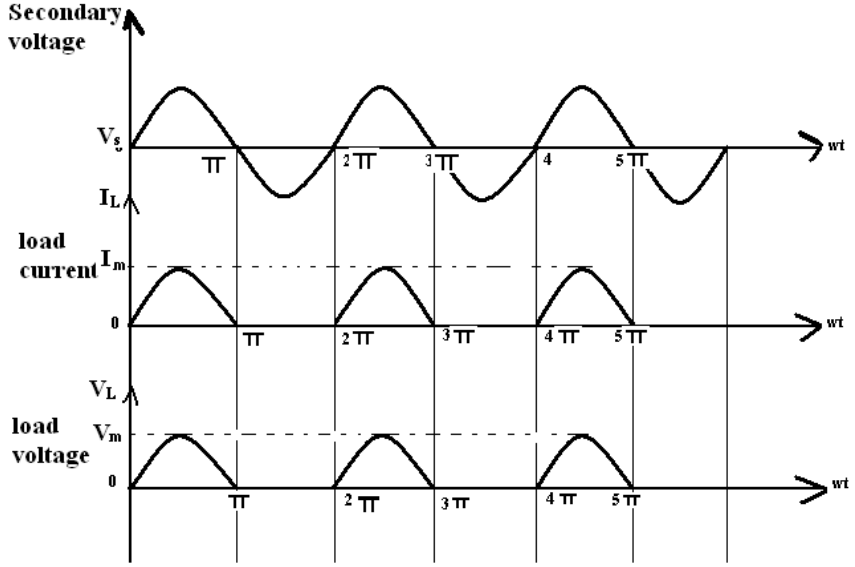


Figure 18: Waveform

The DC output waveform is expected to be a straight line but the half wave rectifier gives output in the form of positive sinusoidal pulses. Hence the output is called pulsating DC. It is discontinuous in nature. Hence it is necessary to calculate the average value of load current and average value of a output voltage.

1) Average DC load Current (I_{DC})

The average or DC value of alternating current is obtained by *integration*.

For finding out the average value of an alternating waveform, *determine the area under the curve over one complete cycle i.e. from 0 to 2π and then dividing it by the base i.e. 2π*.

Mathematically, current waveform can be described as,

$I_L = I_m \sin wt$ for $0 \le wt \le \pi$

$I_L = 0$ for $\pi \le wt \le 2\pi$

where I_m = peak value of load current

$I_{DC} = (1 / 2\pi) [\int_0^{2\pi} I_L dwt]$

$= (1 / 2\pi)[\int_0^{\pi} I_L dwt + \int_{\pi}^{2\pi} I_L dwt]$

Substituting value of I_L

$= (1 / 2\pi)[\int_0^{\pi} I_m \sin wt dwt + \int_{\pi}^{2\pi} 0 \, dwt]$

$= (I_m / 2\pi) [(-\cos wt)_{0-\pi}]$

$= (- I_m / 2\pi) [(\cos\pi – \cos 0]$

$= (- I_m / 2\pi) [-1 - 1]$

$I_{DC} = Im / \pi$

2) Average DC Load Voltage (V_{DC})

It is the product of average DC load current and the load resistance R_L.

$V_{DC} = I_{DC} R_L$

Substituting value of I_{DC},

$V_{DC} = (I_m / \pi) \times R_L$ $= E_{sm} / (R_F + R_L + R_S)\pi * R_L$

3) R.M.S Value of load Current (I_{RMS})

The R.M.S means squaring, finding mean and then finding square root. Hence R.M.S value of load current can be obtained as,

$I_{RMS} = \sqrt{(1 / 2\pi) [\int_0^{2\pi} (I_L)^2 dwt]}$

$= \sqrt{(1 / 2\pi)[\int_0^{\pi} (I_L)^2 dwt + \int_{\pi}^{2\pi} (I_L)^2 dwt]}$

$= \sqrt{(1 / 2\pi) [\int_0^{\pi} (I_m)^2 \sin^2 wt dwt + \int_{\pi}^{2\pi} 0 \, dwt]}$

$= \sqrt{((I_m)^2 / 4\pi) [\int_0^{\pi} (1 – \cos 2wt) dwt]}$

$= \sqrt{((I_m)^2 / 4\pi) [(\int_0^{\pi} 1 dwt) – (\int_0^{\pi} \cos 2wt)]}$

$= \sqrt{((I_m)^2 / 4\pi) [(wt)_{0-\pi} – (\sin 2wt/2)_{0-\pi}]}$

$= \sqrt{((I_m)^2 / 4\pi)\,[\pi - 0]}$

$I_{RMS} = Im / 2$

4) Efficiency (η): It is the ratio of output DC power to the AC input power.

$\eta = P_{DC} / P_{AC}$

DC Power (P_{DC})

$P_{DC} = I_{DC}^2 R_L$

$= (I_m / \pi)^2 R_L$

$= (I_m^2 / \pi^2 R_L)$

AC Power (P_{AC})

$P_{AC} = I_{RMS}^2 (R_L + R_F + R_S)$

$= (I_m^2/4)(R_L + R_F + R_S)$

Hence,

$\% \eta = P_{DC} / P_{AC}$

$= (I_m^2 / \pi^2 R_L) / (Im^2/4)(R_L + R_F + R_S)$

Neglecting Rs and R_F

$= (4/\pi^2) \times 100$

$= 0.406 \times 100$

$\eta = 40.6\%$

Q. 7) *What is Rectifier? Explain center tapped Full wave Rectifier with Input Output Waveform and derive the equation for I_{dc}, V_{dc} and Efficiency.*

Answer: A Rectifier is a device which converts AC voltage to pulsating DC voltage, using one or more p-n junction diodes.

Center tapped Full wave Rectifier

In full wave rectifier, rectifying element conducts during both positive half cycle and negative half cycle of input AC supply.

Construction:

In Full wave rectifier, diode conducts during both positive and negative half cycle of input AC supply. In order to rectify both the half cycles of AC input, *two diodes* are used in this circuit. The diodes feed a common load R_L with the help of a *centre tap transformer*. The AC voltage is applied through a suitable power transformer with proper turns ratio.

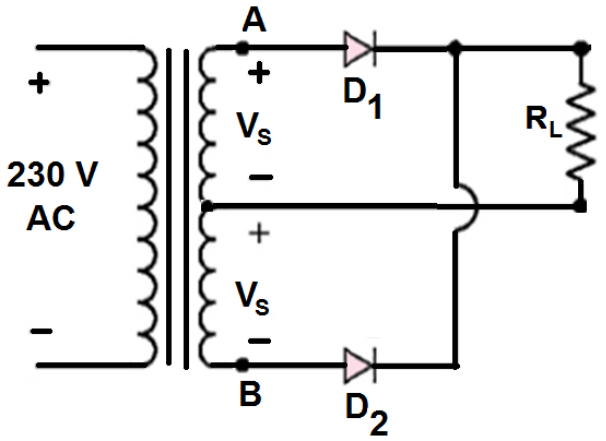


Figure 19: Circuit Diagram of Center Tapped Full wave rectifier

For the proper operation of the circuit, a center-tap on the secondary winding of the transformer is essential.

Operation**:**

Consider the *positive half cycle* of AC input voltage (V_S) where terminal A is positive and terminal B is negative. The diode D1 will be forward biased and hence will conduct; while D2 will be reversed biased and will acts as open circuit and will not conduct. The diode D1 supplies the load current that is $I_L = I_{D1}$. This current is flowing through upper half of secondary winding while the lower half of secondary winding of the transformer carries no current since diode D2 is reversed biased. In the next cycle of AC input, polarity reverses and terminal A becomes negative and B becomes positive. The diode D2 conducts, being forward biased, while D1 does not, being reversed biased. The diode D2 supplies the load current, i.e. $I_L = I_{D2}$. Now the lower half of secondary winding carries the current but the upper half does not.

It is noted that the load current flows in both half cycles of AC voltage and in the same direction through the load resistance. Hence we get rectified output across the load. The load current is sum of individual diode currents flowing in corresponding half cycle.

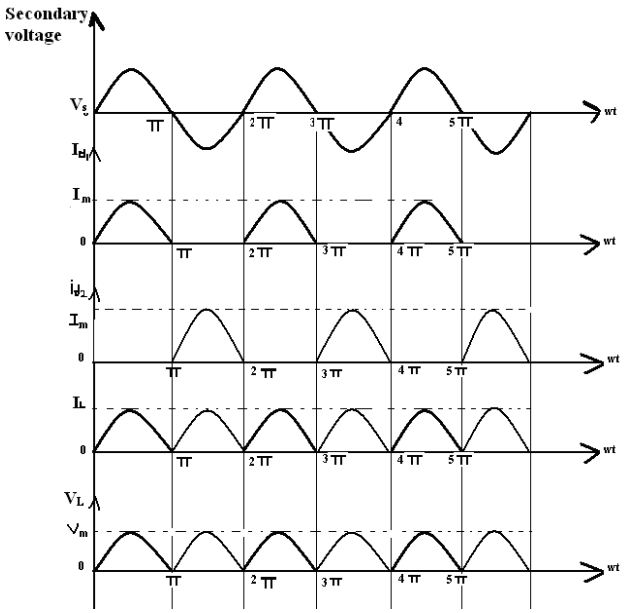


Figure 20: Waveform

1) Average DC load Current (I_{DC})

The average or DC value of alternating current is obtained by *integration*.

Mathematically, current waveform can be described as,

$I_L = I_m \sin wt$ for $0 \leq wt \leq \pi$

but from π to 2π, the current I_L is again positive while sinwt term is negative during π to 2π

$I_L = - I_m \sin wt$ for $\pi \leq wt \leq 2\pi$

$I_{DC} = (1 / 2\pi) [{}_0\int^{2\pi} I_L \, dwt]$

$= (1 / 2\pi)[{}_0\int^{\pi} I_L dwt + {}_\pi\int^{2\pi} I_L dwt]$

Substituting value of I_L

$= (1 / 2\pi)[{}_0\int^{\pi} I_m \sin wt dwt - {}_\pi\int^{2\pi} I_m \sin wt dwt dwt]$

$= (I_m / 2\pi) [(-\cos wt)_{0-\pi} + (\cos wt)_{\pi-2\pi}]$

$= (I_m / 2\pi) [(-\cos\pi + \cos 0 + \cos 2\pi - \cos\pi]$

$= (I_m / 2\pi) [1 + 1 + 1 + 1]$

$I_{DC} = 2Im / \pi$

2) Average DC Load Voltage (V_{DC})

It is the product of average DC load current and the load resistance R_L.

$$V_{DC} = I_{DC}R_L$$

Substituting value of I_{DC},

$$\boxed{V_{DC} = (2I_m / \pi) \times R_L} = 2E_{sm} / (R_F + R_L + R_S)\pi \times R_L$$

3) R.M.S Value of load Current (I_{RMS})

The R.M.S means squaring, finding mean and then finding square root. Hence R.M.S value of load current can be obtained as,

$$I_{RMS} = \sqrt{(1 / 2\pi) [\int_0^{2\pi}(I_L)^2 dwt]}$$

$$= \sqrt{(1 / 2\pi)[\int_0^{\pi}(I_L)^2 dwt + \int_{\pi}^{2\pi} (I_L)^2 dwt]}$$

$$= \sqrt{(1 / 2\pi) [\int_0^{\pi}(I_m)^2 \sin^2 wt dwt + \int_{\pi}^{2\pi}(I_m)^2 \sin^2 wt dwt]}$$

$$= \sqrt{(2(I_m)^2 / 2\pi) [\int_0^{\pi} \sin^2 wt dwt]}$$

$$= \sqrt{((I_m)^2 / 2\pi) [(\int_0^{\pi} 1 dwt) - (\int_0^{\pi} \cos 2wt)]}$$

$$= \sqrt{((I_m)^2 / 2\pi) [(wt)_{0-\pi} - (\sin 2wt/2)_{0-\pi}]}$$

$$= \sqrt{((I_m)^2 / 2\pi) [\pi - 0]}$$

$$\boxed{I_{RMS} = Im / \sqrt{2}}$$

4) Efficiency

$\eta = P_{DC} / P_{AC}$

DC Power (P_{DC})

$P_{DC} = I_{DC}^2 R_L$

$= (2I_m / \pi)^2 R_L$

$=(4I_m^2 / \pi^2 R_L)$

AC Power (P_{AC})

$P_{AC} = I_{RMS}^2(R_L + R_F + R_S)$

$=(I_m^2/ 2)(R_L + R_F + R_S)$

Hence,

$\% \eta = P_{DC} / P_{AC}$

$=(4I_m^2 / \pi^2 R_L) /(Im^2/2) (R_L + R_F + R_S)$

Neglecting Rs and R_F

$= (8/\pi^2) \times 100$

$= 0.812 \times 100$

$$\boxed{\eta = 81.2\%}$$

Q. 8) *A Ge diode has a reverse saturation current of 3uA.Calculate the voltage at which 1% of the rated current will flow through the diode,at room temperature if diode is rated for 1A.*

Answer:- $\eta = 1$ for Ge,

$Io = 3uA = 3 \times 10^{-6}A$

Rated current = 1 A

I = 1% of rated current = 0.01A

V_T = 26 mV at room temperature

Using current equation of diode,

$I = Io[e^{V/nVT}-1]$

$0.01=3x10^{-6}[e^{V/1x26x10-3}-1]$

$e^{V/26x10-3}-1= 3333.33$

$e^{V/26x10-3} = 3334.33$

taking natural log of both sides,

$\ln (e^{V/26x10-3})= \ln (3334.33)$

$V/26x10^{-3}= 8.112$

V = 0.2109 V

Q. 9) *For what values of reverse voltage will the reverse current reach 90% of its saturation value at room temperature. Assume Si p-n junction diode.*

Answer: - $\eta = 2$ &V_T = 26mV

I = - (90% of Io)

= - 0.9Io

We know $I = Io[e^{V/nVT}-1]$

$-0.9Io = Io(e^{V/2x26x10-3}-1)$

$-0.9 = e^{V/52x10-3}-1$

$0.1 = e^{V/52x10-3}$

$V / 52 \times 10^{-3} = \ln (0.1) = -2.3025$

V = - 0.1198 V

Q. 10) *What are the characteristics of a rectifier circuit?*

Answer: The important points to be studied while analyzing the various rectifier circuits are,

a) **Waveform of the load current:**As rectifier converts AC to pulsating DC**,** it is important to analyze the nature of the current through load which ultimately determines the waveform of the load voltage.

b) **Regulation of the output voltage:** As the load current changes, load voltage changes. Practically load voltage should remain constant. So concept of regulation is to study the effect of change in load current on the load voltage.

c) **Rectifier efficiency:** It signifies how efficient the rectifier circuit converts Ac power into DC power.

d) **Peak value current in the rectifier circuit:** The peak value is the maximum value of an alternating current in the rectifier circuit. This decides the rating of the rectifier circuit element which is diode.

e) **Peak value of voltage across the rectifier element in the reverse direction (PIV):** When the diode is not conducting, the reverse voltage gets applied across the diode. The peak value of such voltage decides the peak inverse voltage i.e. PIV rating of a diode.

f) **Ripple factor:** The output of the rectifier is of pulsating DC type. The amount of AC content in the output can be mathematically expressed by a factor called ripple factor.

Q. 11) *Write short note on BJT.*

Answer:

When a third doped element is added to a crystal diode in such a way that two PN junctions are formed, the resulting device is known as a transistor. The transistor is capable of achieving amplification of weak signals in a fashion comparable and often superior to that realized by vacuum tubes. The amplification in the transistor is achieved by passing the signal from a region of *low resistance* to a region of *high resistance*. This concept of transfer of resistance has given the name **Transistor** (Transfer + Resistor). Transistor can be used for amplification in analog purpose while in digital purpose transistor can be used for designing digital gates and switches. BJT's are basically of two types: an **N-P-N** and **P-N-P** type.

When a transistor is formed by sandwiching a single p-region between two n-regions, it is an n-p-n type transistor. The p-n-p type transistor has a single n-region between two p-region, as shown in fig.

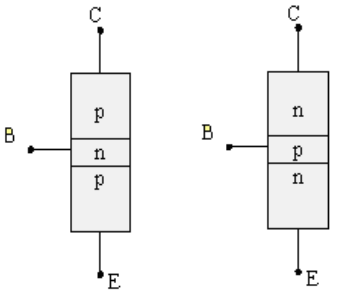


Figure 21: N-P-N and P-N-P type Transistor

A transistor(P-N-P or N-P-N) has three sections of doped semiconductors. The section on one side is the emitter and the section on the opposite side is the collector. The middle section is called the base and forms two junctions between the emitter and collector.

Emitter:

The section on one side that *supplies charge carriers* (electrons or holes) is called the emitter. Emitter is highly doped. The emitter is always *forward bias* with respect to base so that it can supply a large number of majority carriers i.e. holes if emitter is of p-type and electrons if the emitter is n-type.

Collector:

The section on the other side that *collects the charge carriers* is called the collector. The collector is heavily doped. But the doping level in collector is *slightly less* than that of emitter and the collector region area is slightly more than that of emitter. The collector is always *reversed biased*. Its function is to remove charges from its junction with the base.

Base:

The middle section which forms two PN junctions between the emitter and collector is called the base. This region is very thin and lightly doped. The base-emitter junction is forward biased, allowing low resistance for the emitter circuits. The base-collector junction is reversed biased and provides high resistance with collector circuit.

Q. 12) *What do you mean by unbiased transistor?*

Answer:

A transistor has two PN junctions. One junction is in between the emitter and the base, and is called the Emitter Base junction, or simply the Emitter junction J_E. The other junction is between the base and the collector, and is called Collector Base junction, or simply Collector junction J_C. There are depletion regions at both the junctions and the width of depletion regions will be different because of different doping levels. Thus transistor is like two pn junction diodes connected back to back.

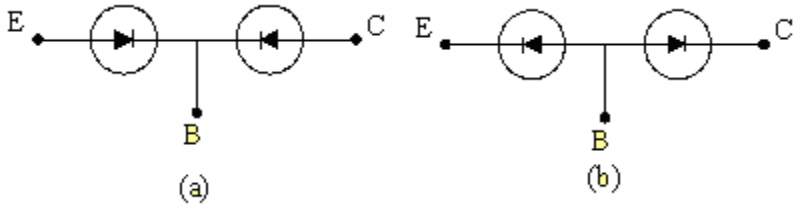


Figure 22: N-P-N and P-N-P type Transistor

An unbiased transistor means a transistor with no external voltage (biasing) is applied. Obviously, there will be no current flowing from any of the transistor leads. Since transistor is like two PN junction diodes connected back to back, there are depletion regions at both the junctions, emitter junction (J_E) and collector junction (J_C) as shown in fig.

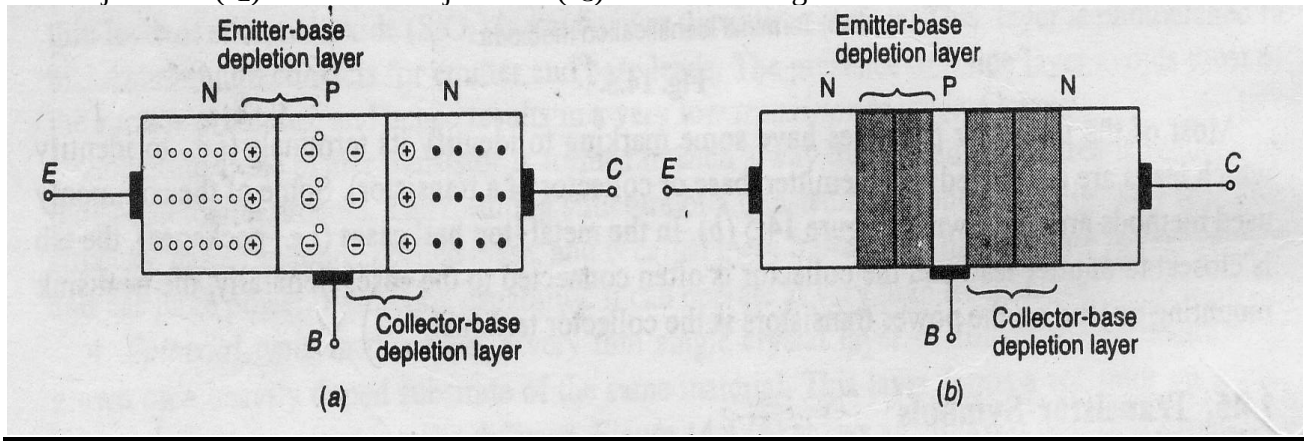


Figure 23: N-P-N and P-N-P type Transistor

Because of different doping levels in three regions, two depletion regions do not have same width. During diffusion process, depletion region *penetrates more deeply* into the lightly doped side

in order to include an equal number of impurity atoms in the each side of the junction. As shown in the fig., depletion region at emitter junction penetrates *less* in the heavily doped emitter and extends *more* in the base region. Similarly, depletion region at collector junction penetrates *less* in the heavily doped collector and extends *more* in the base region.
As collector is slightly less doped than the emitter, *the depletion layer width at the collector junction is more than the depletion layer width at the emitter junction*.

Q. 13) *What are the different regions of operation of transistor?*
Answer: In order to operate transistor properly as an amplifier, it is necessary to correctly bias the two PN junctions with external voltages. Depending upon external bias voltage polarities used, the transistor works in one of the three regions.
(1) Active region. (2) Cut-off region. (3) Saturation region.

Region	**Emitter base junction**	**Collector base junction**
Active	Forward Biased	Reverse Biased
Cut-off	Reverse Biased	Reverse Biased
Saturation	Forward Biased	Forward Biased

The externally applied bias voltages are $\mathbf{V_{EE}}$ and $\mathbf{V_{CC}}$ and biased the transistor in its respective region. The operation of the p-n-p is the same as for the n-p-n except that the roles of the electrons and holes, the bias voltage polarities, and the current direction are all reverse. Note that in both cases the emitter base junction is *forward bias* and the collector base junction is *reversed biased*.
Active region:

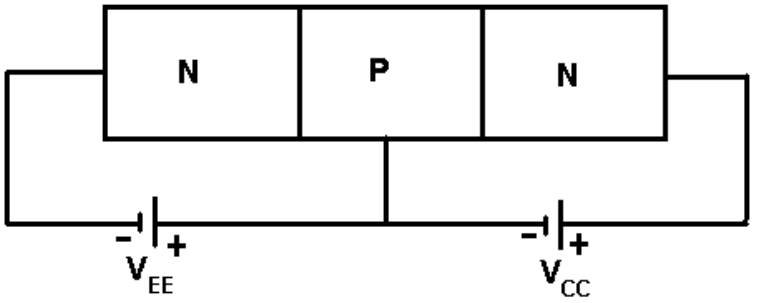


Figure 24: N-P-N Transistor

Saturation region:

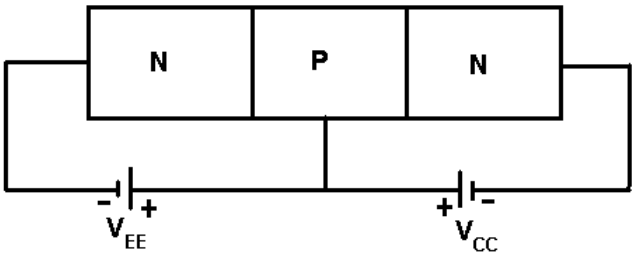


Figure 25: N-P-N Transistor

Cut-off region:

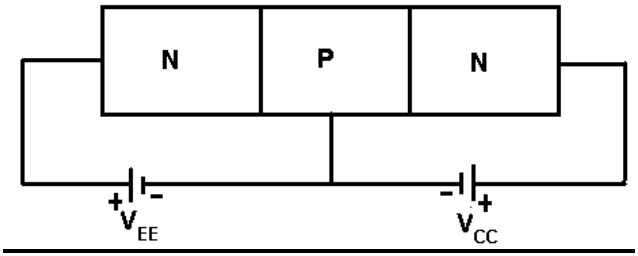


Figure 26: N-P-N Transistor

Q. 14) *Explain working of Common base configuration with its input and output characteristics.*
Answer:
In common base configuration, the *base is common* to both input and output terminals. The base is closest to or at ground potential. The arrow in the symbol defines the direction of emitter current direction (Conventional) through the device.

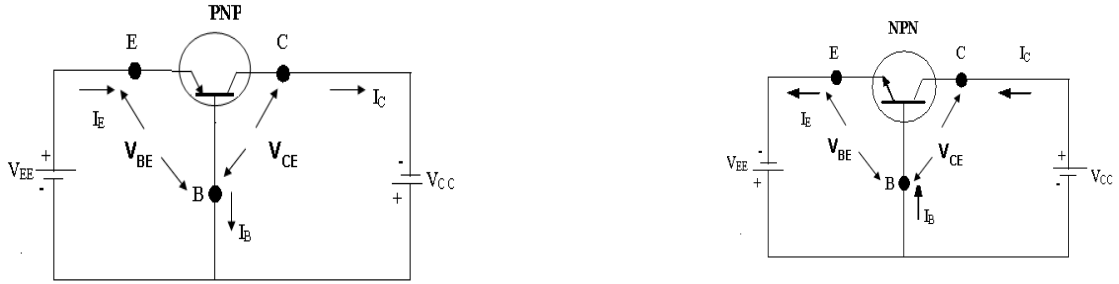


Figure 27: Circuit Diagram of Common Base configuration

INPUT CHARACTERISTICS

The input characteristics relate the *input current (I_E)* to *input voltage (V_{BE})* for different values of *output voltage (V_{CB})*. To determine the input characteristics, the NPN transistor is connected in common base configuration as shown in fig. To plot the input characteristics, the output voltage **(V_{CB})** is fixed and the input voltage **(V_{BE})** is varied in steps and corresponding input current **(I_E)** is recorded. When the output voltage is zero, the emitter base junction is forward biased and the input characteristics are essentially close to forward biased PN junction diode. When the collector to base voltage is increased, the depletion region at the CB junction increases and penetrate deeper into the base of the transistor. This reduces the distance between emitter-base and collector-base depletion regions, thus reducing distance between the two regions. This reduction in the resistance increases V_{CE}. Therefore the input characteristics shifts left with increase in V_{CB}.

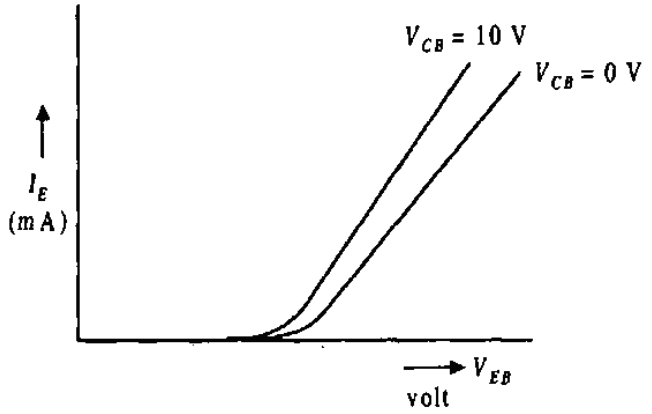


Figure 28: Input Characteristics

Current relations:

Current amplification factor(α)

Ratio of collector current to the total emitter current

$\alpha = I_C/I_E$

the range of α is from **0.95 to o.995**

$I_E = I_B + I_C$

$I_E = I_B + \alpha I_C$

$I_B = (1 - \alpha) I_E$

OUTPUT CHARACTERISTICS

The output characteristics for common base configuration are a plot between collector to base voltage (V_{CB}) and collector current (I_C) for various levels of emitter current (I_E). The output characteristics have 3 regions the ACTIVE, CUTOFF and SATURATION regions.

ACTIVE REGION: The active region is normally used for operating the transistor as an amplifier. In this region the emitter-base junction is **forward biased** while the collector-base junction is **reversed biased**. In this region when the emitter current $I_E = 0$, the collector current equals to reverse saturation current I_{CBO} which is in the order of microamperes. As emitter current increases, the magnitude of the collector current increases.

SATURATION REGION: In this region the emitter-base and collector-base junctions are **forward biased**. It is the region that lies to the *left of* $V_{CB} = 0$. Even when $V_{CB} = 0$, the collector current flows. When the collector base junction is forward biased the flow of charge carriers is reduced and the collector current reduces to zero.

CUTOFF REGION: In cutoff region the emitter base and collector base junctions of a transistor are **reversed biased**. The cutoff region in output characteristics is the region where $I_C = 0$.

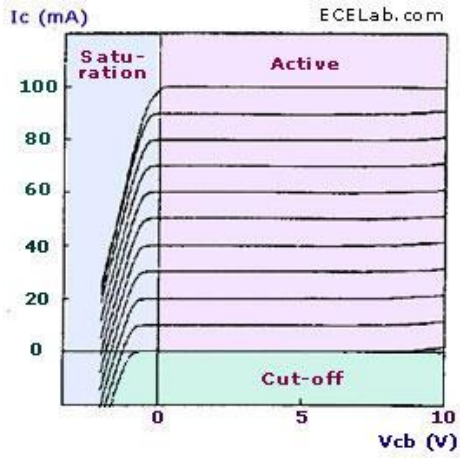


Figure 29: Output Characteristics

Q. 15) *Explain working of Common emitter configuration with its input and output characteristics.*
Answer: In common emitter configuration, emitter current is common to both input and output terminals.

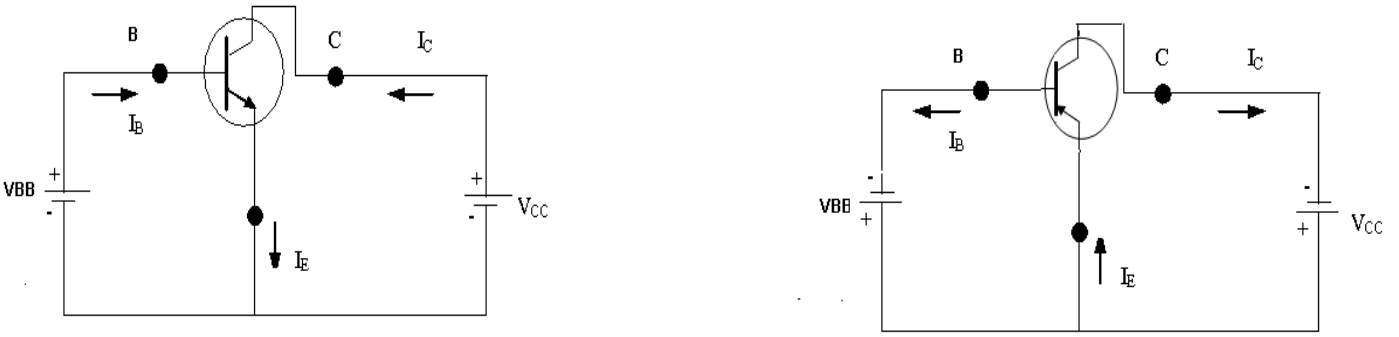


Figure 30: Circuit Diagram of Common Emitter configuration

INPUT CHARACTERISTICS

The input characteristics of a common emitter configuration are a plot between ***input current (I_B)*** and ***input voltage (V_{BE})*** for various values of ***output voltage (V_{CE})***. The base current is zero till the cut-in voltage and increases exponentially as V_{BE} increases. When the collector to emitter voltage increases, due to increase in width of depletion region, base current decreases for constant base to emitter voltage.

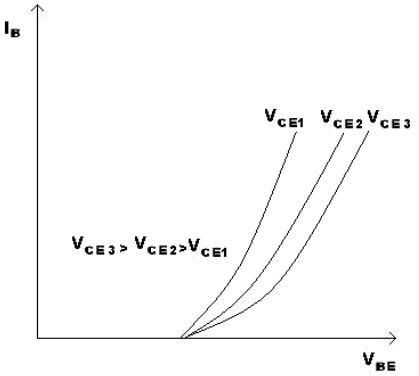


Figure 31: Input Characteristics

Current relation

Current amplification factor = β

We know $I_C = \alpha I_E$

& $I_E = I_B + I_C$

Hence, $I_C = \alpha(I_B + I_C)$

$I_C /\alpha =(I_B + I_C)$

$I_C [1/\alpha-1] = I_B$

$I_C [1-\alpha/\alpha] = I_B$

$I_C=[\alpha/ 1-\alpha]I_B$

$I_C = \beta I_B$

Relation between α & β

$\alpha = I_C/I_E$

$I_E = I_B + I_C$

$I_B = I_E - I_C$

$\beta = I_C /I_B$

$= I_C /I_E - I_C$

$= I_C / I_E /[I_E / I_E - I_C / I_E]$

$\beta = \alpha/ 1- \alpha$

DIVIDING BY 1+B

$\beta /1+ \beta = \alpha/ 1- \alpha /1+ \beta$

$== \alpha/ 1- \alpha /1 + (\alpha/ 1- \alpha)$

$= \alpha/ 1- 0$

$= \alpha$

$\alpha = \beta /1+ \beta$

OUTPUT CHARACTERISTICS

The output characteristics of a CE configuration are plot of ***collector to emitter voltage (V_{CE})*** to ***collector current (I_C)*** for a ***constant base current (I_B)***. It also has three regions ACTIVE, CUTOFF and SATURATION regions.

ACTIVE REGION: In this region the emitter-base junction is *forward biased* while the collector-base junction is *reversed biased*. When the value of V_{CE} is zero, the collector current is negligibly small. For V_{CE} between 0 and approximately 1V, the collector current rises sharply and become almost constant.

SATURATION REGION: In this region the emitter-base and collector-base junctions are forward

biased. In the graph this region corresponds to portion where $V_{CE} < 0.2V$.

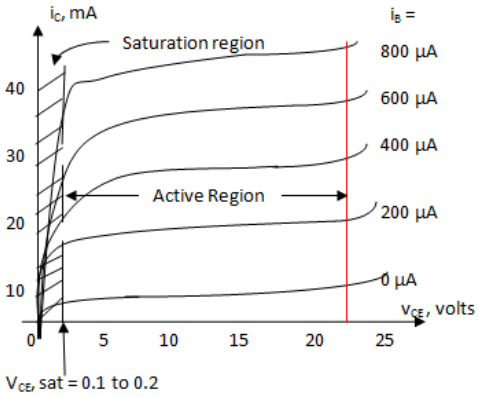


Figure 32: Output Characteristics

CUTOFF REGION: In cutoff region the emitter base and collector base junctions of a transistor are reversed biased. Here I_C is not equal to zero when I_B is zero.

Q. 16) *Explain working of Common collector configuration with its input and output characteristics.*
Answer:

In this configuration, the collector terminal is common to both input and output terminals. The output characteristics of common collector configuration are a plot between emitter current I_E and V_{CE}. Since I_C is approximately equal to I_E, the common collector output characteristic is practically identical to those of CEC. The input characteristics of common collector configuration are different from that of CBC and CEC. When V_{CB} increase, the base current I_B decreases, and reduces to zero as in fig.

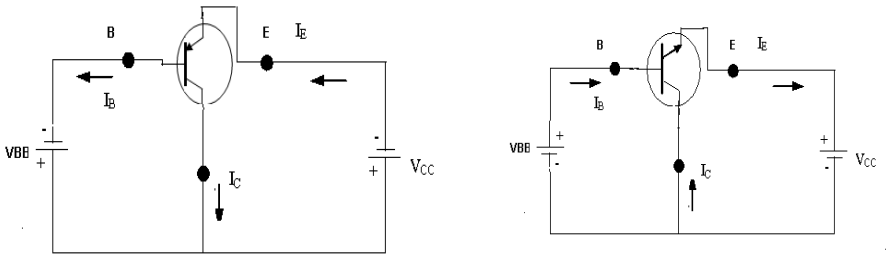


Figure 33: Circuit Diagram of Common Collector configuration

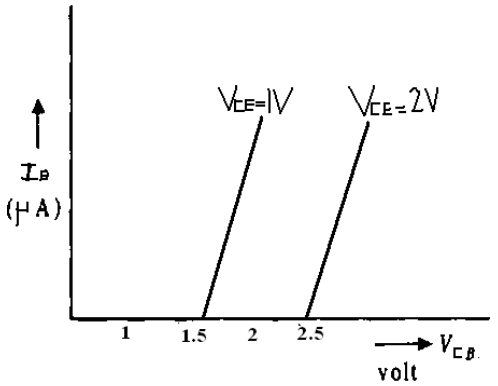


Figure 34:INPUT CHARACTERISTIC

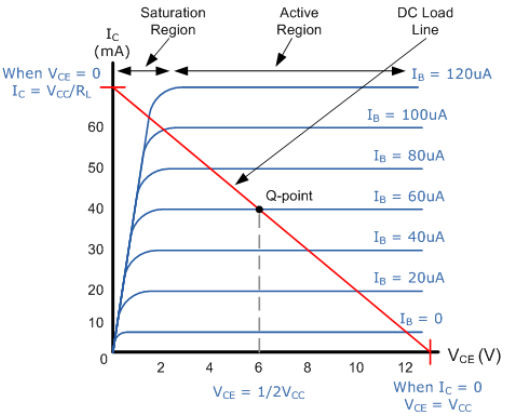


Figure 35:OUTPUT CHARACTERISTIC

Q.17) *Explain working of depletion type MOSFET.*
Answer: DEPLETION TYPE MOSFET

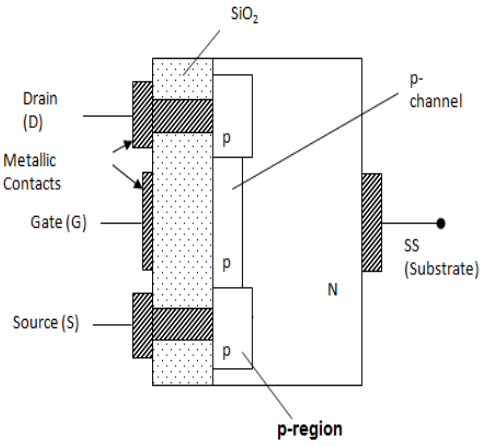


Figure 36:P-Channel MOSFET

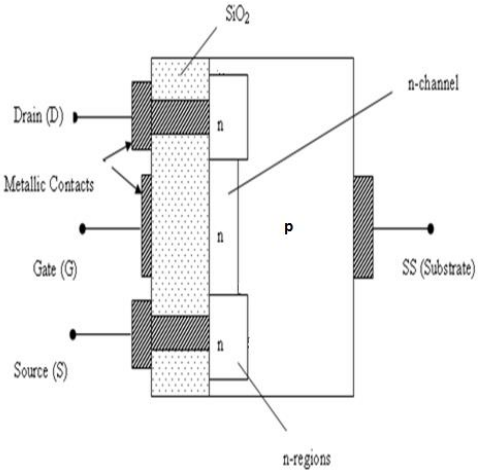


Figure 37:N-Channel MOSFET

Construction:

2 highly doped n (*p*) regions are diffused into a lightly doped p (*n*) type substrate. These 2 doped n (*p*) regions represent **source** and **drain**. **Substrate** is internally connected to **source** terminal. S & D terminals are connected through a metallic contacts to n (*p*) doped regions linked by n (*p*) channel. **Gate** is connected to metal contact but remains insulated from n (*p*) channel by a thin layer of SiO_2.

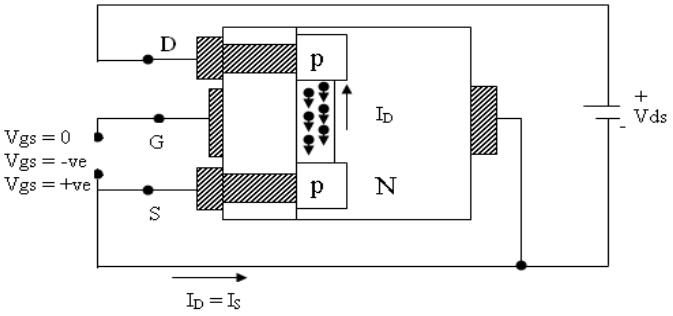


Figure 38:P- Channel

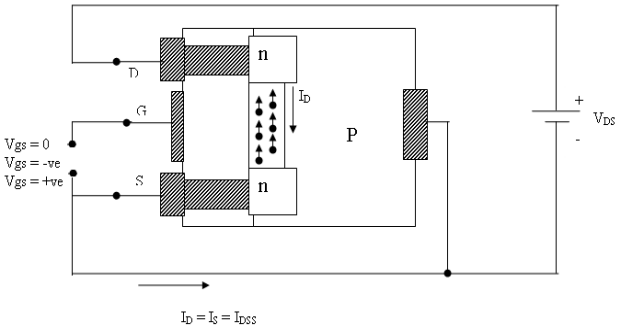


Figure 39:N-Channel

Working (N-Channel):

On application of V_{DS} and keeping V_{GS}=0, then free electrons from n-channel attract towards +ve potential of $V_{DS,}$ which establishes drain current (I_D). When V_{GS}= -ve, the negative charges on gate repel electrons from the channel and attract holes from p-type substrate. Hence there is a recombination between them which reduces drain current. When V_{GS}= +ve, , the positive charges on gate will draw additional electrons from p- substrate, increasing I_D.

Working (P-Channel):

On application of V_{DS} and keeping V_{GS}=0, then holes from p-channel attract towards -ve potential of $V_{DS,}$ which establishes drain current (I_D). When V_{GS}= -ve, the negative charges on gate will draw additional holes from n- substrate, increasing I_D. When V_{GS}= +ve, the positive charges on gate repel holes from the channel and attract electrons from n-type substrate. Hence there is a recombination between them which reduces drain current.

Drain Characteristics

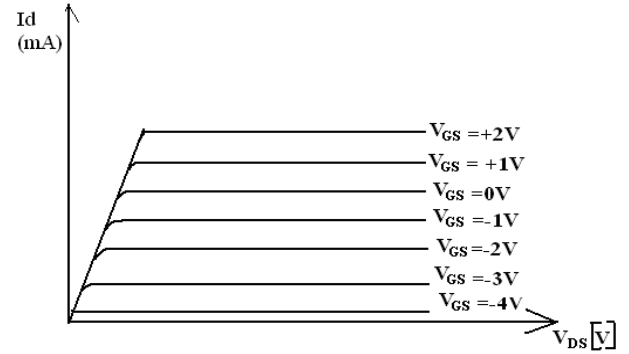


Figure 40: N-Channel

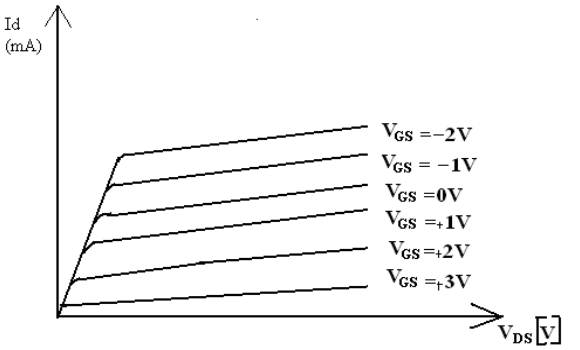
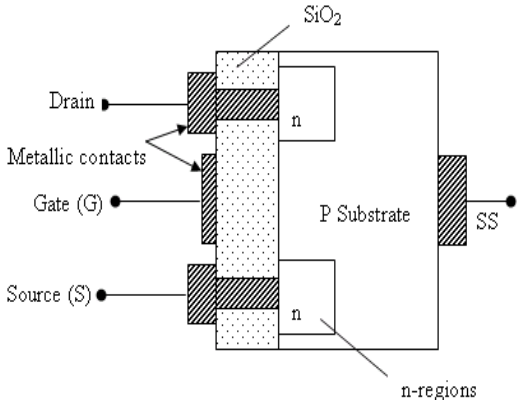


Figure 41:P-Channel

Q. 18) *Explain working of enhancement type MOSFET.*

Answer:

It differs from the depletion MOSFET in that it has no physical channel.



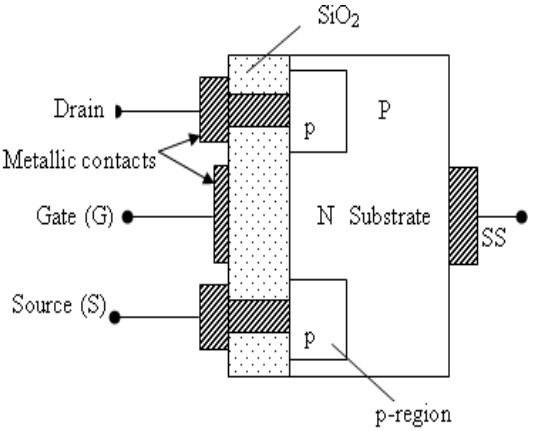


Figure 42:N-Channel Enhancement MOSFET **Figure 43:**P-Channel Enhancement MOSFET

Construction:

2 highly doped n (*p*) regions are diffused into a lightly doped p (*n*) type substrate. These 2 doped n (*p*) regions represent source and drain. Substrate is internally connected to source terminal. The channel between two n (p) region is absent. Gate is connected to metal contact but remains insulated from n (*p*) channel by a thin layer of SiO_2.

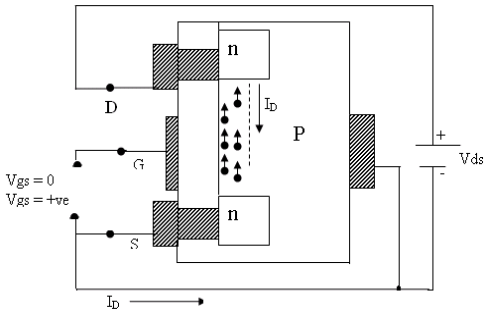


Figure 44:N-Channel Enhancement MOSFET

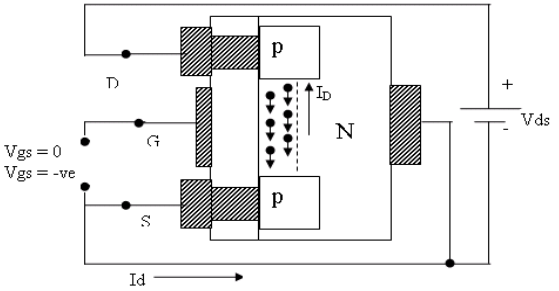


Figure 45:P-Channel Enhancement MOSFET

Working (N-Channel):

On application of V_{DS} and keeping V_{GS}=0, then no current will flow because of absence of channel. When V_{GS}= +ve, , the positive charges on gate will draw additional electrons from p-substrate,which creates an n-channel adjacent to sio_2 layer. Hence conductivity of channel is enhanced by increasing V_{GS}. Hence called enhancement.

Working (P-Channel):

On application of V_{DS} and keeping V_{GS}=0, then no current will flow because of absence of channel. When V_{GS}= -ve, , the negative charges on gate will draw additional holes from p-substrate,which creates an p-channel adjacent to sio_2 layer.

Hence conductivity of channel is enhanced by decreasing V_{GS}. Hence called enhancement

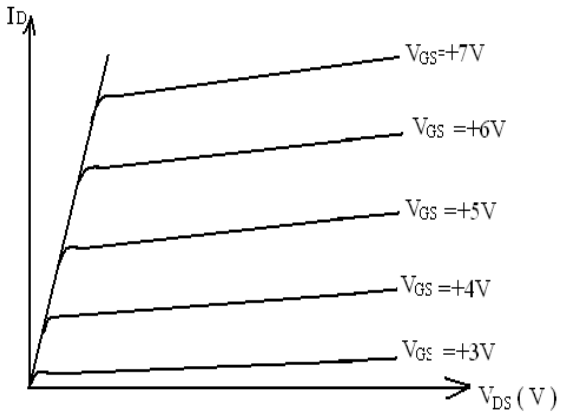


Figure 46:N-Channel Enhancement MOSFET

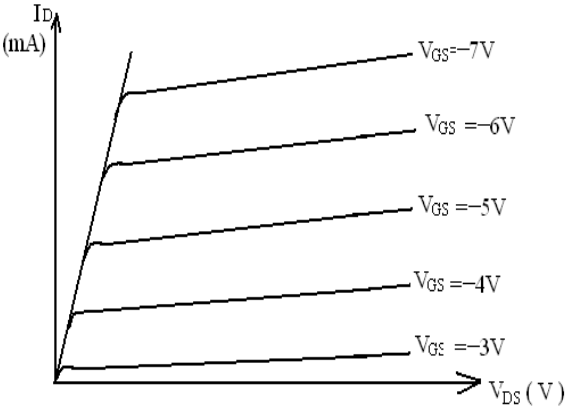


Figure 47:P-Channel Enhancement MOSFET

Q. 19) *How BJT act as an Amplifier?*
Answer:

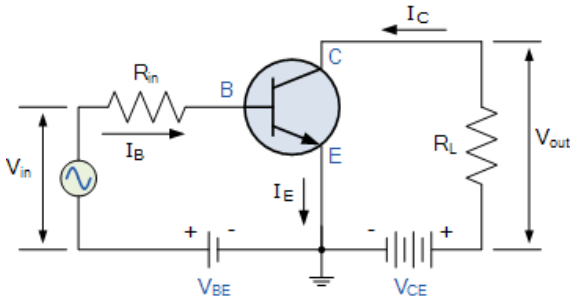


Figure 48: Circuit Diagram

In this type of configuration, the current flowing out of the transistor must be equal to the currents flowing into the transistor as the emitter current is given as Ie = Ic + Ib.
As the load resistance (RL) is connected in series with the collector, the current gain of the common emitter transistor configuration is quite large as it is the ratio of Ic/Ib. A transistors current gain is given the Greek symbol of Beta, (β).

As the emitter current for a common emitter configuration is defined as Ie = Ic + Ib, the ratio of Ic/Ie is called Alpha, given the Greek symbol of α. Note: that the value of Alpha will always be less than unity.

Since the electrical relationship between these three currents, Ib, Ic and Ie is determined by the physical construction of the transistor itself, any small change in the base current (Ib), will result in a much larger change in the collector current (Ic).

Then, small changes in current flowing in the base will thus control the current in the emitter-collector circuit. Typically, Beta has a value between 20 and 200 for most general purpose transistors. So if a transistor has a Beta value of say 100, then one electron will flow from the base terminal for every 100 electrons flowing between the emitter-collector terminals.
Then to summaries a little. This type of bipolar transistor configuration has greater input impedance, current and power gain than that of the common base configuration but its voltage gain is much lower. The common emitter configuration is an inverting amplifier circuit. This means that the resulting output signal has a 180o phase-shift with regards to the input voltage signal

Q. 20) *How BJT act as a switch?*

Answer:

Switching circuits are significantly different than linear circuits. They are also easier to understand. Before investigating more complex circuits, we will begin by introducing discrete solid-state switching circuits: those built around BJTs.

A switch consists of a BJT transistor that is alternately driven between the saturation and cutoff regions. A simple version of the switch is shown in figure 1. When the input equals $-V_{in}$, the base-emitter junction is reverse biased or off so no current flows in the collector. This is illustrated by the load line shown in the figure. When the BJT is in cutoff, the circuit (ideally) has the following values:

$V_{CE} = V_{CC}$ and $I_C = 0$ A

This state is similar to an open switch.

When the input equals $+V_{in}$, the transistor is driven into saturation and the following conditions occur:

$V_{CE} \tilde{} 0V$ and $I_{Csat} = V_{CC}/R_C$

This state is similar to a closed switch connecting the bottom of R_C to ground.

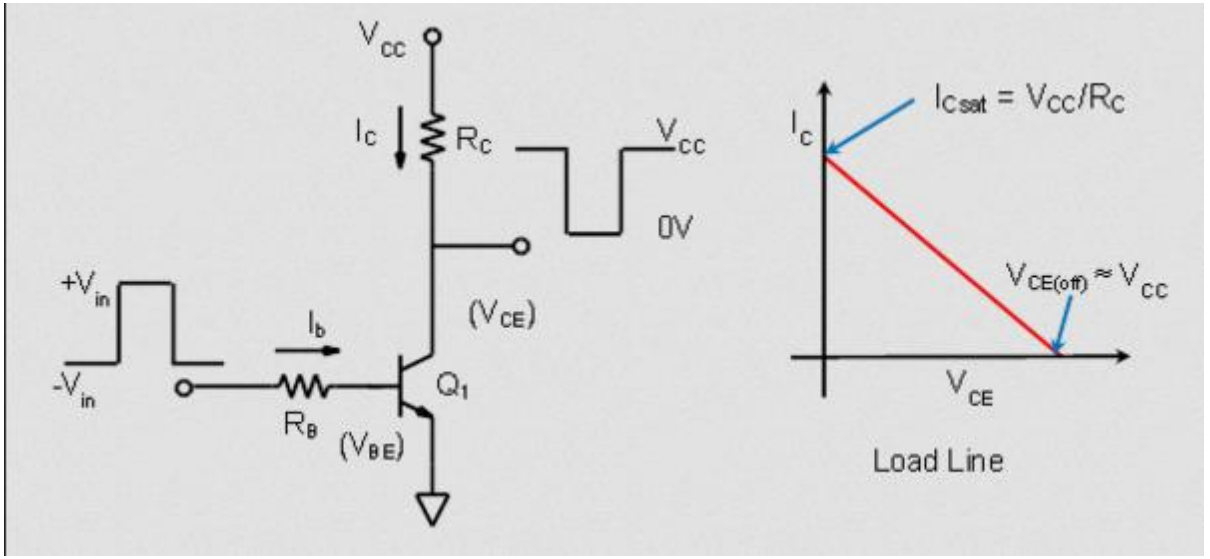


Figure 49: Circuit Diagram

The characteristics for a BJT switch assume that:
$-V_{in}$ is low enough to drive the transistor into cutoff. $+V_{in}$ must produce enough base current through R_B to drive the transistor into saturation. The transistor is an ideal component.
These conditions can be assured by designing the circuit so that:
$-V_{in} = V_{BE}$, $+V_{in} = V_{BE} + I_B R_B$ (V_{CC} is a good maximum), $I_B > I_{Csat}/ß$
Condition 1 guarantees that the circuit is driven into the cutoff region by the input. Conditions 2 and 3 assure that the transistor will be driven into the saturation region.
An actual BJT switch differs from the ideal switch in several aspects. In practice, even in cutoff there is some leakage current through the transistor. Also, in saturation, there is always some voltage dropped across the transistor's internal resistance. Typically, this will be between 0.2 and 0.4 V in saturation depending on the collector current and size of the device. These variations from the ideal are generally minor with a properly sized device, so we can assume near ideal conditions when analyzing or designing a BJT switch circuit.

Reference:

“Electronics Devices and Circuit Theory”, by Robert L. Boylestad, Louis Nashelsky, 10th edition, Pearson Private Limited, Published in 2009.

UNIT NO. 4

***Unit IV* : OPAMP and its application**
Introduction to Op-Amp, Inverting and Non-Inverting Amplifier, Linear Applications of OP-AMP, Comparator.

Q. 1) *What is differential amplifier? Enlist and explain different types of configuration.*
Answer: A differential amplifier is a type of electronic amplifier that amplifies the difference between two voltages but does not amplify the particular voltages.
Differential Amplifier Configuration
1) Dual Input Balanced Output

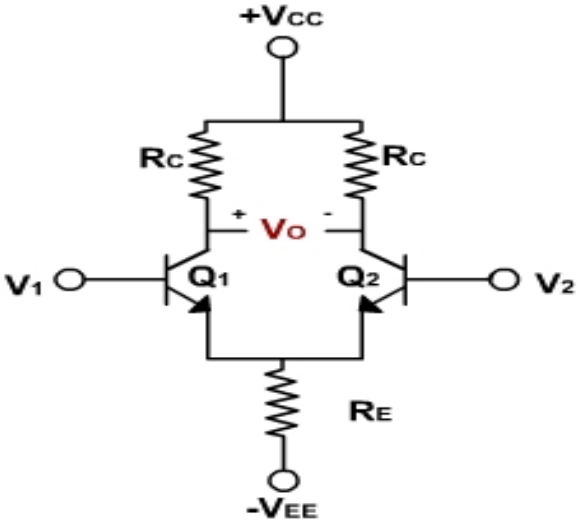


Figure1: Dual Input Balanced Output Differential Amplifier

The circuit is shown in figurehave V1 and V2 as two inputs, applied to the bases of Q1 and Q2 transistors. Theoutput voltage is measured between the two collectors C1 and C2, which are at same dc potentials.
2) Dual Input Unbalanced Output
In this case, two input signals are given however the output is measured at only one of the two-collector w.r.t.ground as shown in fig.

The output is referred to as an unbalanced output because the collector at which theoutput voltage is measured is at some finite dc potential with respect to ground.

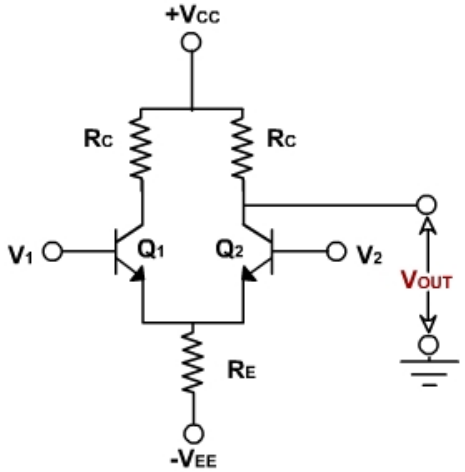


Figure2: Dual Input Unbalanced Output Differential Amplifier

3) Single Input Balanced Output

The circuit is shown in figurehave V1as a single input, applied to the bases of Q1 transistor. Theoutput voltage is measured between the two collectors C1 and C2, which are at same dc potentials.

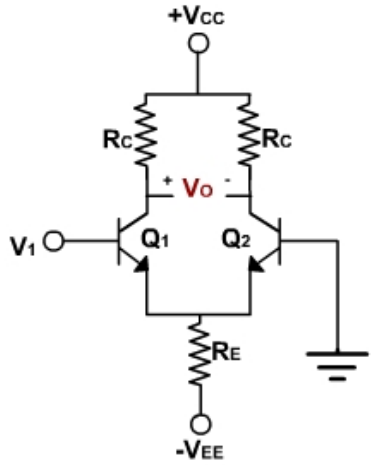


Figure3: Single Input balanced Output Differential Amplifier

4) Single Input Unbalanced Output

In this case, one input signal is given however the output is measured at only one of the two-collector w.r.t.ground as shown in fig.

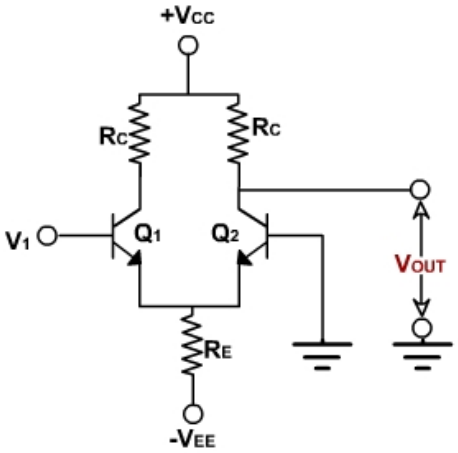


Figure4: Single Input unbalanced Output Differential Amplifier

Q. 2) *Draw and explain Block diagram of OP-AMP.*

Answer:OP-AMPs are available in an integrated circuit form. Commercial integrated circuit OP-AMP usually consists of four cascaded blocks:

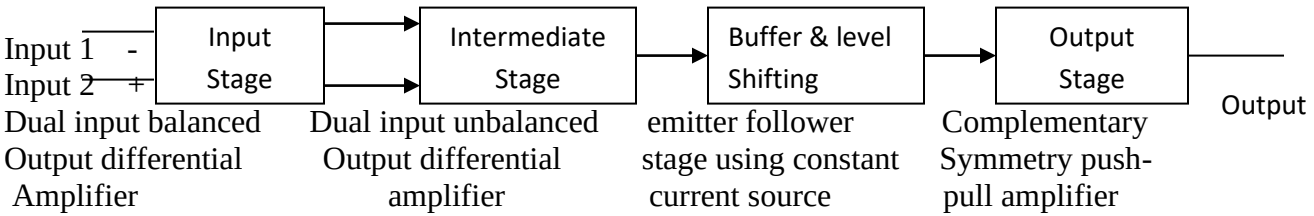


Figure5: Block diagram of OP-AMP

1. Input stage**:** The input stage is the Dual Input Balanced output differential amplifier. The function of the differential amplifier is to amplify the difference between the two input signals. The

differential amplifier has high input impedance. This stage provides most of voltage gain of the amplifier and also establishes the input resistance of the OP-AMP.

2. Intermediate Stage**:** The intermediate stage is usually a differential amplifier with dual input, unbalanced single ended output which is driven by the output of the first stage. The overall gain requirement of the OP-AMP is very high. The input stage alone can not provide such a high gain. The main function of the intermediate stage is to provide the additional voltage gain required.

3. The level shifter stage: Because of direct coupling used, the DC voltage at the output of the intermediate stage is well above ground potential. Therefore, the level shifter stage brings the DC level down to zero volts with respect to ground, when no signal is applied at the input terminals. The buffer is usually an emitter follower whose input impedance is very high. This prevent loading of the high gain stage.

4. Output Stage**:** The basic requirements of an output stage are low output impedance, large AC output voltage swing and high current sourcing and sinking capability. The push-pull complementary amplifier meets these entire requirement and hence used as an output stage. This stage increases the output voltage swing and keeps the voltages swing symmetrical with respect to ground. The stage raises current supply capability of the OP-AMP.

Q. 3) *Explain all ideal characteristics of OP-AMP.*
Answer:

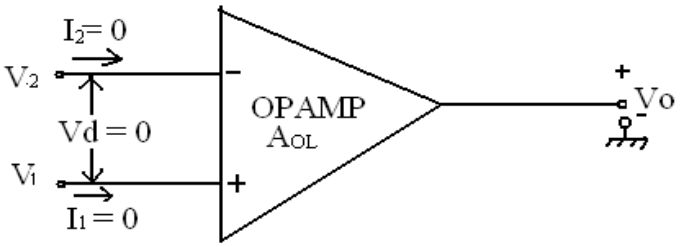


Figure6:OP-AMP

An op-amp would exhibit the following electrical characteristics:

Open – loop voltage gain (A):- When the OPAMP is used without any feedback, the differential voltage gain is known as Open – loop voltage gain.

Ideally A is infinite but practically for good op-amps, it is in the range of 10^3 to 10^5.

Input Impedance (Zin):- It is the impedance across input side.The input impedance is infinite for an ideal OP-AMP. This ensures that no current can flow into an ideal OP-AMP. Typical value is greater than 1 MΩ.

Output Impedance (Zout):- It is the impedance across output side. The output impedance is zero for an ideal OP-AMP. This ensures that the output voltage of OP-AMP remains same, irrespective of the value of the load resistance connected.

Typical value is few hundred ohms.

Input Bias Current (I_B):- It is defined as the current flowing into each of the two input terminals when they are biased to the same voltage levels i.e., when the OP-AMP is balanced. The two bias currents are never same, hence the manufacturers specify the average input bias current I_B which is given as,

$$Ib = \frac{|Ib1| + |Ib2|}{2}$$

Ideally $I_B = 0$, typical value is 80 nA.

Input Offset Current (I_{OS}):- The difference in magnitudes of I_{B1} and I_{B2} is called as input offset current and is denoted as I_{OS}.

Ios = $\left| I_{B1} - I_{B2} \right|$

Ideally $I_{OS} = 0$, typical value is 200 nA.

Input Offset Voltage (Vos):-Whenever both the input terminals of the OP-AMP are grounded, ideally the output voltage should be zero. However, the practical OP-AMP shows a small non zero output voltage. To make this output voltage zero, a small voltage in milivolts is required to be applied to one of the input terminals. Such a voltage makes the output voltage exactly zero. This D.C voltage which makes the output voltage zero, when the other terminal is grounded is called as input offset voltage denoted as Vos.

Ideal value = 0, typical value = 2mV.

Bandwidth (BW):- The range of frequency over which the amplifier performance is satisfactory is called its bandwidth.

The bandwidth of an ideal OP-AMP is infinite i.e., operating frequency range is from 0 to ∞. This ensures that the gain of the OP-AMP will be constant over the frequency range from dc (zero frequency) to infinite frequency. So OP-AMP can amplify DC as well as AC signals.

Typical value = 1 MHz.

Common mode Rejection ratio(CMRR):- The ratio of differential mode gain & common mode gain is defined as CMRR.

CMRR = Ad / Ac

(When the same voltage is applied at both input terminals, the voltage is called common mode voltage V_{CM} and Ac = V_{oCM} / V_{iCM}). Infinite CMRR of an ideal OP-AMP ensures Ac = 0.

Slew Rate (S):- The slew rate is defined as the maximum rate of change of output voltage with time. The slew rate is specified in volts/μsecond.

Thus slew rate = S = dVo/dt Ideally slew rate is infinite; this ensures that the change in the output voltage occurs simultaneously with the changes in the input voltage.

Power Supply Rejection Ratio (PSRR):- It is defined as the ratio of change in input offset voltage due to change in the supply voltage producing it, keeping other power supply voltage constant. It is also called power supply sensitivity (PSV).

PSRR = ΔVos / ΔVcc(due to change in Vcc)

Also PSRR = ΔVos / ΔV_{EE}(due to change in V_{EE})

Ideally it is 0, Typical value 30μV/V

Q. 4) *Explain the concept of virtual ground.*

Answer:

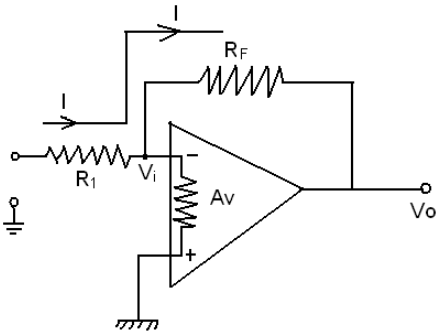


Figure7: Circuit Diagram

For an ideal operational amplifier, since the input resistance is infinite there is no current flow into either input terminals. Hence, the current I through R1 will pass through Rf as shown in figure. The open circuit voltage gain is |A| = infinity (∞) for an ideal operational amplifier.

So $A = \frac{Vo}{Vid} = \infty$ **or**

$$\boldsymbol{Vid = \frac{Vo}{A} = 0}$$

This indicates that the input is effectively shorted and hence it can be said that there exists a *virtual ground*. The meaning of the ordinary ground is that it has zero voltage and can sink infinite current. The term virtual ground means any point in a circuit that has zero voltage and draws no current. So as far as voltage is concerned there is no difference between ordinary ground and virtual ground. But for current ordinary ground can sink infinite current whereas virtual ground draws no current.

For an operational amplifier the input port appears as a short for voltage, and opens for current.Thus the voltage at the non-inverting input terminal of an op amp can be realistically assumed to be equal to the voltage at the inverting input terminal.

The open loop gain, $\boldsymbol{A = \infty}$

$$\boldsymbol{Vid = (Vp - Vn) = 0}$$

$$\boldsymbol{Vp = Vn}$$

Q. 5) *Draw and explain the Inverting amplifier using OP-Amp.*

Answer:

In the inverting amplifier, only one input is applied to the inverting input terminal. The non inverting input terminal is grounded.

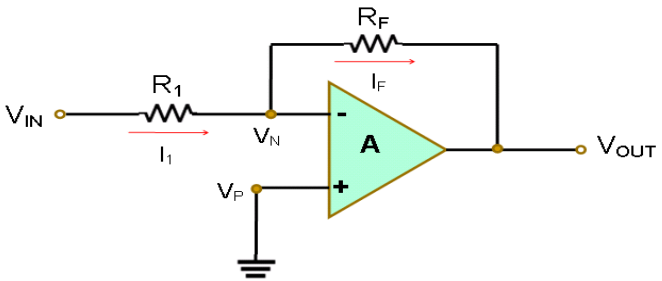


Figure8: Inverting Amplifier

Input is applied to the inverting terminal of OPAMP

According to Virtual ground concept,

$$Vn = Vp = 0$$

As current I_F is flowing from V_N to V_{OUT}

KCL at node V_N,

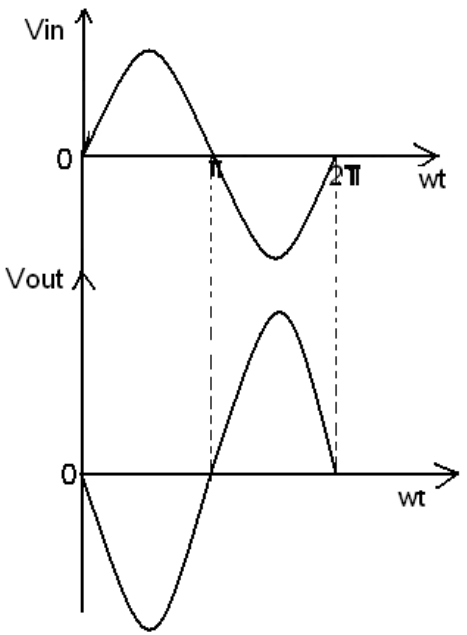
$$I1 = If$$

$$\frac{Vin - Vn}{R1} = \frac{Vn - Vout}{Rf}$$

$$\frac{Vin}{R1} = \frac{-Vout}{Rf}$$

Or

$$\frac{Vout}{Vin} = \frac{-Rf}{R1}$$



$$Vout = -\left(\frac{Rf}{R1}\right) Vin$$

The R_F/R_1 is the gain of the amplifier while negative sign indicates that the polarity of the output is opposite to that of the input. Hence it is called inverting amplifier.

Q. 6) *Draw and explain the Non- Inverting amplifier using OP-Amp.*
Answer:
In this configuration the input is applied to the non-inverting input terminal, and the inverting terminal is connected to ground.

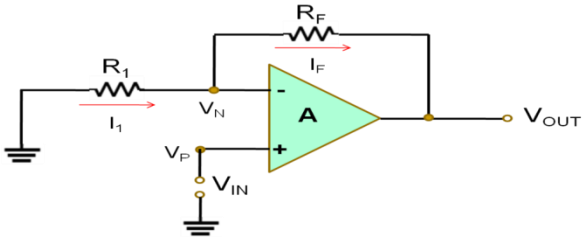


Figure10: Non-Inverting Amplifier

Input is applied to the non-inverting terminal of OPAMP.
According to Virtual ground concept,

$$Vn = Vp = Vin$$

As current $I_F$is flowing from V_N to V_{OUT}
KCL at node Vn,

$$\frac{0 - Vn}{R1} = \frac{Vn - Vout}{Rf}$$

$$\frac{0 - Vin}{R1} = \frac{Vin - Vout}{Rf}$$

$$\frac{Vout}{Rf} = \frac{Vin}{Rf} + \frac{Vin}{R1}$$

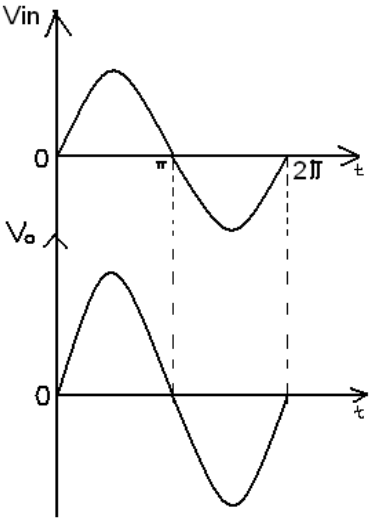


Figure11: Waveform

$$\frac{Vout}{Rf} = Vin\left[\frac{1}{Rf} + \frac{1}{R1}\right]$$

OR

$$\frac{Vout}{Vin} = Rf\left[\frac{1}{Rf} + \frac{1}{R1}\right]$$

$$\frac{Vout}{Vin} = \frac{Rf}{Rf} + \frac{Rf}{R1}$$

$$\frac{Vout}{Vin} = 1 + \frac{Rf}{R1}$$

$$Vout = \left(1 + \frac{Rf}{R1}\right)Vin$$

Gain of the amplifier is $(1+ R_F/R_1)$ & output is in phase with the input.

Q. 7) *Draw and explain summing Amplifier using OP-AMP.*
Answer:
The circuit gives the addition of the applied signals at the output is called summer or adder circuit.

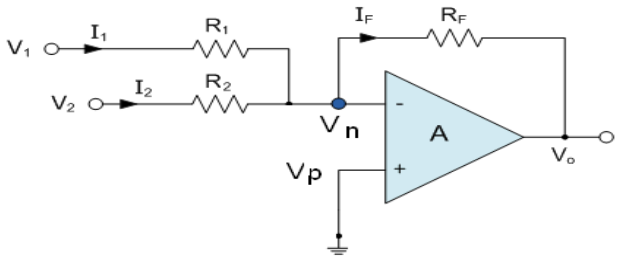


Figure12: Summing Amplifier

According to Virtual ground concept,

$$Vn = Vp = 0$$

As current I_F is flowing from Vn to $Vout$

KCL at nodeVn,

$$I1 + I2 = If$$

$$\frac{(V1 - Vn)}{R1} + \frac{(V2 - Vn)}{R2} = \frac{(Vn - Vout)}{Rf}$$

$$\left(\frac{V1}{R1}\right) + \left(\frac{V2}{R2}\right) = \left(\frac{-Vout}{Rf}\right)$$

Or

$$Vout = -\left[\left(\frac{Rf}{R1}\right)V1 + \left(\frac{Rf}{R2}\right)V2\right]$$

If $R1 = R2 = Rf$, then

$$\boldsymbol{Vout = -(V1 + V2)}$$

The magnitude of the output voltage is the sum of the input voltages & hence circuit is called as summer or adder circuit.

If the inverting summer circuit

$$R1 = R2 = R \quad \& \quad Rf = \frac{R}{2}$$

Then

$$\boldsymbol{Vout = -\frac{(V1 + V2)}{2}}$$

Thus the magnitude of the output voltage is the average of the two input voltages. So circuit acts like an AVERAGER.

Q. 8) *Draw and explain difference Amplifier using OP-AMP.*

Answer:

The circuit gives the subtraction of the applied signals at the output, hence called subtractor or difference amplifier circuit.

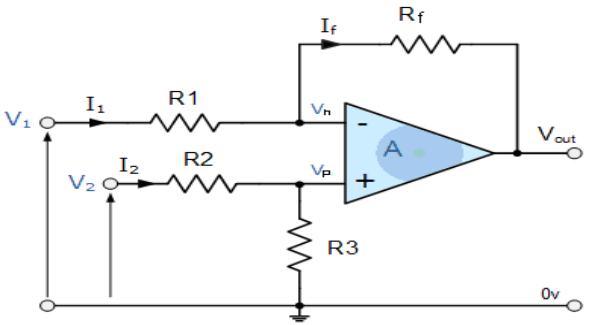


Figure13: Difference Amplifier

1)According to Virtual ground concept,

$$Vn = Vp$$

Applying voltage divider rule at **V_P**

$$Vp = \left[\frac{R3}{(R2+R3)}\right] V2 = Vn$$

2) As current $I_F$is flowing from V_N to V_{OUT}

KCL at V_N

$$I1 = If$$

$$\frac{(V1 - Vn)}{R1} = \frac{(Vn - Vout)}{Rf}$$

$$\frac{\left\{V1 - \left[\frac{R3}{(R2+R3)}\right] V2\right\}}{R1} = \frac{\left\{\left[\frac{R3}{(R2+R3)}\right] V2 - Vout\right\}}{Rf}$$

$$Vout = \left[\frac{R3}{(R2+R3)}\right] V2 - \left(\frac{Rf}{R1}\right)\left\{V1 - \left[\frac{R3}{(R2+R3)}\right] V2\right\}$$

Consider$R2 = R3 = Rf = R1 = R$

Therefore

$$\boldsymbol{Vout = V2 - V1}$$

The magnitude of the output voltage is the subtraction of the input voltages & hence circuit is called as Subtractor circuit.

Q. 9) *Draw and explain Integrator using Op-amp. Also derive the expression for output voltage.*

Answer:

A circit in which the output voltage waveform is the integral of the input voltage waveform is called as integrator.

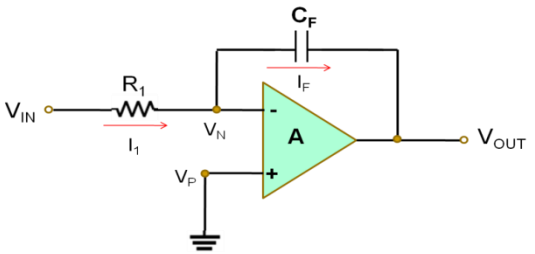
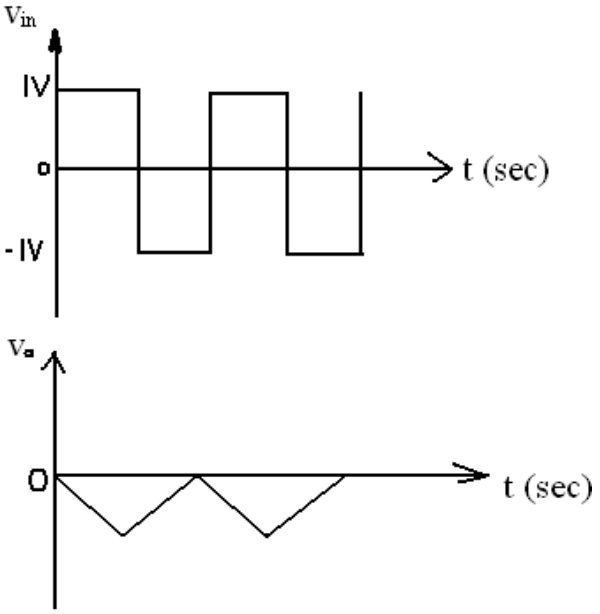


Figure14: Integrator Circuit

Such a ckt is obtained by using a basic inverting amplifier configuration. Here the feedback resistor R_F is replaced by a feedback capacitor C_F.



According to Virtual ground concept,

$$Vn = Vp = 0$$

As current $I_F$is flowing from V_N to Vout

KCL at V_N

$$I1 = If$$

also current flowing through capacitor is

$$Ic = C\frac{dVc}{dt}$$

$$\text{Therefore, } \frac{(Vin - Vn)}{R1} = Cf\left(\frac{d}{dt}\right)(Vn - Vout)$$

$$\frac{Vin}{R1} = Cf\left(\frac{d}{dt}\right)(-Vout)$$

Integrating both sides with respect to time,

$$\int_0^t \frac{Vin}{R1}dt = \int_0^t Cf\left(\frac{d}{dt}\right)(-Vout)\,dt$$

$$= Cf(-Vout)$$

$$\boldsymbol{Vout = -\frac{1}{(R1Cf)}\int_0^t Vin\,dt}$$

The last equation indicates that the output voltage is inversely proportional to the negative integral of input voltage and inversely proportional to time constantR_1C_F.

Q. 10) *Draw and explain differentiator using Op-amp.Also derive the expression for output voltage.*

Answer:

The circuit performs the mathematical operation of differenciation. i.e output waveform is a derivative of input waveform.

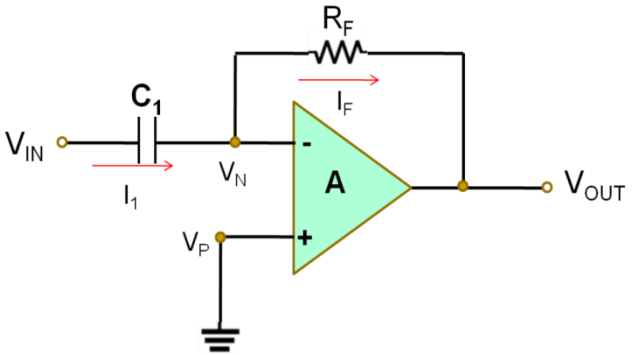


Figure16: Differentiator Circuit

It may be constructed from a basic inverting amplifier if an input resistor R_1 is replaced by a capacitor C_1.

According to Virtual ground concept,

$$Vn = Vp = 0$$

As current I_F is flowing from V_N to V_{OUT}

KCL at V_N

$$I1 = If$$

$$C1\left(\frac{d}{dt}\right)(Vin - Vn) = \frac{(Vn - Vout)}{Rf}$$

$$C1\frac{d}{dt}(Vin) = -\frac{Vout}{Rf}$$

$$\boldsymbol{Vo = -RfC1\frac{dVin}{dt}}$$

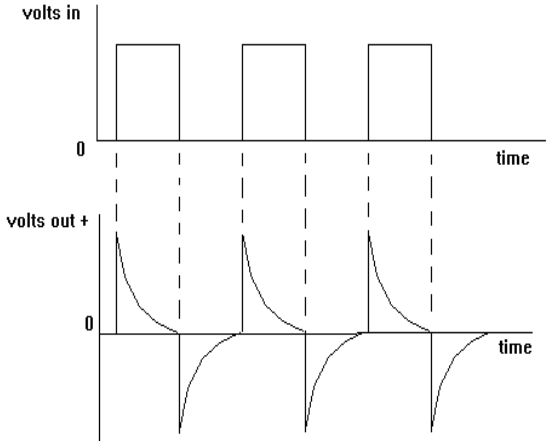
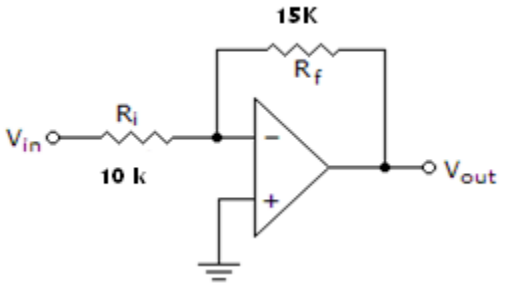


Figure17: Waveform

Q. 11) *What is the range of the output voltage in the circuit of fig. if the input varies from 0.1 to 0.5V and Ri is raised by 50%?*



Answer: Given Circuit is Inverting Amplifier so the output voltage is given by-

Vo = -(Rf/Ri) * Vin
Given = Rf = 15 k, Ri = 10K
For Vin = 0.1 V and Ri = 10 k
Vo = -(15 k / 10 k) * 0.1 = -0.15 V
For Vin = 0.5 V and Ri = 15 K
Vo = -(15 k/15 k) * 0.5 = - 0.5 V

Range of Output Voltage is = -0.1 V to -0.5 V

Q. 12) *Calculate the output voltage of summing amplifier for the following set of inputs V1 = 200mV , V2= 400mV, V3= 800mV, R1 = 20K, R2= 40K and R3 = 80K. R1,R2 and R3 are the corresponding resistors of V1,V2 and V3. All the voltages are applied at the inverting terminal*

Answer: Output Equation of Summing Amplifier is

Vo = -(Rf/R1 *V1 + Rf/R2 * V2 + Rf/R3 * V3)
Consider Rf = 20 K
Vo = -(20 /20 *200 m + 20 / 40 * 400m + 20/80 * 800 m)
Vo = - 600 mV

Q. 13) *For a given op-amp, CMRR=105 and differential gain Ad=105. Determine common-mode gain Acm of the op-amp.*

Answer: CMRR = 105, Ad = 105, Acm=?

CMRR = Ad/Acm
Acm = Ad / CMRR
Acm = 105 / 105 = 1

Q. 14) *The voltage applied at the non-inverting terminal is 5V and at the inverting terminal is 0V with the feedback resistance of 7K and input resistance of 5K then find the value of output voltage.*

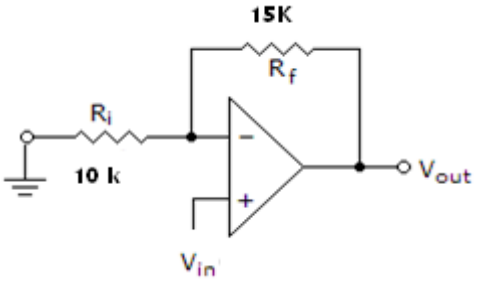
Answer: Vp = 5V, Vn = 0 V, Rf = 7 K, Ri = 5K

Vo = (1 + Rf/R1) * Vin

Vo = (1 + 7/5) * 5

Vo = 12 V

Q. 15) *What is the range of the output voltage in the circuit of fig. if the input resistance is a potentiometer that varies from 10k to 20K and Vin is 1V?*



Answer: Given circuit is Non -Inverting Amplifier

Vo = (1 + Rf/Ri) * Vin

Rf = 15k, Vin = 1V

For Ri = 10 K

Vo = (1+15/10) * 1 = 2.5 V

For Ri = 20 K

Vo = (1 + 15/20) * 1 =1.75 V

Range of output voltage 2.5 V to 1.75 V

Q. 16) *A Differential dc amplifier has a differential mode gain of 100 and a common-mode gain 0.01. What is its CMRR in dB?*

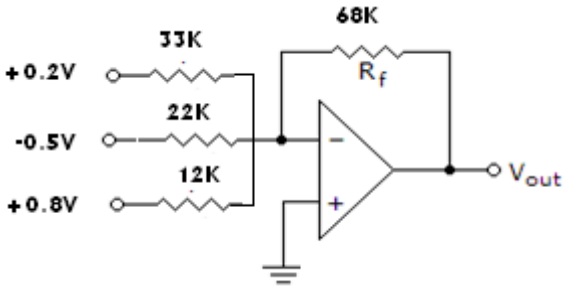
Answer: CMRR = ? , Ad = 100, Acm = 0.01

CMRR = Ad/Acm

CMRR = 100/0.01 =10000

CMRR in dB = 20 log 10000 = 80

Q. 17) *Find the output Voltage of the Following circuit.*



Answer:Output Equation of Summing Amplifier is

Vo = -(Rf/R1 *V1 + Rf/R2 * V2 + Rf/R3 * V3)

Rf = 68 K

Vo = -(68k/33k *0.2 + 68k / 22k * -0.5 + 68k/12k * 0.8)

Vo = -3.402V

Reference:

"OP-AMP and Linear Integrated Circuit", by Ramakant A. Gayakwad, Prentice Hall India Learning Private Limited, Published in 2002.

UNIT NO. 5

Unit V: Measurement and Instruments
Introduction, Important terms in measurement such as accuracy, precision, sensitivity, Types of errors & their sources, Static & dynamic characteristics of measurement system, Bridges - Wheatstone bridge, Maxwell Bridge, Schering bridge, Meters- Ammeter, Voltmeter and Multimeter.

Q.1) *Define the following:*
i. *Arithmetic Mean*
ii. *Dispersion from Mean*
iii. *Deviation*
iv. *Average Deviation*
v. *Standard Deviation*
vi. *Range*
vii. *Variance*

Ans:

Arithmetic Mean:

It is defined as sum of all the measured variable divided by total number of reading. Thus,

$$X' = (x1+x2+x3....+xn)/n$$
$$= \sum x/n$$

Dispersion from Mean:

Dispersion means the extent of which the values are dispersed about the central value.
This is also termed as spread or scatter.

Deviation:

Deviation is departure of the observed reading from arithmetic mean of the group of reading.
Let deviation of reading x1 is d1, x2 is d2 and so on....
Then
$X' = \sum(xn-dn)/n$
Algebraic sum of deviation is zero.

Average Deviation :

Average deviation is defined as sum of the absolute value of deviation divided by number of reading.
$= \sum d/n$

Standard Deviation :

It is defined as square root of sum of individual deviation squared, divided by number of reading.

$S.D=\sigma= \sqrt{((d1^2+d2^2+----+dn^2)/n)}$

$= \sqrt{\sum d^2/n}$

Variance:

The variance is mean square which is same as SD except the square root is not extracted.

Thus V=(SD)^2

$=\sum d2/n$

Range: It is defined as the difference between greatest and least value of data.

Q.2) *Draw and explain Wheatstone Bridge.*

Ans:

Wheatstone Bridge is the very important device used in measurement of medium resistance. It is one of the widely used instrument in industry because of it's accuracy and reliability.

The principle operation of working of wheatstone bridge is "NULL INDICATION". According to this principal the voltage difference at two end of node will be zero. Moreover the indication is independent of the calibration of null indicating instrument or any of it's characteristics. That's why very high degree of accuracy can be achieved using wheatstone bridge. The accuracy achieved by this bridge is 0.1% which is far more than the accuracy of any ordinary ohmmeter which is used for measurement of medium resistance.

The circuit diagram of the bridge is as shown below.

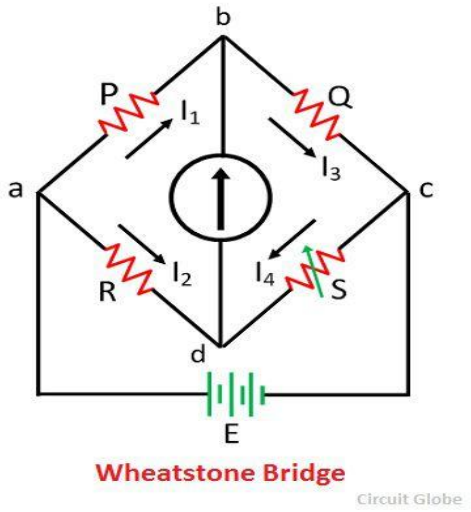


Figure 1: Circuit diagram of Wheatstone Bridge

From the circuit diagram it is seen that the bridge consist of 4 arms P,Q,R and S, where R is the unknown resistance to be measured S is the potentiometer and P and Q are predefined resistance and is termed as ratio arm. A battery source E is applied across the circuit with a null detector between node b and d. Now according to the principal of Null indication the potential difference across the galvanometer must be zero.
i.e. the voltage across ab= voltage across ad
Thus for balancing the bridge

I1P=I2R----------(1)

For Galvanometer current to be Zero

I1=I3=E/(P+Q) ----------(2)

I2=I4=E/(R+S) –----------(3)

Now From 1,2, & 3

P/(`P+Q)=R/(R+S)

$P(R+S)=R(P+Q)$
$PR+PS=RP+RQ$
$QR=PS$
Thus
$R=S*(P/Q)$

Thus the working of bridge can be summarized as when the unknown resistance R is applied across the bridge the null detector show some reading as the bridge is unbalanced. Thus we will adjust the potentiometer S which is a variable resistance till the bridge is balanced and the null detector shows zero output. This can be achieved very easily since resistance P and Q are constant.

Sensitivity of Whetstone Bridge

The Galvanometer is slightly unbalanced so that the current flow in the galvanometer branch of bridge network. Due to this reason the following point need to be considered:

i. Selecting a Galvanometer with which a given unbalance may be observed in a specific bridge arrangement
ii. Determining the minimum unbalance which can be observed with a given galvanometer in the specified bridge arrangement
iii. Determining the deflection to be expected for a given unbalance

Thus the sensitivity to unbalance can be computed by solving the bridge for small unbalance.
For this purpose the bridge is converted to "Thevenin Equivalent" circuit.
In balance condition,
$P/Q=R/S$
Now if the R is changed to $R+\Delta R$,
Then bridge will be unbalanced and the Galvanometer shows some deflection
This occur due to voltage drop between point a and b
Let
$Eab=I1P$
$=EP/(P+Q)$
Similarly
$Ead=I2(R+\Delta R)$
$=E(R+\Delta R)/ R+\Delta R+S$
Thus the voltage difference is
$E=Eab-Ead$
$=E(((R+\Delta R)R+\Delta R+S)-P/(P+S))$

As P/P+Q=R/R+S
=ES ΔR/(R+s)^2+ ΔR(R+S)
~EES ΔR/(R+S)^2

As ΔR(R+S)<<(R+S)^2
Thus deflection of galvanometer with voltage sensitivity Sv is given by
Θ=Sve=SvES ΔR/(R+S)^2

Q.3) *Draw and explain Maxwell induction Bridge.*
Ans:

Maxwell bridge circuit is a type of AC bridge which is used for measurement of inductance. The AC bridge consist of 4 arms, a source of excitation and a balance detector. In this bridge each of the 4 arms is an impedance. Along with that the ac source is provided and the balance detector is sensitive to small alternating potential difference.

The various application where this bridge is used is communication system and complex electronic circuit like phase shifting, filtering out undesirable signal, measuring frequency of audio signal, providing feedback for oscillator and amplifier.

This bridge circuit is as shown in figure.

Where
Z1 consist of
L1= unknown Inductance of resistance R1
L2=Variable Inductance of Resistance r2
R2=Variable resistance connected in series with inductor L2
R3,R4=known non inductive resistance

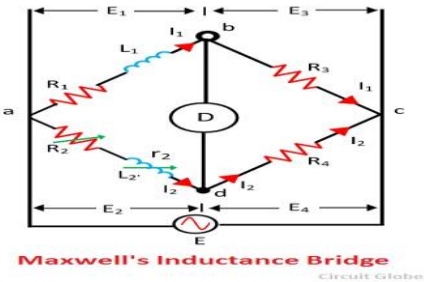


Figure 2: Circuit Diagram of Maxwell's Inductance Bridge

The circuit diagram is similar to wheat stone bridge only the resistance is replaced by Impedance, Galvanometer by detector which is sensitive to small potential difference and DC source to AC source.

Now The working principal of the Bridge is it should be balance

i.e. Z1Z4=Z2Z3

Z1=R1+jwL1

Z2= R2+jwL2

Z3=R3

Z4=R4

(R1+jwL1)R4=(R2+jwL2)R3

R1R4+jwL4R4=R2R3+jwL2R3

Equating Real part

R1R4=R2R3

R1=R2R3/R4

Equating Imaginary part

jwL1R4=jwL2R3

L1R4=L2R3

L1=L2R3/R4

Q. 4) *Draw the block diagram and explain the working principal of Digital Multi meter.*

Ans:

Introduction to Digital Multi meter

Digital multi meter is one of the widely used instrument in laboratory. It is used to measure AC Voltage DC Voltage, AC Current, DC Current and Resistance. The display unit is dital and hence the accuracy of this multi meter is very high. The input resistance of this multi meter is very high which is again one of the advantage of this instrument. It provide the range and selection of operation to be performed in very easy and compatible way and hence has become most popular and widely used in various application along with laboratory.

The Block Diagram of Digital Multi meter is as shown below:

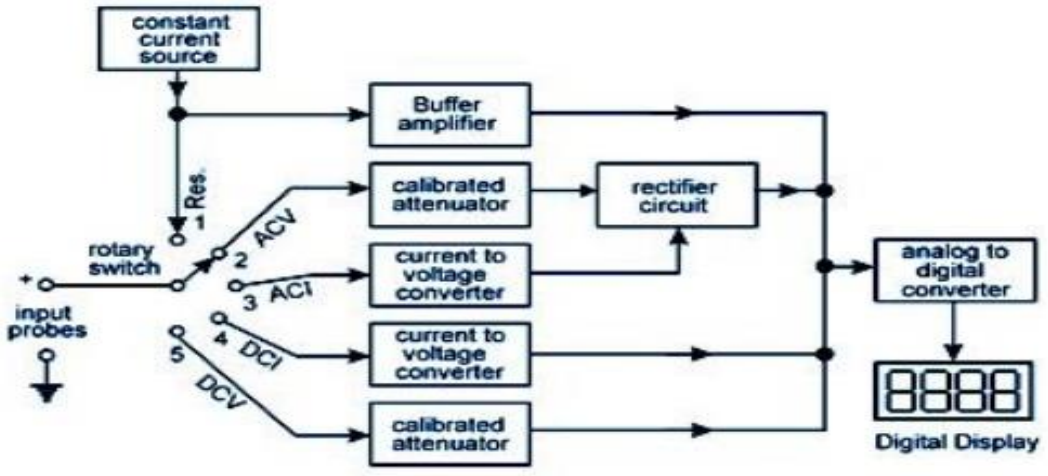


Figure 3: Block diagram of Digital Multimeter

Working of Digital Multi meter

A digital multi meter consists of a rotary switch at the i/p side. This switch is connected to 5 probes which are

Probe 1: Resistance (Buffer Amplifier)
Probe 2: AC Voltage (Calibrated Attenuator)
Probe 3: AC Current (Current to Voltage Convertor)
Probe 4: DC Voltage (Calibrated Attenuator)
Probe 5: Dc Current (Current to voltage convertor)

The 5 different probes are connected to various blocks and switch the multi meter to measure various parameters as chosen. The constant current source is applied to the entire circuit. The signal after processing is given to analog to digital convertor at the output side. This convertor convert the signal in digital output and is given to digital counter circuit which is connected to digital display. The final value of measured quantity is shown on this display which is digital in nature and hece accurate and reliable.

How to measure Resistance?

Keep the switch on Probe 1. Now connect the Resistance across the input probes. As resistance do not have any polarity any probe can be connected to any side of resistance. Now as the current from constant current source flows through the resistor, according to ohm law(V=IR) the voltage is produced across it which is directly proportional to it's resistance. This voltage is given to A-D convertor and thus the final output is shown on the digital display.

How to measure AC Voltage?

Keep the rotary switch to Probe 2. Connect the AC voltage across the input probe. If this voltage is above the selected range then it is attenuated first by calibrated attenuator. As this is an AC Voltage hence it is needed to be converted into DC as the output is digital in nature. Thus the rectifier circuit converts it into DC voltage which is given to A-D Convertor and shown on the digital Display.

How to measure AC Current?

Keep the rotary switch to Probe 3. Connect the AC current across the input probe. Here the current is converted to voltage using current to voltage convertor for further processing. As this is again an AC Voltage it is needed to be converted into DC as the output is digital in nature. Thus the rectifier circuit converts it into DC voltage which is given to A-D Convertor and shown on the digital Display.

How to measure DC Current?

Keep the rotary switch to Probe 4. Connect the DC current across the input probe. Here the current is converted to voltage using current to voltage convertor for further processing. As this is DC Voltage it is not needed to be converted and hence directly given to A-D Convertor and shown on the digital Display

How to measure DC Voltage?

Keep the rotary switch to Probe 5. Connect the DC voltage across the input probe. If this voltage is above the selected range then it is attenuated first by calibrated attenuator. As this is an DC Voltage hence it is not needed to be converted and is directly given to A-D Convertor and shown on

the digital Display.

Q.5) *Draw the block diagram and explain the working principal of True RMS Voltmeter.*
Ans:

Complex waveform like sine wave, square wave or saw tooth wave are measured with a true RMS reading voltmeter. In this voltmeter Thermo couple are used. The working principal of thermo couple is when temp is increased or given at the junction the voltage is obtained. The Block Diagram is as follow:

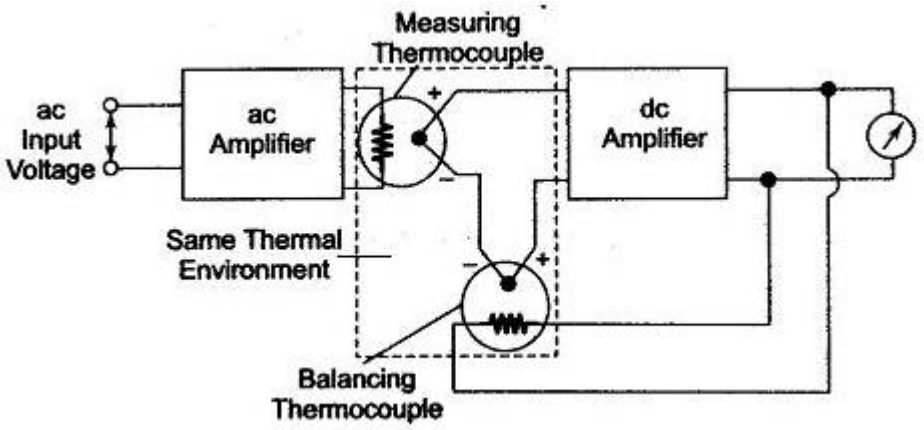


Figure 4: True RMS Voltmeter

From block diagram it is seen that, it consists of two thermocouple, Measuring Thermocouple and Balancing Thermocouple. Initially when the I/P is zero i.e. no waveform is applied and the voltage is zero. But when the I/P is applied, due to flow of current the temperature increase and the voltage is produced at the O/P. This voltage V1 is given to DC amplifier which amplifies the voltage and feed back to the heater of balancing Thermocouple. Thus there is the difference in the voltage of measuring Thermocouple and balancing thermocouple which is given as:-

$Vo=A(V1-V2)$

The balancing thermocouple increase the voltage till the voltage of both the coupler is equal and the bridge is balanced. Thus the DC feedback current is equal to the ac current in the I/P thermocouple. This DC current is directly proportional to the RMS value of I/P voltage. It is indicated on DC voltmeter.

Derivation:

$Vo=A(V1-V2)$

Where,

A= Voltage Gain
V1-V2=Vo/A which is approximately equal to 0
A is very large for high gain amplifier
Thus
V1=V2
Thus, KVrms=KVo^2
Vrms=Vo

Crest Factor

A typical laboratory rms voltmeter provide accurate rms reading of complex waveform having crest factor of 10/1. Thus 10% of full scale meter deflection, where there is less change of amplifier saturation, waveform with crest factor as high as 100/1 can be accommodated.

Thus voltage in range of 100μV to 300V within a frequency range of 10Hz to 10MHz is measured with accurately with instrument.

Q. 6) *Draw and explain Schering Bridge.*
Ans:

Schering bridge circuit is a type of AC bridge which is used for measurement of capacitance. The AC bridge consist of 4 arms, a source of excitation and a balance detector. In this bridge each of the 4 arms is an impedance. Along with that the ac source is provided and the balance detector is sensitive to small alternating potential difference.

The various application where this bridge is used is communication system and complex electronic circuit like phase shifting, filtering out undesirable signal, measuring frequency of audio signal, providing feedback for oscillator and amplifier.

This bridge circuit is as shown in figure.

In this bridge :
Z1 consist of C1 7 r1(In series)
Z2 consist of C2
Z3 consist of R3
Z4 consist of variable C4 and R4(In Parallel)
The Circuit diagram is as shown below.

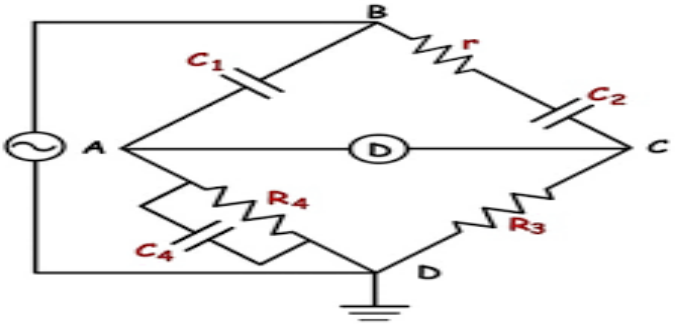


Figure 5: Circuit Diagram of Schering Bridge

Let
C1=Capacitor whose capacitance is to be determined
r1= a series of resistance representing the loss in capacitor C1
C2=A standard capacitor which is loss free
R3=Non Inductive Resistance
C4= Variable Capacitor
R4=Variable non inductive resistance in parallel with variable capacitor C4
At balance,
Z1Z4=Z2Z3
Z1=R1+1/jwC1
Z2=1/jwC2
Z3=R3
Z4=R4/(1+jwC4R4)
Thus
(R1+1/jwC1)(R4/(1+jwC4R4)=1/jwC2*R3
(R1+1/jwC1) R4=(R3/jwC2)*(1+jwC4R4)
R1R4+R4/jwC1=R3/jwC2+R3C4R4/C2

Equating Real Terms
R1R4=R3C4R4/C2
R1=R3C4/C2

Equating Imaginary part
R4/C1=R3/C2
C1=C2R4/R3

Q. 7) *Define Error. Explain the various types of Error.*

Answer:

Error:

It is define as difference between actual vale and measured value of the quantity. This difference is term as error and it occur due to various factor.

These are classified as:

Gross Error:

This type of error occur due to human mistake and is called as Gross error. This type of error include Mistake in Reading Instrument, Mistake in Recording, Calculating measurement Result etc.

For ex. A measuring unit record show 31.5 C and human may record 21.5 C. The human may read 28.5 and record 25.8. Even this error may occur like observer told 30.6 and the person who is recording the data may record 31. These type lead to change in final output though recorder seems to be correct.

Gross error may be of any amount and their mathematical analysis is impossible. However gross error can be avoided by adopting two ways:

i. Great care should be taken in reading and recording the data.
ii. 2-3 or even more reading should be taken off the quantity under measurement.

Systematic Error:

This type of error is divided in 3 types

Instrumental Error:

This error occur due to malfunctioning or fault in designing of measuring unit. This error arrived due to 3 main reason:

Inherent Short coming of Instrument:

This occur due to mechanical structure, construction, calibration or operation of instrument or measuring device. These error may cause instrument to read too low or to high

For ex. If the spring of permanent magnet instrument has become week then the instrument will always read high. These error may also caused because of friction, hysteresis, or even gear backlash.

These error can be overcome or reduce by

i. Adopting the careful plan measurement procedure
ii. Substitution method, calibration against standard
iii. correction factor should be applied after determining instrumentation error
iv. The instrument may be recalibrated carefully

Misuse of Instrument:

This error occurs due to fault of operator. When the operator is having less knowledge about the measuring unit or illiterate, in that case though the instrument is proper there will be mistake in handling of the measuring instrument.

For example misuse of instrument may be failure to adjust the zero of the instruments, poor initial adjustment, using leads to high resistance etc. However the above improper practice may not cause permanent damage of instrument but at the same time cause error.

If the instrument is been used contrary to manufacture instruction and specification in that case not only error but a permanent damage of the instrument may occur because of overheating and overloading. Many a time it leads to instrument failure or even system failure.

This can be overcome by giving proper training and knowledge to the person using that instrument.

Loading Effect:

When the improper use of instrument is being done at the initial level then loading effect error occurs.

For example a well calibrated voltmeter may give a misleading voltage reading when connected across a high resistance circuit and the same voltmeter when connected in a low resistance circuit may give a more dependable reading.

It is generally seen that instrument will give more accurate and reliable result when the loading effect is properly vanished.

Environmental Error:

These error occur due to surrounding area of instrument. This may include temperature, pressure, humidity, dust, vibration, or of external magnetic or electrostatic.

The steps to eliminate these error are:

1. Arrangement should be made to keep external condition constant as much as possible.
2. Using equipment which is immune to external parameter.
3. Employing technique which eliminate the effects of these disturbance
4. In case it is suspected that external magnetic and electrostatic field can effect the reading of instrument, magnetic and electrostatic shield must be provided.

5. Applying computed correction: Efforts are made to avoid use of computed correction but whenever needed they must be incorporated.

Observational Error:

The main type of Observational error is PARALLEX effect. This effect will occur when the line of vision of the observer is not exactly above the pointer.

To avoid this error, highly accurate meter are needed with mirrored scales(Which minimize the error to very small extent). When the pointer image appear hidden by the pointer, observer eye is directly in line with the pointer. This error can also be eliminated by having the pointer and scale in same plane.

The other type of observational error are, sensing capability of individual observer which affect the accuracy of measurement. For example: one observer may tend to anticipate the signal and read too soon. Different observer may produce different result.

Modern electrical instrument have digital display of output which completely eliminates the error on account of human observational or sensing power as the output is in form of digits.

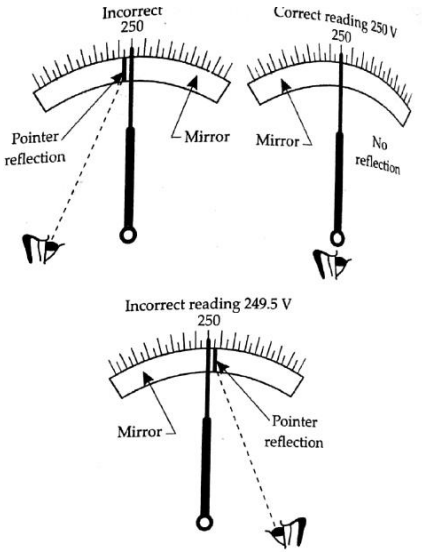


Figure 6: Example of Parallax Error

Random Error

It has been consistently found that experimental result show variation from one reading to other even after all systematic error have been accounted. These errors are due to multitude of small

factor which changes or fluctuates from one measurement to other. These quantity being measured is affected is affected by many happenings throughout the universe. This occurs due to magnetic field, longitude and various factors. These happing or disturbances are lumped together and called as Random or residual error.

Q. 8) *Define Various Static Characteristic of Measurements.*

Ans:

Static Characteristics:

The set of criteria defined for the instrument which are used to measure the quantity which are slowly changing with time. These are mostly termed to be constant and is called as static characteristics.

The various static characteristics are:

Accuracy:

It is the degree of closeness with which the reading approach the true value of quantity to be measured.

It can be expressed as:-

Point Accuracy: Specified at only one particular point

Output accuracy of scale span: Express in the range of scale

Output accuracy of True value: Specify in term of true value

Precision: It is measured of Reproducibility i.e. given fixed value of quantity.

It is composed of two characteristics.

a. Conformity
b. Number of Significant

Sensitivity:

It is define as the smallest change in the measured variable to which the instrument respond. It is defined as the ratio of change in the output of an instrument to a change in value of quantity to be measured.

Reproducibility:

It is the degree of closeness with which a given value may be repeatedly measured. It is specified in termsof scale reading over a given period of time.

Repeatability:

It is defined as the variation of scale reading which are random in nature.

Resolution:

If the input is slowly increased from some arbiter input value, it will again be found that output does not change at all until a certain increment is exceeded. This increment is called Resolution.

Stability:

It is the ability of instrument to retain its performance throughout is specified operating life.

Q. 9) *Given Values: x1=49.7, x2=50.1, x3=50.2, x4=49.6, x5=49.8*
Then calculate i. Arithmetic Mean ii. Deviation from mean iii. Average Deviation iv. Std. Deviation
Answer:

Arithmetic mean:

x'=(x1+x2+x3+x4+x5)/5
=(49.7+50.1+50.2+49.6+49.8)/5
= 249.4/5
=49.88

Deviation from mean:

d1=x1-x'=49.7-49.88=-0.18
d2=x2-x'=50.1-49.88=0.22
d3=x3-x'=49.6-49.88=-0.28
d4=x14-x'=50.2-49.88=0.32
d5=x5-x'=49.8-49.88=-0.08

Sum of deviation:=d1+d2+d3+d4+d5
=-0.18+0.22-0.28+0.32-0.08
=0

Average Deviation: ∑|d|/n
=(0.18+0.22+0.28+0.32+0.08)/5
=0.216

Standard Deviation: ((∑d^2)/n-1)^0.5
=((0.18^2+0.22^2+0.32^2+0.28^2+0.08^2)/4)^0.5
=0.25884

Variance: V=S^2=(0.25884)^2
=0.066998

Arithmetic Mean: 49.88
Deviation from mean: 0
Average Deviation :0.216
Std. Deviation: 0.25884
Variance: 0.066998

Q. 10) *Six experimenters gave a set of independent voltage measurement as 12.8 V, 12.2 V, 12.5 V, 13.1 V, 12.9 V and 12.4 V.*
Calculate :—
(i) The arithmetic mean. (ii) Deviation from the mean.
(iii) The average deviation. (iv) Standard deviation. (v) Variance.
Answer:

Arithmetic mean:

x'=(x1+x2+x3+x4+x5+x6)/6
=(12.8+12.2+12.5+13.1+12.9+12.4)/6
=75.9/6
=12.65

Deviation from mean:

d1=x1-x'=12.8-12.65=0.15
d2=x2-x'=12.2-12.65=-0.45
d3=x3-x'=12.5-12.65=-0.15
d4=x4-x'=13.1-12.65=0.45
d5=x5-x'=12.9-12.65=0.25
d6=x6-x'=12.4-12.65=-0.25

Sum of deviation:=d1+d2+d3+d4+d5+d6
=-0.15-0.45-0.15+0.45+0.25-0.25
=0

Average Deviation: ∑|d|/n
=(0.15+0.45+0.15+0.45+0.25+0.25)/6
=0.283

Standard Deviation: ((∑d^2)/n-1)^0.5
=((0.15^2+0.45^2+0.15^2+0.45^2+0.25^2+0.25^2)/5)^0.5
=((.0225+.0225+.2025+.2025+0.0625+.0625)/5)^0.5
=(.575/5)^0.5
=.339

Variance: V=S^2=(0.339)^2
=0.114

Reference: "Electrical & Electronic measurement & Instrument", A. K. Sawhney, Dhanpat Rai & Co., 18th edition 2008.

UNIT NO. 6

VI: Sensors and Transducer
Strain Gauges, LVDT, Classification of transducers, transducers actuating mechanisms, resistive, capacitive, and inductive transducers, thermoelectric & photoelectric transducers, Temperature sensors.

Q. 1) *Define Transducer. Draw and explain with help of Block Diagram*
Answer:
Transducer: A transducer is defined as a device that converts one form of energy to other. It converts the measured physical quantity to a usable electrical signal. Thus it converts the physical quantity into a proportional electrical quantity.

It consist of two parts that are closely related to each other i.e. The sensing element and Transduction element. The sensing element is called as sensor. It is producing measurable response to change in physical quantity. The transduction element converts the sensor output into suitable electrical form.

Block Diagram:

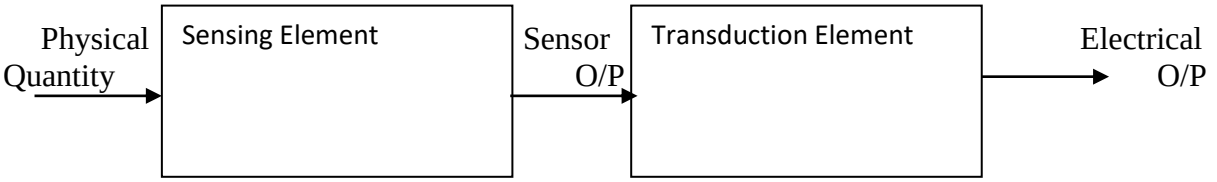


Figure 1: Block diagram of Transducer

As seen from the diagram transducer consists of two basic block, sensing element and transduction element. The sensing element accepts the physical quantity from nature as input. The output of sensing element is termed as sensor output and given to the transduction element which converts this quantity into electrical signal.

Initially the physical quantity in the form of light, temperature, pressure etc. is been sensed with the help of sensor. The sensor accepts this physical quantity and converts it into some intermediate form which is compatible with the transduction element.

This transduction element consists of the device which actually converts this intermediate output into electrical signal. The principal of operation of this element varies from element to

element.

For ex. Let consider the example of automated door which get open when some object come in the vicinity of the camera. In this case the light sensor is present which is continuously receiving the beam of light. As the object come in front of this sensor this beam of light vanishes for certain time and internally the signals are generated in such a way that the door open for certain some time as set by the programmer.

Q.2) *Explain various types of Transducer in detail.*

Answer:

Transducer: A transducer is a device that convert one form of energy to other. It convert the measured to a usable electrical signal.

In broad way it can be define as a device that convert mechanical force into electrical signal. The physical parameter such as heat,intensity of light, flow rate, liquid level, humidity and pH value are convert into electrical energy by means of transducer. These transducer provide an output signal when stimulated by a mechanical or non mechanical output.

For example: A photoconductor converts light intensity into resistance, a thermocouple converts heat energy into electrical voltage, a stain gauge convert force into resistance etc.

Electrical Transducer:

In order to measure non electrical quantities a detector is used which usually convert the physical quantity into a displacement. This displacement actuates an electrical transducer, which act as secondary transducer and gives an output which is electrical in nature. These electrical quantities are measured by standard methods used for electrical measurement. This result is proportional to the magnitude of physical quantity.

Advantages of Electrical Transducer

The advantages of converting physical quantities into analog electrical quantity are:

i. Electrical amplification and attenuation can be done easily
ii. The mass inertia effect is minimized
iii. Effect of friction are minimized
iv. The electrical and electronic system can be controlled with less power
v. The electrical output can be easily used, transmitted and processed
vi. Telemetry is used in all sophisticated measurement system
vii. Miniaturization can be easily done

Classification of Transducer:

The transducer can be classified as:

1. Active and Passive Transducer
2. Analog and Digital Transducer
3. On the basic of Transconduction principal
4. Primary and secondary Transducer
5. Transducer and inverse Transducer

Active and Passive Transducer:

Active Transducer:

This Transducer do not need any external source of power for their operation. These are self generating devices which operate under energy conversion principal.

Velocity, temperature, light intensity an force can be traduced with the help of active transducer. For example tachogenerator, thermocouple, photovoltaic cell, piezoelectric crystal etc.

Let's take the example of piezoelectric crystal which is used for measurement of accelerator. In this transducer the crystal is sandwiched between two metallic electrode and the entire sandwiched is fastened to the base which may be the floor of the rocket. A fixed mass is placed on top of sandwich. According to the property of piezoelectric crystal when a force is applied to them the output voltage is generated.

Thus when a mass is exert certain force on crystal due to acceleration applied at the base, voltage is generated which is proportional to the acceleration. This transducer is called as accelerometer.

Passive Transducer:

This transducer need external source of power for their operation. Thus they are not self generating type transducer. A DC power supply or an audio frequency generator is used as an external power source. These transducer produce the O/P signal in the form of variation in resistance, capacitance, inductance or some other electrical parameter in response to the quantity to be measured.

Lets take the example of POT which is used for measurement of displacement. It is a resistive transducer powered by a source voltage which is used for measurement of linear displacement xi.

Thus suppose L is the total length of potentiometer whose total resistance is Ri and input displacement xi then,

$e0=(xi/L)*ei$

$xi=(e0/ei)*L$

Primary and Secondary Transducer

In most measurement system there is a suitable working combination where a mechanical device act as a primary detector and electrical device act as secondary transducer.

For example a Load Cell which is a short column with resistance wire strain gauge bonded to it. The force is first detected by column and is converted into strain which is a mechanical displacement. The higher the force the higher is the strain and thus the input signal is converted into analog output. The strain changes the resistance of strain gauge. Thus the output is change in value of resistance, which is in electrical form. In this case first the force is converted into mechanical displacement by the column and then secondly this mechanical displacement is converted into change in resistance. Thus column act as primary transducer and gauge as secondary transducer.

Similarly in case of LVDT the bourdan tube act as primary detector which sense the pressure and convert it into displacement. This displacement move the core of linear variable differential transformer that act as secondary transducer, which produce an output voltage which is proportional to displacement.

Primary Transducer:

The Mechanical device that convert physical quantity to be measured into a mechanical signal. Such mechanical device are called as primary transducer, because they deal with physical quantity to be measured.

Secondary Transducer:

The electrical device that convert this mechanical signal into a corresponding electrical signal. Such electrical device are known as secondary Transducer.

According to Transconduction Principal

Capacitive Transducer

In this type the measured is converted to a change in the Capaciatnce. A typical capacitor is comprised of two parallel plates of conducting material separated by electrical insulating material called dielectric. The plates and dielectric may be either flattened or rolled. The purpose of the dielectric is to help the two parallel plates to maintain their stored electrical charges.

Inductive Transducer

In inductive transduction the measured is converted into a change in the self inductance of a signal coil. It is achieved by displacing the core of the coil that is attached to a mechanical sensing element. Resistive Transducer.The transducer in which the resistance change due to the change in some physical phenomenon.

The resistance of a metal conductor is expressed by a simple equation

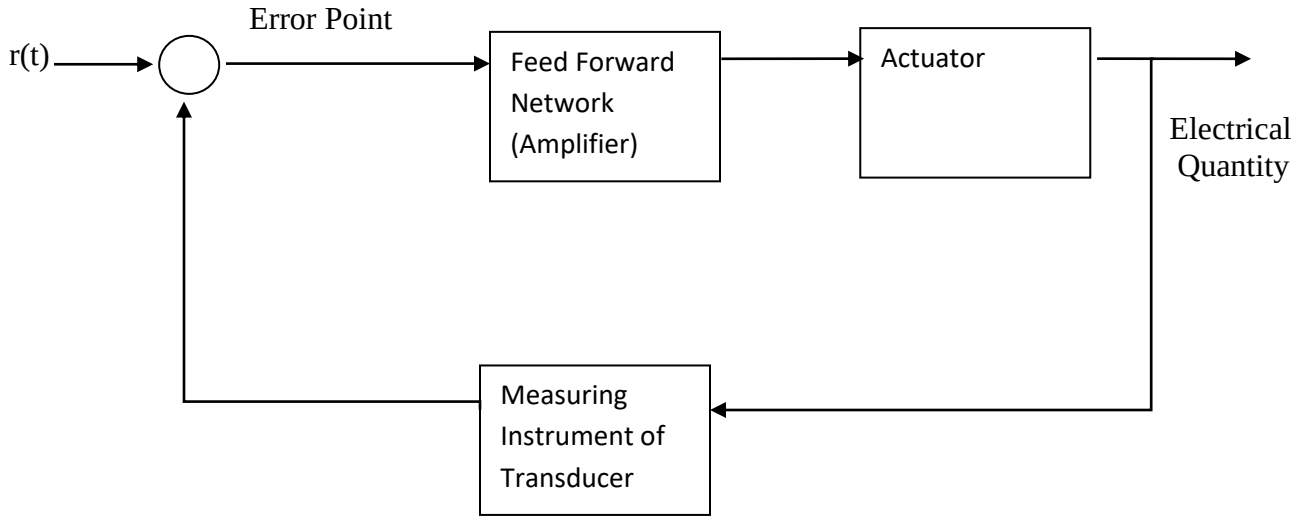
$R=_{o}L/A$

Where

R=Resistance of Conductor
L=Length of conductor in m
A=Cross sectional area of conductor m^2,
$_{\varrho}$= resistivity of conductor material

Transducer and Inverse Transducer

In industrial automation process considering a example of a Feedback control system. In this system the input is a physical quantity which is to be monitored. Thus for this purpose we need to process the input quantity and thus this physical quantity need to be converted into electrical quantity and the processing is done. These signal are then send to feed back circuit and further decision are taken where we need to convert this electrical quantity into physical quantity. Thus many a time we require to transform even electrical quantity into physical form. Thus we require Transducer as well as Inverse Transducer in the automation system.



Transducer

Transducer converts non electrical quantity to electrical quantity. For example physical quantity like speed, temperature, pressure, flow rate etc. These physical quantity need to be converted into electrical output for processing of signal.

Inverse Transducer

Inverse Transducer converts electrical quantity to a non electrical quantity.

Analog and Digital Transducer

Analog Transducer

The transducer which gives the output in analog output is known as Analog Transducer. For example: strain gauge, LVDT, thermocouple etc

Digital Transducer

The transducer which gives the output in digital form is known as digital Transducer. These output are in form of 0 and 1 and are represented on opaque and transparent area on a glass scale os non conducting and conducting metal scale.

The complex binary number denoting position is obtained by scanning the pattern across the scale at a stationary index mark. These scale can be read optically by means of light source, optial system or photocells.

Q. 3) *Explain in detail LVDT*

Ans:

An LVDT is defined as Linear Voltage Differential transformer where in the displacement is converted into voltage i.e. physical quantity into electrical quantity.

Construction:

It comprises of Primary winding P which is excited with an AC current, central ferrite core which is in central position and the secondary winding S1 and S2 wound on a cylindrical former.This winding have equal no of turns and are identically placed on either side of primary winding. A movable soft iron core is placed inside the former.

Working Principal:

The displacement to be measured is applied to the arm attached to the soft iron core which is made of high permeability, nickel iron which is hydrogen annealed, which give low harmonics, low null voltage and high sensitivity. This is slotted longitudinally to reduce eddy current losses.

This entire assembly is placed in a stainless steel housing and the end lid provide electrostatic and electromagnetic shielding.

The primary winding is excited with the AC current between 50Hz to 20kHZ. This AC current produce alternating magnetic field which is induced in secondary winding. i.e S1 is Es1 and S2 is Es2. Thus the differential output voltage is **E0=Es1-Es2**

When the core is in the centre of the coil equal emf is induced in both the secondary coil i.e. e01=e02 due to equal flux linkage. Thus output voltage e0 is equal to zero. This position is called Null Position.

When there is the displacement the central core moves either to or fro due to which the emf

induced in secondary is unequal i.e.e01 is not equal e02 and there is some output voltage e0.

When the core is moved to left, more flux is links with winding S1 and less with winding S2. Thus Es1>Es2 which gives E0=Es1-Es2 i.e. output voltage in phase with the primary voltage.

When the core is moved to right, more flux is links with winding S2 and less with winding S1. Thus Es2>Es1 which gives E0=Es1-Es2 i.e. output voltage is 180 degree out of phase with the primary voltage.

The amount of voltage change in secondary is proportional to the amount of movement in core. Depending upon the increase or decrease in output voltage, we can determine the direction of motion.

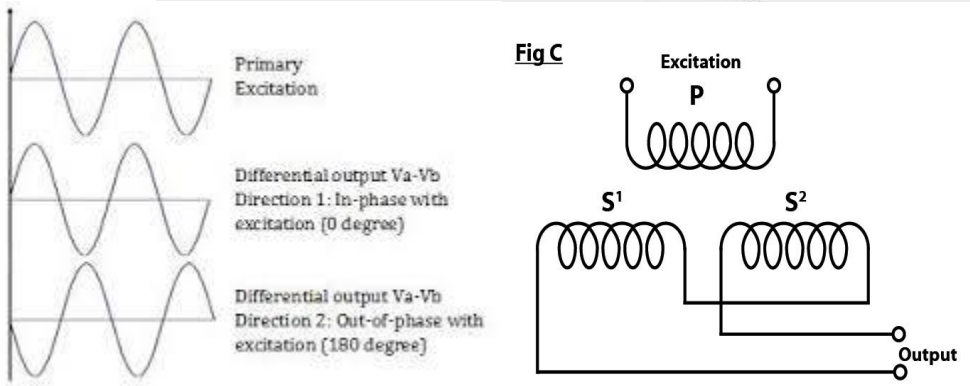


Figure 2: LVDT

Q. 4) *Explain Strain Gauge in Detail.*

Ans:

A Strain gauge is an example of passive transducer that convert a mechanical displacement into a change in resistance. It works on the property called piezoresistive effect which state that, the resistivity of the conductor is changed when it is strained. Therefore this strain gauge is also termed as piezoresistive gauge.

This can be explain as if the strip of elastic material is subjected to tension or strained, it's longitudinal dimension will increase while there will be reduction in the lateral dimention. Thus when a gauge is subjected to positive strain, it's length increase while it's area of cross section decrease. Since the resistance of conductor is proportional to it's length and inversely proportional to it's cross section, the resistance of the gauge increases with positive strain.

Let us consider a strain gauge made of circular wire with dimension

L=Length

A=Area

D=Diameter before Strained

ρ = Resistivity

Resistance of unstrained Gauge $R= \rho L/A$

Now if Tensile stress s is applied to the wire the dimension of the wire changes

Let

ΔL=Change in Length

ΔA=Change in Area

ΔD=Change in Diameter

ΔR=Change in Resistance

In order to find how ΔR depends upon the material physical quantities, the expression for R is differential with respect to stress s

Thus we get:

$dR/ds= \rho/A*\delta L/\delta s- \rho L/A2\ \rho A/\ \delta s+L/A\delta\rho/\delta s$

Dividing the equation by $R= \rho L/A$

$1/R\ dR/ds=1/L\ \delta L/\delta s-1/A\delta A/\delta s+1/\rho\delta\rho/\delta s$

Thus from equation it can be concluded that

i. Per unit change in Length=ΔL/L
ii. Per unit change in Length=ΔA/A
iii. Per unit change in Length=Δρ/ρ

Thus the Gauge factor is defined as the ratio of per unit change in resistance to per unit change in length.

Thus Gauge Factor Gf=(ΔR/R)/(ΔL/L)

Or

$\Delta R/R = Gf * \Delta L/L$

$= Gf * \varepsilon \Delta L/L$

Where ε=Strain= $\Delta L/L$

The gauge factor can be written as

$=1+2v+(\Delta \rho/ \rho)/ \varepsilon$

1: Resistance change due to change in length

2v: Resistance change due to change in area

$(\Delta \rho/ \rho)/ \varepsilon$: Resistance change due to piezoresistive effect

$Gf=(\Delta R/R)/(\Delta L/L) = 1+2v+(\Delta \rho/ \rho)/ (\Delta L/L)$

If the change in the value of resistivity of a material when strained is neglected, the gauge factor is:

$Gf=1+2v$

Types of Strain gauge:

Based on principal of working:

1. Mechanical
2. Electrical
3. Piezoelectric

Based on Mounting:

1. Bonded Strain gauge
2. Un Bonded Strain Gauge

Based on Construction

1. Foil Strain Gauge
2. Semiconductor strain gauge
3. Photoelectric strain gauge

Advantages:

1. There is no moving part
2. It is small
3. It is reasonable

Disadvantage

1. It is non linear
2. It needs to be calibrated

Application

1. Residual stress

2. Vibration measurement
3. Torque Measurement
4. Bending and deflection measurement
5. Compression and tension measurement
6. Strain Measurement

Q. 5) *Explain Proximity Sensor in Detail.*
Ans:

Proximity sensors detect an object when the object approaches within the detection range and boundary of the sensor. Proximity sensors include non contact detection.

Types of Proximity Sensor
1. Inductive Proximity Sensor
2. Capacitive Proximity Sensor
3. Ultrasonic Proximity Sensor
4. Optical Proximity Sensor

Inductive Proximity Sensor

An inductive proximity sensor is an electronics proximity sensor which detect metallic object without touching them. Their operating principal is based on a coil and high frequency oscillator that creates a field in the close surrounding of the sensing surface. The operating distance of the sensor depends on the coil size as well as the target shape, size and material.

Advantages:
1. They are very accurate compared to other technologies
2. High Switching rate
3. Rigid in Nature

Disadvantage
1. It can detect only metallic Target
2. Operating range may be limited

Application
1. Metal Detector
2. Car washes
3. Host of automated industrial process

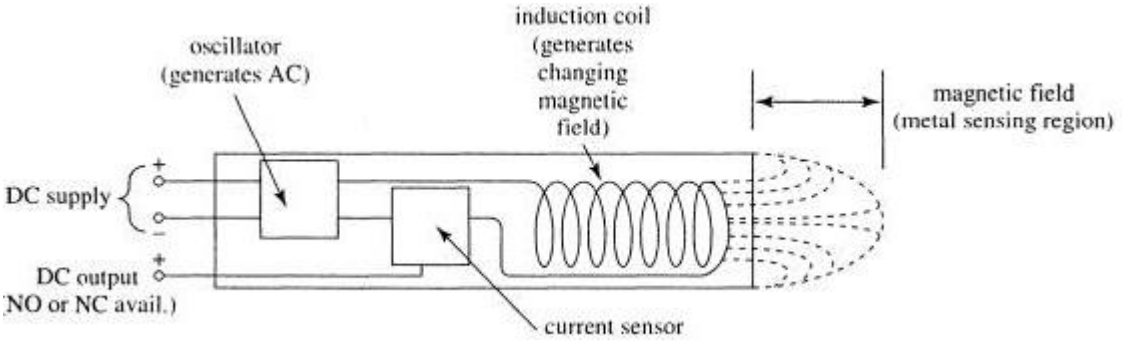


Figure 3: Inductive Proximity Sensor

Capacitive Proximity Sensor

Capacitive sensor are used for non contact detection of metallic object and non metallic object . Capacitive proximity sensor use the variation of capacitance between the sensor and object being detected. These sensor are very sensitive in nature. The main component of these sensor are Plate, Oscillator, Threshold Detector and output circuit. The plate inside the sensor act as one plate of the capacitor and the target act as another plate and the air act as the dielectric between the plates. The capacitive sensor can detect any target whose dielectric constant is more than air. As the object comes closer to the plate of the capacitor the capacitance increases and as the object moves away the capacitance decreases. An electronic circuit inside the sensor began to oscillate. The rise or fall of such oscillation is identified by the threshold circuit and based on that output switches.

Advantages:

1. It can detect both metallic and non metallic target
2. Good Stability
3. High Speed
4. Capacitive Sensor are good in terms of power usage
5. Low cost

Disadvantages:

1. They are affected by temperature and humidity
2. Difficulty in design
3. Accuracy is less as compared to inductive transducer

Application

1. These sensor are used in many devices such as laptop track pad, digital audio player, computer display, mobile phone or other.
2. Used for design purpose as they are versatile, reliable, robust and less costly.

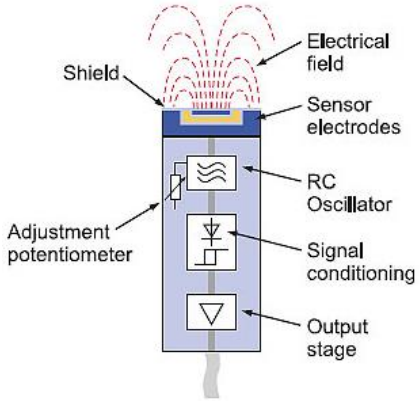


Figure 4: Capacitive Proximity Sensor

Q. 6) *Explain working principal of Thermocouple.*
Ans:

A thermocouple is a temperature measuring device consisting of two dissimilar conductors that contact each other at one junction. It produce a voltage when the temperature of one of the ends differs from the reference temperature at other end of the circuit.

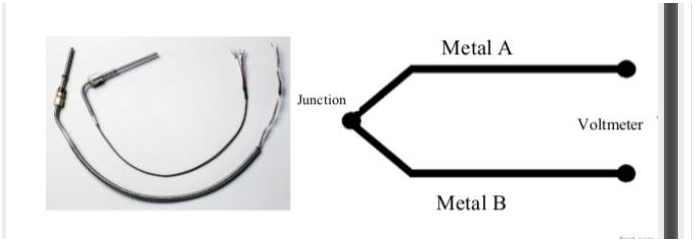


Figure 5: Thermocouple

SEEBECK EFFECT

The seebeck effect is the conversion of thermal energy/temperature difference directly into electrical energy or electricity. The change in the voltage is proportional to the temperature difference between the junctions when the end are connected form a loop.

Principal of Operation

As shown in figure it consist of two wire A and B with different physical and chemical property. When the temperature at junction T1 is changed the voltage in two wires changes according to their property which is reflected at node T2. This voltage difference is shown as a voltage by Voltmeter at the end of circuit i.e opposite to T1.

The emf produced in a thermocouple circuit is given by:

$E=a(\Delta\theta)+b(\Delta\theta)^2$

Where

$\Delta\theta$=difference in temperature between the hot thermocouple junction and the refrence junction of the thermocouple; degree C

a,b= constant

a is usually very large as compared with b and therefore emf thermocouple is

$E \sim a(\Delta\theta)$ or $\Delta\theta \sim E/a$

In a thermocouple temperature measuring circuit, the emf set up is measured by sending a current through a moving coil instrument, the deflection being directly proportional to the emf.

Since emf is a function of temperature difference $\Delta\theta$, the instrument can be calibrated to read the temperature.

.

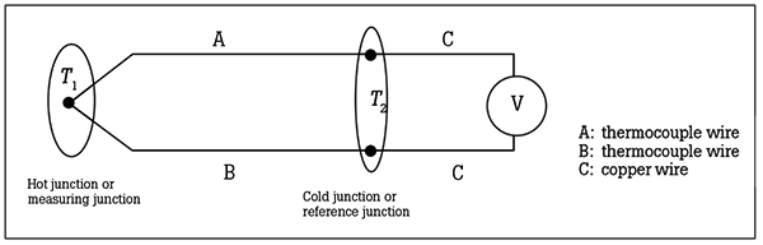


Figure 6: Seebeck Effect

Application

1. Steel Industry
2. Gas Appliance Safety
3. Thermopile radiation sensor
4. Manufacturing
5. Power production
6. Thermoelectric coding
7. Process Plants
8. Thermocouple as vacuum Gauge
9. Heaters

Q.7) *Explain Thermister in detail.*

Ans:

The word Thermistor is derived from two words "Thermal Resistors". Temperature sensing element which measure temperature according to change in resistance. These are generally composed of semi conductor material. They may or may not be self heated. They use ceramic or polymer material while RTDs use pure metal.

Thermistor are widely used in application which involve measurement in the range of -60 degree C to 15 degree C. The resistance of thermistor range from 0.5Ω to 0.75 Ω. These are highly sensitive device however exhibits a non linear characteristics of resistance versus temperature.

There are two types of Thermistor

Positive Temperature Co-efficient: When the Resistance of thermistor increases with increase in temperature then it is known as Positive Temperature Co-efficient thermistor.

Negative Temperature Co-efficient: When the Resistance of thermistor decreases with increase in temperature then it is known as negative Temperature Co-efficient thermistor.

This temperature co efficient can be as large as several percentage per degree Celsius. Thus I can detect very small change in temperature which could nit be observed with RTD or thermocouple.

Resistance Temperature Characteristics of Thermistors

The mathematical expression between resistance and temperature is given by:

$RT1=RT2 \exp [\beta(1/T1-1/T2)$

Where,

RT1=Resistance of the thermistor at absolute temperature T1; 0K

RT2=Resistance of the thermistor at absolute temperature T2; 0K

And

β=a constant depending upon the material of thermistor, typically 3500 to 4500 0K

ΔR=kΔT

The sensitivity of thermistor for measurement of temperature can be understood by taking example of resistance temperature characteristics of platinum which is commonly used material for resistance thermistor. Between -100 degree C and 400 degree C normally thermistor changes it's resistivity from 10^5 to 10^-2 Ωm, a factor of 10^7, while platinum changes it's resistivity by factor about 10 within the same temperature range.

Advantages:

1. Low Cost
2. Sensitivity is high
3. Small in size
4. Good Stability
5. High Output Signal
6. Easy to transport

Disadvantages:

1. Non linear output
2. Non suitable for high temperature measurement
3. Require external power supply
4. Shielded cables should be used to minimize inyerferance
5. Self heating

Application:

The Positive Temperature Thermistor is used in

1. Current limiting device
2. Timer in degaussioan coil
3. Motors
4. Self Regulating Heaters

The Negative Temperature Thermistor is used in

1. Very low temperature thermometer
2. Digital thermostat
3. In rush protection device
4. Battery Pack monitors

Q. 8) *Define and explain load cell in detail.*
Ans:

Transducer that is used to convert a force/pressure into an electrical signal. Electrical output is in the order of few millivolts and requires amplification by an instrumentation amplifier for further use. Load cell are also called Load Transducer or Load sensor Force is measured in terms of deflection or strain of elastic member or increase in fluid pressure.

Types of load Cell

1. Hydraulic Load Cell:

When a force is applied on a liquid medium contained in a confirmed space, the pressure of the liquid increase. This increase in pressure of liquid is proportional to the applied force. Hence a measure of the increase in pressure of the liquid becomes a measure of the applied force.

2. Pneumatic Load Cell

If a force is applied to one side of diaphargam and an air pressure is applied to the other side some particular value of pressure will be necessary to exactly balance the force. This pressure is proportional to applied force.

3. Strain Gauge Load Cell

Working principal:

A load cell is made by bonding starin gaudge to an elastic material. For accurate measurement, it is bounded to the position of elastic material of the stress will be the largest. Thus the pressure is converted in electrical resistance.

Advantages:

1. Rugged and compact construction
2. No moving parts
3. Highly accurate
4. Wide range of measurement can be used for static and dynamic loading

Disadvantage

1. Mounting is difficult
2. Calibration is tedious

Application:

1. Dual Tank Level Controller
2. Bag Filling Machine
3. Tank/Silo/Hopper
4. Food Packing

Q. 9) *Explain Bonded Wire Strain Gauge in detail.*

Ans:

The Bonded Wire Strain gauge are used for stress analysis and construction of transducers .It consist of grid of fine wire resistance wire of about 0.025mm in diameter or less.

This grid is connected to base which may be thin sheet of paper, a thin sheet of Bakelite or sheet of Teflon. The wire is covered on top with a thin sheet of material so as to prevent from mechanical damage. The spreading of wire permits a uniform distribution of stress over the grid. The carrier is bonded with an adhesive material to the specimen under study which permit good transfer of strain from carrier to grid of wires.

Since the material and the wire size used for bonded wire strain gauge are same as used for un bonded wire strain gauge, the gauge factors and resistance for both comparable.

The size of strain gauge varies with application .i.e. (as small as 3mm by 3cm and 25mm long and 12.5mm wide)

For excellent and reproducible results, it is desirable that the resistance wire strain gauge should having following characteristics

i. It should have a high value of gauge factor Gf. A high value of gauge factor indicates a large change in resistance for a particular strain resulting in high sensitivity
ii. The resistance of the strain gauge should be as high as possible since this minimizes the effect of undesirable variation of resistance in the measurement

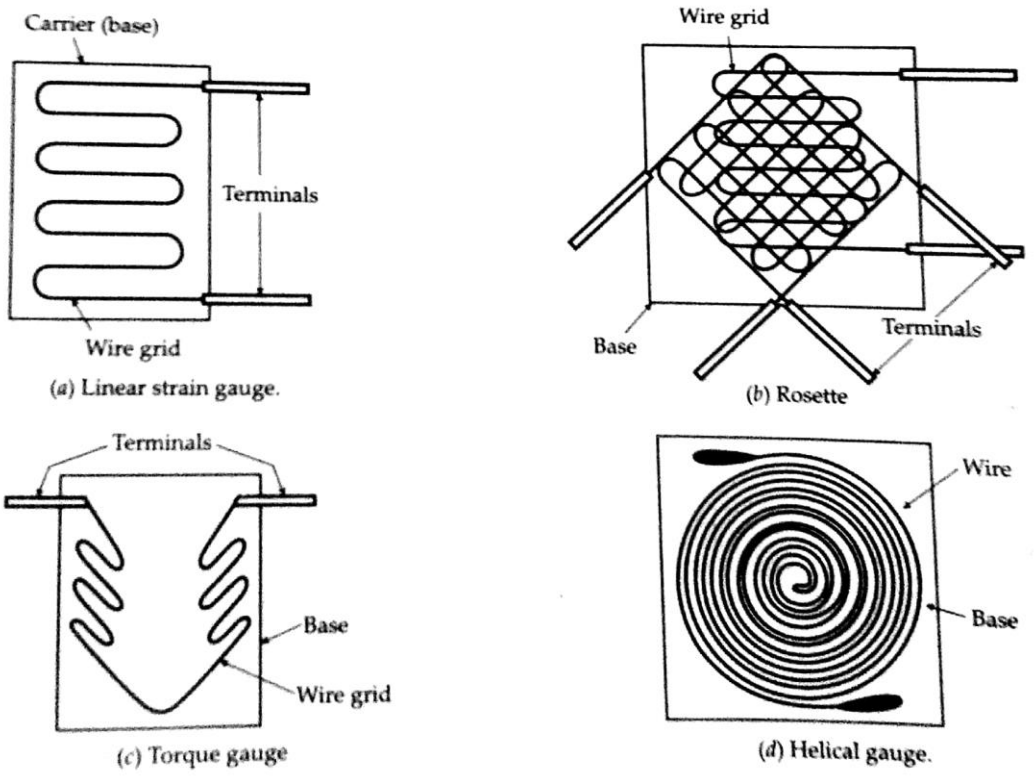


Figure 7: Different types of Bonded wire Strain Gauges

Reference:

"Electrical & Electronic measurement & Instrument", A. K. Sawhney, Dhanpat Rai & Co.,18th edition 2008.