Engineering Notebook

VOLUME 1

EE1308 Analog integrated circuits and its applications

A.V.Gokhale

Dr.Y.A.Gaidhani

DEPARTMENT OF ELECTRONICS ENGINEERING

YESHWANTRAO CHAVANCOLLEGE OFENGINEERING,

(AnautonomousinstitutionaffiliatedtoRashtrasantTukadojiMaharajNagpurUniversity,Nagpur)

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CONTENTS

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UNIT-1

Differential Amplifier configurations

Q.1. *Explain how the differential amplifier is developed and its different configurations?*

Answer:

The operational amplifier is a direct-coupled high gain amplifier usable from 0 to over 1MH Z to which feedback is added to control its overall response characteristic i.e. gain and bandwidth. The op-amp exhibits the gain down to zero frequency.

Such direct coupled (dc) amplifiers do not use blocking (coupling and by pass) capacitors since these would reduce the amplification to zero at zero frequency. Large by pass capacitors may be used but it is not possible to fabricate large capacitors on a IC chip. The capacitors fabricated are usually less than 20 pf. Transistor, diodes and resistors are also fabricated on the same chip.

Differential amplifier is a basic building block of an op-amp. The function of a differential amplifier is to amplify the difference between two input signals.Let us consider two emitter-biased circuits as shown in **fig. 1.1**.

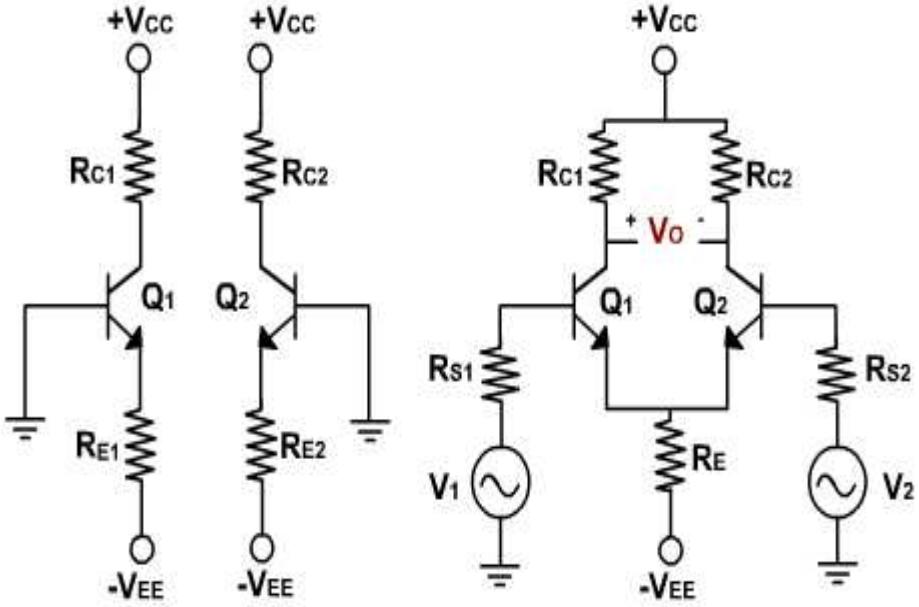

Figure 1.1 Differential Amplifier

The two transistors Q_1 and Q_2 have identical characteristics. The resistances of the circuits are equal, i.e. $R_{E1} = R_{E2}$, $R_{C1} = R_{C2}$ and the magnitude of $+V_{CC}$ is equal to the magnitude of $-V_{EE}$. These voltages are measured with respect to ground.

To make a differential amplifier, the two circuits are connected as shown in **fig. 1.1**. The two $+V_{CC}$ and $-V_{EE}$ supply terminals are made common because they are same. The two emitters are also connected and the parallel combination of R_{E1} and R_{E2} is replaced by a resistance R_E. The two input signals v_1& v_2 are applied at the base of Q_1 and at the base of Q_2. The output voltage is taken between two collectors. The collector resistances are equal and therefore denoted by $R_C = R_{C1} = R_{C2}$.

Ideally, the output voltage is zero when the two inputs are equal. When v_1 is greater then v_2 the output voltage with the polarity shown appears. When v_1 is less than v_2, the output voltage has the opposite polarity.

The differential amplifiers are of different configurations.

The four differential amplifier configurations are following:

1. Dual input, balanced output differential amplifier.
2. Dual input, unbalanced output differential amplifier.
3. Single input balanced output differential amplifier.
4. Single input unbalanced output differential amplifier.

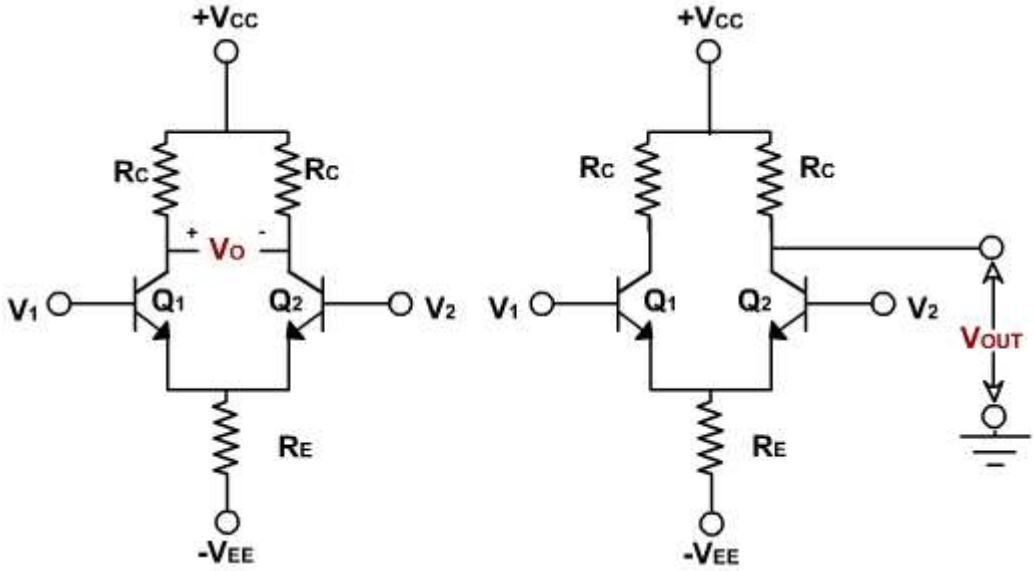

Figure 1.2 Dual input Balanced output and Dual input Unbalanced output Differential Amplifier

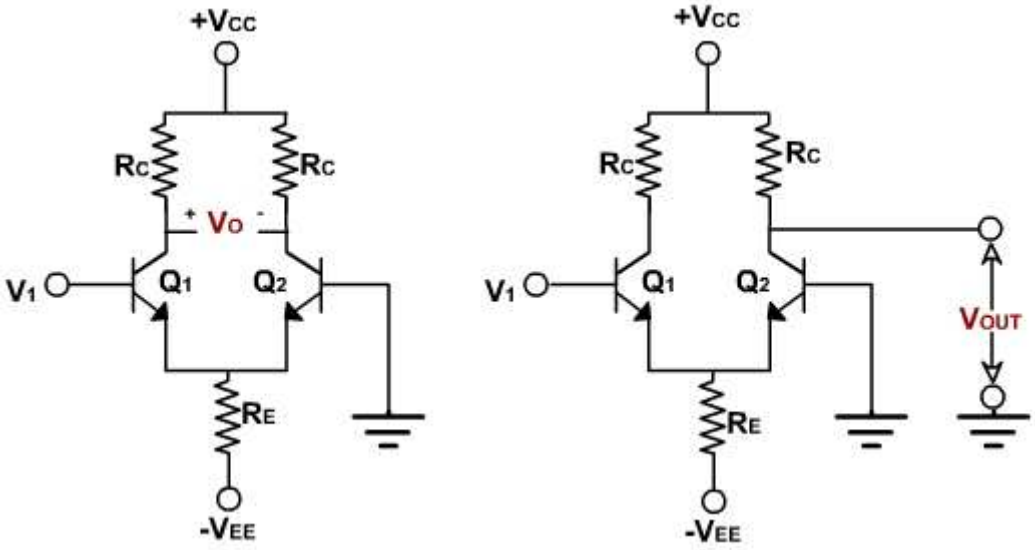

Figure 1.3 Single input Balanced output and Single input Unbalanced output Differential Amplifier

These configurations are shown in **fig. 1.2 and 1.3**, and are defined by number of input signals used and the way an output voltage is measured. If use two input signals, the configuration is said to be

dual input, otherwise it is a single input configuration. On the other hand, if the output voltage is measured between two collectors, it is referred to as a balanced output because both the collectors are at the same dc potential w.r.t. ground. If the output is measured at one of the collectors w.r.t. ground, the configuration is called an unbalanced output.

A multistage amplifier with a desired gain can be obtained using direct connection between successive stages of differential amplifiers. The advantage of direct coupling is that it removes the lower cut off frequency imposed by the coupling capacitors, and they are therefore, capable of amplifying dc as well as ac input signals.

Q.2. *Derive the expressions for DC analysis of Dual Input, Balanced Output Differential Amplifier.*

Answer:

The circuit of Dual Input, Balanced Output Differential Amplifieris shown in **fig. 1.4,** v_1 and v_2 are the two inputs, applied to the bases of Q_1 and Q_2 transistors. The output voltage is measured between the two collectors C_1 and C_2 , which are at same dc potentials.

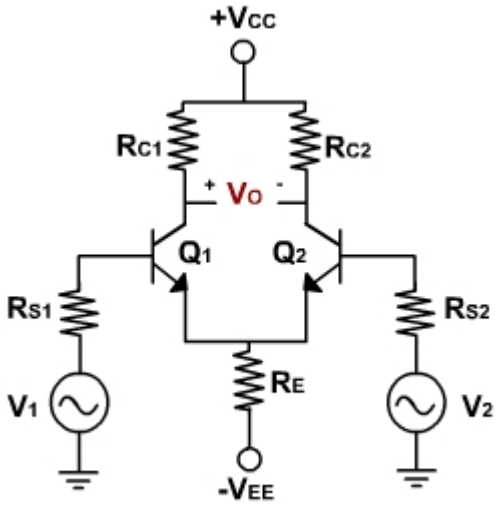

Figure 1.4 Dual input Balanced output Differential Amplifier

D.C. Analysis:

To obtain the operating point (I_{CC} and V_{CEQ}) for differential amplifier dc equivalent circuit is drawn by reducing the input voltages v_1 and v_2 to zero as shown in **fig. 1.5**.

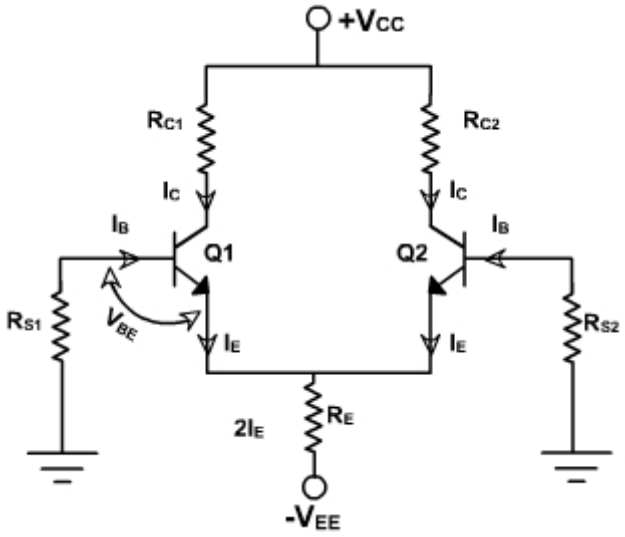

Figure 1.5 DC equivalent circuit of Dual input Balanced output Differential Amplifier

The internal resistances of the input signals are denoted by R_S because $R_{S1}= R_{S2}$. Since both emitter biased sections of the different amplifier are symmetrical in all respects, therefore, the operating point for only one section need to be determined. The same values of I_{CQ} and V_{CEQ} can be used for second transistor Q_2.

Applying KVL to the base emitter loop of the transistor Q_1.

$$R_S I_B + V_{BE} + 2 I_E R_E = V_{EE}$$

But $I_B = \frac{I_E}{\beta_{dc}}$ and $I_C \approx I_E$

$$\therefore I_E = I_C = \frac{V_{EE} - V_{BE}}{2R_E + R_S / \beta_{dc}} \qquad \text{(E-1)}$$

$V_{BE} = 0.6V$ for S_i and $0.2V$ for G_e.

Generally $\frac{R_S}{\beta_{dc}} << 2R_E$ because R_S is the internal resistance of input signal.

$$\therefore I_E = I_C = \frac{V_{EE} - V_{BE}}{2R_E}$$

The value of R_E sets up the emitter current in transistors Q_1 and Q_2 for a given value of V_{EE}. The emitter current in Q_1 and Q_2 are independent of collector resistance R_C.

The voltage at the emitter of Q_1 is approximately equal to $-V_{BE}$ if the voltage drop across R is negligible. Knowing the value of I_C the voltage at the collector $V_C$is given by

$$V_C = V_{CC} - I_C R_C$$

and $V_{CE} = V_C - V_E$

$$= V_{CC} - I_C R_C + V_{BE}$$

$$V_{CE} = V_{CC} + V_{BE} - I_C R_C \qquad \text{(E-2)}$$

From the two equations V_{CEQ} and I_{CQ} can be determined. This dc analysis applicable for all configurations of differential amplifier.

Q.3. *Derive the expressions for AC analysis of Dual Input, Balanced Output Differential Amplifier.*

Answer:

The circuit is shown in **fig. 1.6** v_1 and v_2 are the two inputs, applied to the bases of Q_1 and Q_2 transistors. The output voltage is measured between the two collectors C_1 and C_2, which are at same dc potentials.

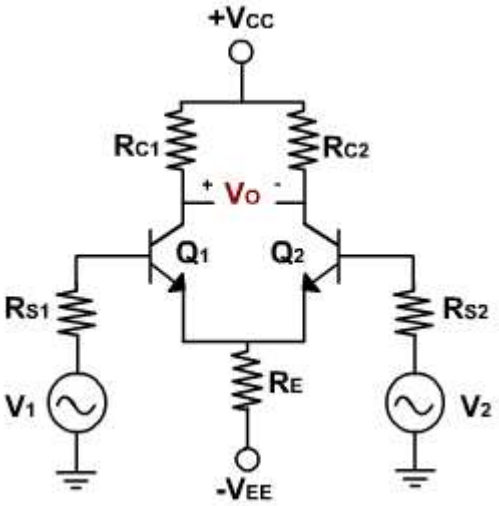

Figure 1.6 Dual input Balanced output Differential Amplifier

A.C. Analysis :**Differential Voltage GainA_d**

After performing the dc analysis we obtain the operating point of the two transistors.

To find the voltage gain A_d and the input resistance R_i of the differential amplifier, the ac equivalent circuit is drawn using r-parameters as shown in **fig. 1.7**. The dc voltages are reduced to zero and the ac equivalent of CE configuration is used.

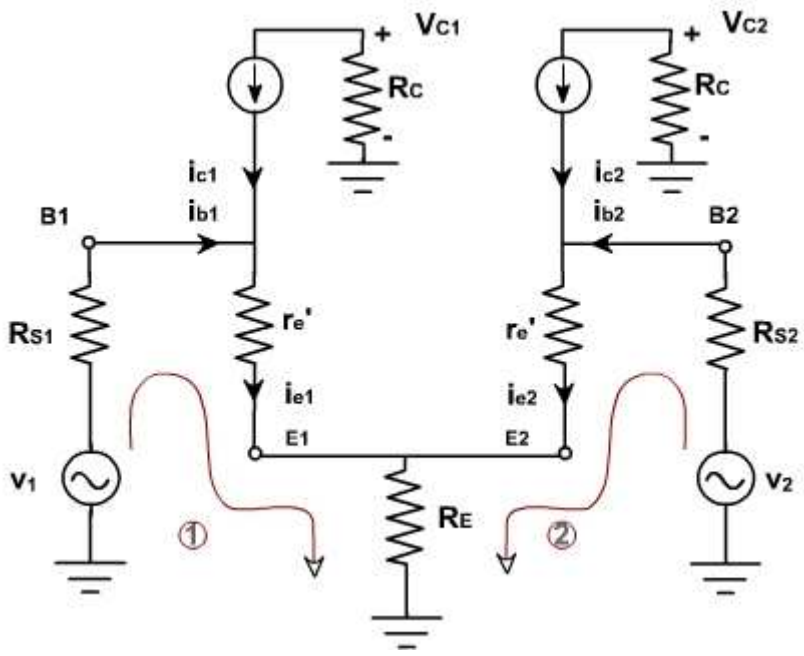

Figure 1.7 AC equivalent circuit of Dual input Balanced output Differential Amplifier

Since the two dc emitter currents are equal. Therefore, resistance r'_{e1} and r'_{e2} are also equal and designated by r'_e . This voltage across each collector resistance is shown 180° out of phase with respect to the input voltages v_1 and v_2. This is same as in CE configuration. The polarity of the output voltage is shown in Figure. The collector C_2 is assumed to be more positive with respect to collector C_1 even though both are negative with respect to to ground.

Applying KVL in two loops 1 & 2.

$$v_1 = R_{S1}\, i_{b1} + i_{e1}\, r'_e + (i_{e1} + i_{e2})\, R_E$$
$$v_2 = R_{S2}\, i_{b2} + i_{e2}\, r'_e + (i_{e1} + i_{e2})\, R_E$$

Substituting current relations,

$$i_{b1} = \frac{i_{e1}}{\beta}, \quad i_{b2} = \frac{i_{e2}}{\beta}$$
$$V_1 = \frac{R_{S1}}{\beta}\, i_{e1} + r'_e\, i_{e1} + R_E\, (i_{e1} + i_{e2})$$
$$V_2 = \frac{R_{S2}}{\beta}\, i_{e2} + r'_e\, i_{e2} + R_E\, (i_{e1} + i_{e2})$$

Again, assuming R_{S1} / b and R_{S2} / b are very small in comparison with R_E and r_e' and therefore neglecting these terms,

$$(r'_e + R_E)\, i_{e1} + R_E\, i_{e2} = v_1$$
$$R_E\, i_{e1} + (r'_e + R_E)\, i_{e2} = v_2$$

Solving these two equations, i_{e1} and i_{e2} can be calculated.

$$i_{e1} = \frac{(r_e + R_E)\, v_1 - R_E\, v_2}{(r'_e + R_E)^2 - R_E^2}$$

$$i_{e2} = \frac{(r'_e + R_E)\, v_2 - R_E\, v_1}{(r'_e + R_E)^2 - R_E^2}$$

The output voltage V_O is given by

$$V_O = V_{C2} - V_{C1}$$

$$= -R_C\, i_{C2} - (-R_C\, i_{C1})$$

$$= R_C\, (i_{C1} - i_{C2})$$

$$= R_C\, (i_{e1} - i_{e2})$$

Substituting i_{e1}, & i_{e2} in the above expression

$$v_o = R_C \left\{ \frac{(r_e + R_E)V_1 - R_E V_2}{(r'_e + R_E)^2 - R_E^2} - \frac{(r_e + R_E)V_2 - R_E V_1}{(r'_e + R_E)^2 - R_E^2} \right\}$$

$$= \frac{R_C (v_1 - v_2)(r'_e - 2R_E)}{r'_e (r'_e + 2R_E)}$$

$$\text{Therefore}, v_o = \frac{R_C}{r'_e}(v_1 - v_2) \qquad \text{(E-1)}$$

Thus a differential amplifier amplifies the difference between two input signals. Defining the difference of input signals as $v_d = v_1 – v_2$ the voltage gain of the dual input balanced output differential amplifier can be given by

$$A_d = \frac{v_C}{v_d} = \frac{R_C}{r'_e} \quad \text{(E-2)}$$

Differential Input Resistance: R_{i1} and R_{i2}

Differential input resistance is defined as the equivalent resistance that would be measured at either input terminal with the other terminal grounded. This means that the input resistance R_{i1} seen from the input signal source v_1 is determined with the signal source v_2 set at zero. Similarly, the input signal v_1 is set at zero to determine the input resistance R_{i2} seen from the input signal source v_2. Resistance R_{S1} and R_{S2} are ignored because they are very small.

$$R_{i1} = \left.\frac{v_1}{i_{b1}}\right|_{v_2 = 0}$$

$$= \left.\frac{v_1}{i_{e1}/\beta}\right|_{v_2 = 0}$$

Substituting i_{e1},

$$R_{i1} = \frac{\beta r'_e (r'_e + 2R_E)}{r'_e + R_E}$$

Since $R_E >> r'_e$

$\therefore \quad r'_e + 2R_E >> 2R_E$

or $\quad r'_e + R_E >> R_E$

$$\therefore R_{i1} = 2\beta r_e' \qquad \text{(E-3)}$$

Similarly,

$$R_{i2} = \left.\frac{V_2}{i_{b2}}\right|_{V_1=0}$$

$$= \left.\frac{V_2}{i_{e2}/\beta}\right|_{V_1=0}$$

$$R_{i2} = 2\beta r'_e \qquad \text{(E-4)}$$

The factor of 2 arises because the r_e' of each transistor is in series.

Output Resistance: $R_{O1}$and R_{O2}

Output resistance is defined as the equivalent resistance that would be measured at output terminal with respect to ground. Therefore, the output resistance R_{O1} measured between collector C_1 and ground is equal to that of the collector resistance R_C. Similarly the output resistance R_{O2} measured at C_2 with respect to ground is equal to that of the collector resistor R_C.

$$R_{O1} = R_{O2} = R_C \qquad \text{(E-5)}$$

The current gain of the differential amplifier is undefined. Like CE amplifier the differential amplifier is a small signal amplifier. It is generally used as a voltage amplifier and not as current or power amplifier.

Q.4. *The following specifications are given for the dual input, balanced-output differential amplifier of* ***fig.1.8:***
R_C = 2.2 kΩ, R_B = 4.7 kΩ, $R_{in\,1} = R_{in\,2}$ = 50 Ω , $+V_{CC}$ = 10V, $-V_{EE}$ = -10 V, β_{dc} =100 and V_{BE} = 0.715V.
Determine the operating points (I_{CQ} and V_{CEQ}) of the two transistors.

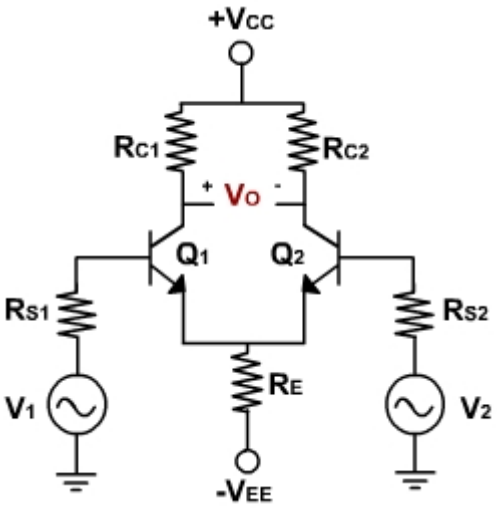

Figure 1.8 Dual input Balanced output Differential Amplifier

Solution:

The value of I_{CQ} can be obtained from equation (E-1).

$$I_{CQ} = I_E = \frac{V_{EE} - V_{BE}}{2R_E + R_{in}/\beta_{dc}}$$

$$= \frac{10 - 0.715}{9.4k\Omega + 50/100} = 0.988mA$$

The voltage V_{CEQ} can be obtained from equation (E-2).

$$V_{CEQ} = V_{CC} + V_{BB} - R_C I_{CQ}$$
$$= 10 + 0.715 - (2.2k\Omega)(0.988mA)$$
$$= 8.54V$$

The values of I_{CQ} and V_{CEQ} are same for both the transistors.

Q.5. *The following specifications are given for the dual input, balanced-output differential amplifier: RC = 2.2 kΩ, RE = 4.7 kΩ, Rin 1 = Rin 2 = 50Ω, +VCC= 10V, -VEE = -10 V, βdc =100 and VBE = 0.715V.*

a. Determine the voltage gain.
b. Determine the input resistance
c. Determine the output resistance.

Solution:

(a). The parameters of the amplifiers are same as discussed in example-1 of lecture-1. The operating point of the two transistors are given below

ICQ = 0.988 mA
VCEQ=8.54V

The ac emitter resistance

$$r_e' = \frac{25mV}{I_E mA} = \frac{25mV}{0.988mA} = 25.3\Omega$$

Therefore, substituting the known values in voltage gain equation (E-2), we obtain

$$A_d = \frac{v_o}{v_{id}} = \frac{R_C}{r_e} = \frac{2.2\,k\Omega}{25.3} = 86.96$$

b). The input resistance seen from each input source is given by (E-3) and (E-4):

$$R_{i1} = R_{i2} = 2\beta_{ac} r_e = (2)(100)(25.3) = 5.06k\Omega$$

(c) The output resistance seen looking back into the circuit from each of the two output terminals is given by (E-5)

$$Ro1 = Ro2 = 2.2\ k\ \Omega$$

Q.6. *For the dual input, balanced output differential amplifier of Q.5 above:*

- *a. Determine the output voltage (vo) if vin 1 = 50mV peak to peak (pp) at 1 kHz and vin 2 = 20 mV pp at 1 kHz.*
- **b.** *What is the maximum peal to peak output voltage without clipping?*

Solution:

(a) In Q.5, we have determined the voltage gain of the dual input, balanced output differential amplifier. Substituting this voltage gain (Ad = 86.96) and given values of input voltages in equation, we get

$$v_o = \frac{R_C}{r_e}(v_{in1} - v_{in2}) = 86.96\,(50mv - 20mV)$$
$$= 2.61\ Vpp$$

(b) Note that in case of dual input, balanced output difference amplifier, the output voltage vo is measured across the collector. Therefore, to calculate the maximum peak to peak output voltage, we need to determine the voltage drop across each collector resistor:

$$V_{R_C} = R_C I_C$$

Substituting IC = ICQ = 0.988 mA, we get

$$V_{R_C} = (2.2k\Omega)(0.988mA) = 2.17V < V_{CE} = 8.54V$$

This means that the maximum change in voltage across each collector resistor is ± 2.17 (ideally) or 4.34 V_{PP}. In other words, the maximum peak to peak output voltage with out clipping is (2) (4.34) = 8.68 V_{PP}.

Q.7. *Explain the concept of Inverting & Non – inverting Inputs and Common mode gain for dual input, balanced output difference amplifier*

Answer:

A dual input, balanced output difference amplifier circuit is shown in **fig. 1.9.**

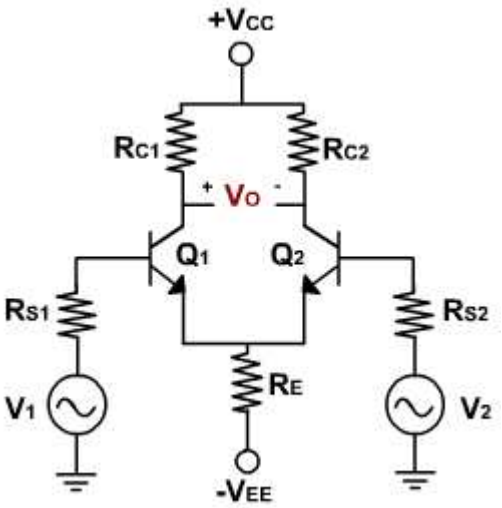

Figure 1.9 Dual input Balanced output Differential Amplifier

Inverting & Non – inverting Inputs:

In differential amplifier the output voltage v_O is given by

$$V_O = A_d (v_1 – v_2)$$

When $v_2 = 0$, $v_O = A_d v_1$

& when $v_1 = 0$, $v_O = - A_d v_2$

Therefore the input voltage v_1 is called the non inventing input because a positive voltage v_1 acting alone produces a positive output voltage v_O. Similarly, the positive voltage v_2 acting alone produces a negative output voltage hence v_2 is called inverting input. Consequently B_1 is called non-inverting input terminal and B_2 is called inverting input terminal.

Common mode Gain:

A common mode signal is one that drives both inputs of a differential amplifier equally. The common mode signal is interference, static and other kinds of undesirable pickup etc.

The connecting wires on the input bases act like small antennas. If a differential amplifier is operating in an environment with lot of electromagnetic interference, each base picks up an unwanted interference voltage. If both the transistors were matched in all respects then the balanced output would be theoretically zero. This is the important characteristic of a differential amplifier. It discriminates against common mode input signals. In other words, it refuses to amplify the common mode signals.

The practical effectiveness of rejecting the common signal depends on the degree of matching between the two CE stages forming the differential amplifier. In other words, more closely are the currents in the input transistors, the better is the common mode signal rejection e.g. If v_1 and v_2 are the two input signals, then the output of a practical op-amp cannot be described by simply

$v_0 = A_d (v_1 – v_2)$

In practical differential amplifier, the output depends not only on difference signal but also upon the common mode signal (average).

$v_d = (v_1 – v_d)$

and$v_C = ½ (v_1 + v_2)$

The output voltage, therefore can be expressed as

$v_O = A_1 v_1 + A_2 v_2$

Where A_1& A_2 are the voltage amplification from input 1(2) to output under the condition that input 2 (1) is grounded.

$$\therefore v_1 = v_C + \frac{1}{2}v_d \ , \quad v_2 = v_C - \frac{1}{2}v_d$$

Substituting V_1 & V_2 in output voltage equation

$$v_O = A_1 \left(v_C + \frac{1}{2}v_d\right) + A_2 \left(v_C - \frac{1}{2}v_d\right)$$

$$= \frac{1}{2}(A_1 - A_2)\, v_d + (A_1 - A_2)\, v_C$$

$$= A_d v_d + A_C v_C$$

The voltage gain for the difference signal is A_d and for the common mode signal is A_C.

The ability of a differential amplifier to reject a common mode signal is expressed by its common mode rejection ratio (CMRR). It is the ratio of differential gain A_d to the common mode gain A_C.

$$CMRR = \frac{A_d}{A_C} = \rho$$

$$\therefore v_O = A_d V_d \left(1 + \frac{1}{\rho}\frac{V_C}{V_d}\right)$$

Data sheet always specify CMRR in decibels CMRR(dB) = 20 log CMRR.

Q.8. *Derive the expressions for AC analysis of Dual Input, UnBalanced Output Differential Amplifier.*

Answer:

For Dual Input, Unbalanced Output Differential Amplifier, two input signals are given however the output is measured at only one of the two-collector w.r.t. ground as shown in **fig. 1.10**. The output is referred to as an unbalanced output because the collector at which the output voltage is measured is at some finite dc potential with respect to ground..

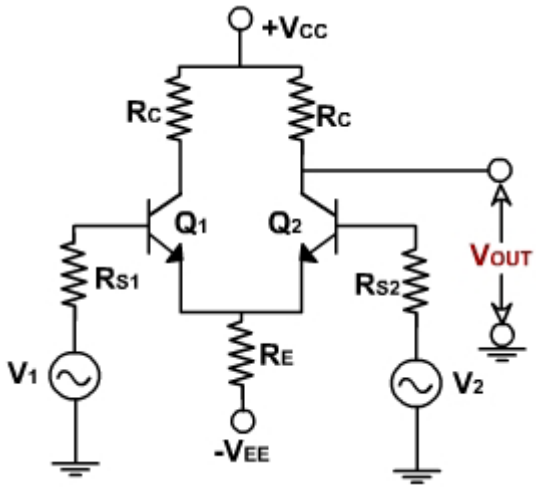

Figure 1.10 Dual input Unbalanced output Differential Amplifier

A.C. Analysis :Differential Voltage Gain A_d

After performing the dc analysis we obtain the operating point of the two transistors.

To find the voltage gain A_d and the input resistance R_i of the differential amplifier, the ac equivalent circuit is drawn using r-parameters as shown in **fig. 1.11**. The dc voltages are reduced to zero and the ac equivalent of CE configuration is used.

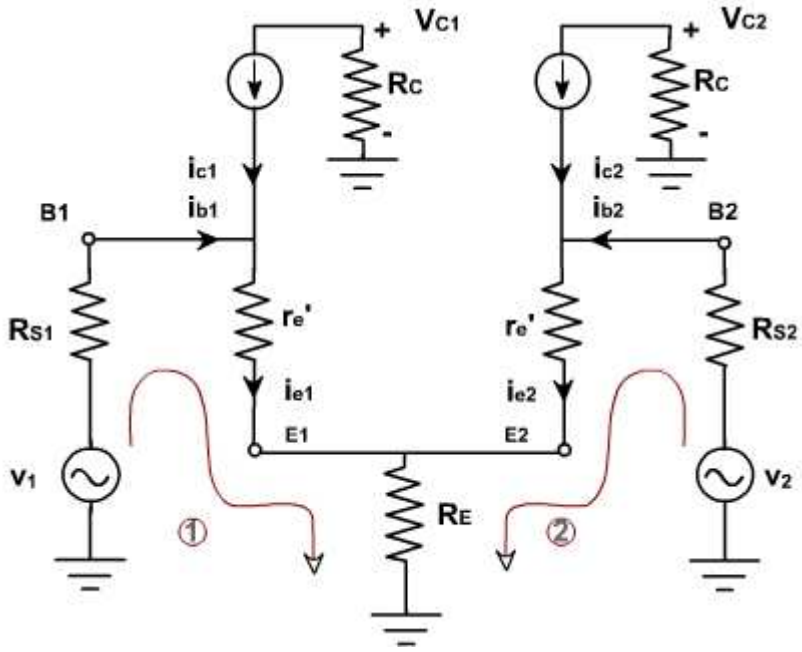

Figure 1.11 AC equivalent circuit of Dual input Unbalanced output Differential Amplifier

Since the two dc emitter currents are equal. Therefore, resistance r'_{e1} and r'_{e2} are also equal and designated by r'_e . This voltage across each collector resistance is shown 180° out of phase with respect to the input voltages v_1 and v_2. This is same as in CE configuration. The polarity of the output voltage is shown in Figure. The collector C_2 is assumed to be more positive with respect to collector C_1 even though both are negative with respect to to ground.

Applying KVL in two loops 1 & 2.

$$v_1 = R_{S1}\, i_{b1} + i_{e1}\, r'_e + (i_{e1} + i_{e2})\, R_E$$
$$v_2 = R_{S2}\, i_{b2} + i_{e2}\, r'_e + (i_{e1} + i_{e2})\, R_E$$

Substituting current relations,

$$i_{b1} = \frac{i_{e1}}{\beta},\quad i_{b2} = \frac{i_{e2}}{\beta}$$
$$V_1 = \frac{R_{S1}}{\beta}\, i_{e1} + r'_e\, i_{e1} + R_E\, (i_{e1} + i_{e2})$$
$$V_2 = \frac{R_{S2}}{\beta}\, i_{e2} + r'_e\, i_{e2} + R_E\, (i_{e1} + i_{e2})$$

Again, assuming R_{S1} / b and R_{S2} / b are very small in comparison with R_E and r_e' and therefore neglecting these terms,

$$(r'_e + R_E)\, i_{e1} + R_E\, i_{e2} = v_1$$
$$R_E\, i_{e1} + (r'_e + R_E)\, i_{e2} = v_2$$

Solving these two equations, i_{e1} and i_{e2} can be calculated.

$$i_{e1} = \frac{(r_e + R_E)\, v_1 - R_E\, v_2}{(r'_e + R_E)^2 - R_E^2}$$
$$i_{e2} = \frac{(r'_e + R_E)\, v_2 - R_E\, v_1}{(r'_e + R_E)^2 - R_E^2}$$

The output voltage V_O is given by

$V_O = V_{C2}$

$= -R_C\, i_{C2}$

$= -R_C\, i_{e2}$

Substituting i_{e2} in the above expression

$$V_o = -R_C \left\{ \frac{(r_e + R_E)V_2 - R_E V_1}{(r_e + R_E)^2 - {R_E}^2} \right\}$$

$$V_o = R_C \left\{ \frac{R_E V_1 - (r_e + R_E)V_2}{r_e(r_e + 2R_E)} \right\}$$

Since $R_E >> r_e$, $(r_e + R_E) \approx R_E$ and $(r_e + 2R_E) \approx 2R_E$

$$V_o = R_C \frac{R_E(V_1 - V_2)}{2r_e R_E}$$

$$V_o = \frac{R_C}{2r_e}(V_1 - V_2)$$

$$A_d = \frac{V_o}{(V_1 - V_2)} = \frac{R_C}{2r_e}$$

Thus a differential amplifier amplifies the difference between two input signals. Defining the difference of input signals as $v_d = v_1 - v_2$ the voltage gain of the dual input balanced output differential amplifier can be given by

$$A_d = \frac{V_c}{V_d} = \frac{R_C}{2r_e}$$

Differential Input Resistance: R_{i1}andR_{i2}

Differential input resistance is defined as the equivalent resistance that would be measured at either input terminal with the other terminal grounded. This means that the input resistance R_{i1} seen from the input signal source v_1 is determined with the signal source v_2 set at zero. Similarly, the input signal v_1 is set at zero to determine the input resistance R_{i2} seen from the input signal source v_2. Resistance R_{S1} and R_{S2} are ignored because they are very small.

$$R_{i1} = \left.\frac{v_1}{i_{b1}}\right|_{v_2 = 0}$$

$$= \left.\frac{v_1}{i_{e1}/\beta}\right|_{v_2 = 0}$$

Substituting i_{e1},

$$R_{i1} = \frac{\beta r'_e (r'_e + 2R_E)}{r'_e + R_E}$$

Since $R_E >> r'_e$

$\therefore \quad r'_e + 2R_E >> 2R_E$

or $\quad r'_e + R_E >> R_E$

$$\therefore R_{i1} = 2\beta r_e' \qquad \text{(E-3)}$$

Similarly,

$$R_{i2} = \left.\frac{V_2}{i_{b2}}\right|_{v_1 = 0}$$

$$= \left.\frac{V_2}{i_{e2}/\beta}\right|_{v_1 = 0}$$

$$R_{i2} = 2\beta r'_e \qquad \text{(E-4)}$$

The factor of 2 arises because the r_e' of each transistor is in series.

Output Resistance: $R_{O1}$and R_{O2}

Output resistance is defined as the equivalent resistance that would be measured at output terminal with respect to ground. Therefore, the output resistance R_O measured between collector C_2 and ground is equal to that of the collector resistance R_C.

$R_O = R_C$

The current gain of the differential amplifier is undefined. Like CE amplifier the differential amplifier is a small signal amplifier. It is generally used as a voltage amplifier and not as current or power amplifier.

Q.9. *Derive the expressions for AC analysis of Dual Input, Balanced Output Differential Amplifier with swamping resistors*

Answer:

The gain of the differential amplifier is inversely proportional to re which is temperature dependent and hence gain becomes dependent on the temperature. By using external resistors R_E' in series with each emitter, the dependence of voltage gain on variations of r_e can be reduced. It also increases the linearity range of the differential amplifier.**Fig. 1.12**, shows the differential amplifier with swamping resistor R_E'. The value of R_E' is usually large enough to swamp the effect of r_e.

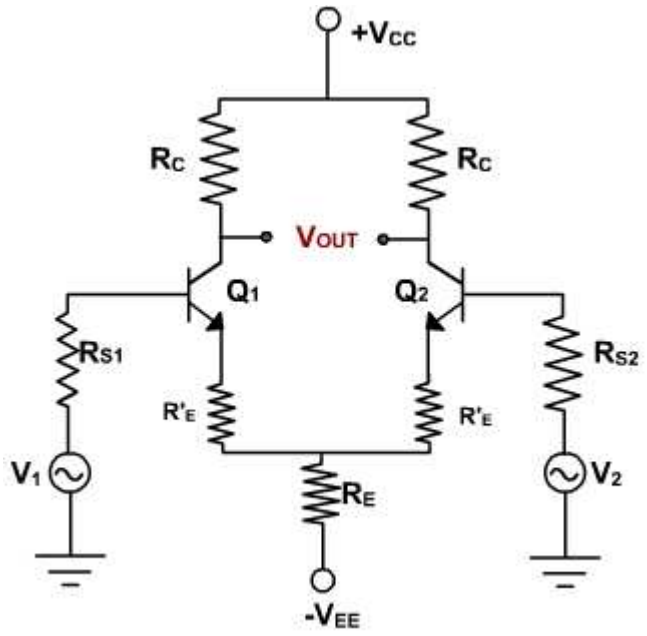

Figure 1.12 Dual input Balanced output Differential Amplifier with Swamping Resistor

DC Analysis:

To obtain the operating point (I_{CC} and V_{CEQ}) for differential amplifier dc equivalent circuit is drawn by reducing the input voltages v_1 and v_2 to zero as shown in **fig. 1.13**.

The internal resistances of the input signals are denoted by R_S because R_{S1}= R_{S2}. Since both emitter biased sections of the different amplifier are symmetrical in all respects, therefore, the operating point for only one section need to be determined. The same values of I_{CQ} and V_{CEQ} can be used for second transistor Q_2.

In DC equivalent circuit there is addition of R_E' in emitter path of both the transisitors, therefore the I_C and V_{CE} equations will have the term $R_E$repacled by $R_E + R_E'$.

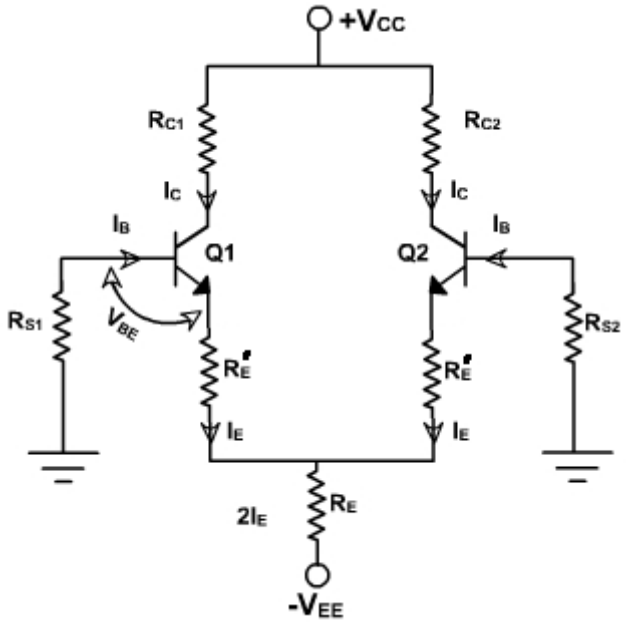

Figure 1.13 DC equivalent circuit of Dual input Balanced output Differential Amplifier with Swamping Resistor

$$I_E = I_C = \frac{V_{EE} - V_{BE}}{2R_E + R_E'}$$

$$V_{CE} = V_{CC} + V_{BE} - I_C R_C$$

AC analysis:

To find the voltage gain A_d and the input resistance R_i of the differential amplifier, the ac equivalent circuit is drawn using r-parameters as shown in **fig. 1.14**. The dc voltages are reduced to zero and the ac equivalent of CE configuration is used.

In the AC equivalent circuit the ac emitter resistance r_e is in series with swamping resistor R_E', therefore the equations will be changed with r_e replaced by $r_e + R_E'$.

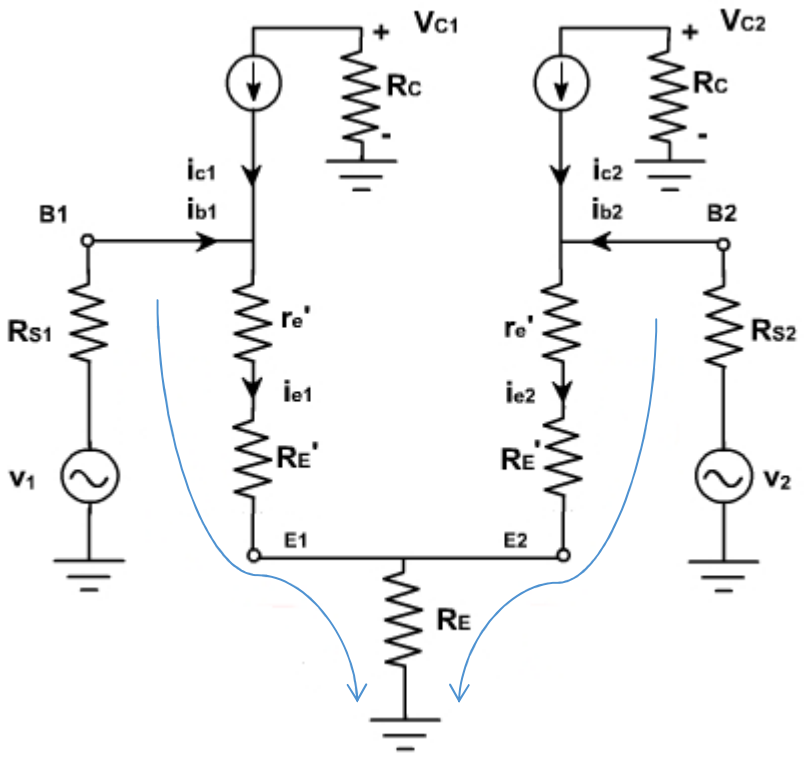

Figure 1.14 AC equivalent circuit of Dual input Balanced output Differential Amplifier with Swamping Resistor

Differential gain A_d

$$A_d = \frac{V_o}{(V_1 - V_2)} = \frac{R_C}{r_e + R_E{}'}$$

Input resistance R_{i1} and R_{i2}

$$R_{i1} = R_{i2} = 2\beta\left(r_e + R_E{}'\right)$$

Output resistance R_{o1} and R_{o2}

$$R_{o1} = R_{o2} = R_C$$

Q.10. *The following specifications are given for the dual input, balanced-output differential amplifier with swamping resistor: R_C = 2.2 kΩ, R_E = 4.7 kΩ, R_E' = 100Ω, $R_{in1} = R_{in2}$ = 50Ω, $+V_{CC}$= 10V, $-V_{EE}$ = -10 V, β_{dc} =100 and V_{BE} = 0.715V.*

a. Determine the voltage gain.
b. Determine the input resistance
c. Determine the output resistance.

Solution:

The operating point of the transistors is given by

$$I_E = I_C = \frac{V_{EE} - V_{BE}}{2R_E + R_E'}$$

$$I_C = \frac{10 - 0.715}{2 \times 4.7\ \text{k}\Omega + 100} = \mathbf{0.977mA}$$

$$V_{CE} = V_{CC} + V_{BE} - I_C R_C$$

$$V_{CE} = 10 + 0.715 - 0.977mA \times 2.2\ \text{k}\Omega = \mathbf{8.565V}$$

The ac emitter resistance re is given by

$$r_e = \frac{V_T}{I_E} = \frac{25mV}{0.977mA} = 25.588\Omega$$

The voltage gain is given by

$$A_d = \frac{R_C}{r_e + R_E'} = \frac{2.2\ \text{k}\Omega}{25.888 + 100} = 17.476$$

Input resistance R_{i1} and R_{i2}

$$R_{i1} = R_{i2} = 2\beta\left(r_e + R_E'\right) = 2 \times 100 \times (25.888 + 100) = 25.176\text{k}\Omega$$

Output resistance R_{o1} and R_{o2}

$$R_{o1} = R_{o2} = R_C = 2.2\ \text{k}\Omega$$

UNIT No 2

Operational amplifier fundamentals

Q1. *Draw the block diagram of operational amplifier and working of each block in brief. Comment on the parameters contributed by each stage.*

Answer:

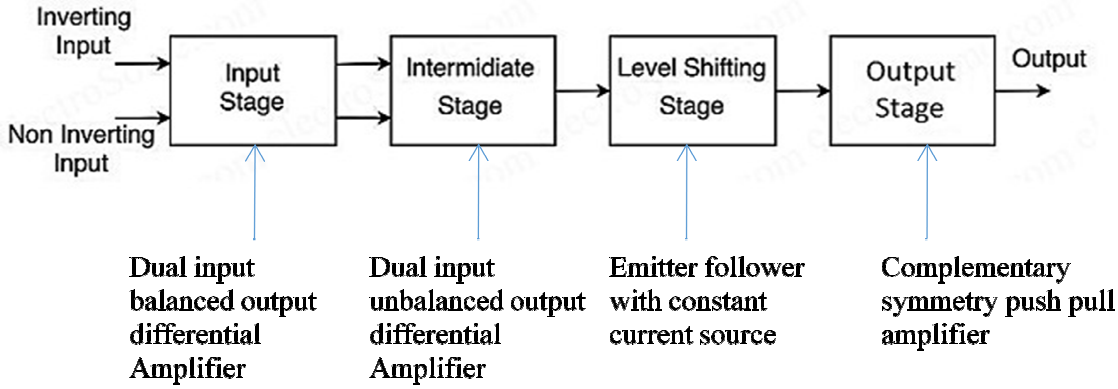

Figure 2.1: Block diagram of Operational amplifier

OPAMP is basically a differential amp i.e., it will amplify dc as well as ac i/p signals and was originally designed for computing such mathematical functions as addition, subtraction, multiplication and integration. Thus the name operational amplifier stems from its original use for these mathematical operation and is abbreviated to opamp. Since opamp is a multistage amplifier it can be represented by the block diagram as shown in above figure.

Input stage: The input stage is a dual input, balanced output differential amplifier. The two inputs are inverting and non- inverting i/p terminals. This stage provides most of the voltage gain of the OP-AMP and also establishes the value of i/p resistance Ri.

Intermediate stage: This is usually another differential amp. The i/p stage drives the stage. The stage is a dual –i/p unbalanced o/p differentiated amp. Due to direct coupling dc voltage at the output of intermediate stage is well above the ground potential.

Level- shifting stage: Due to direct coupling used between the 1st 2 stages, the i/p of level shifting stage is an amplified signal with some non – zero dc level. Level shifting stage is used to bring dc level to zero volts with respect to gnd.

Output stage: This stage is normally a push pull complementary o/p stage. It increases the magnitude of voltage swing and raises the current supplying capability of OP-AMP. It also ensures that the o/p resistance of OPAMP is low.

Q2. *Draw the circuit of voltage shunt feedback amplifier using opamp and derive the expression for closed loop gain , input resistance with feedback, output resistance with feedback and banwidth with feedback.*

Answer:

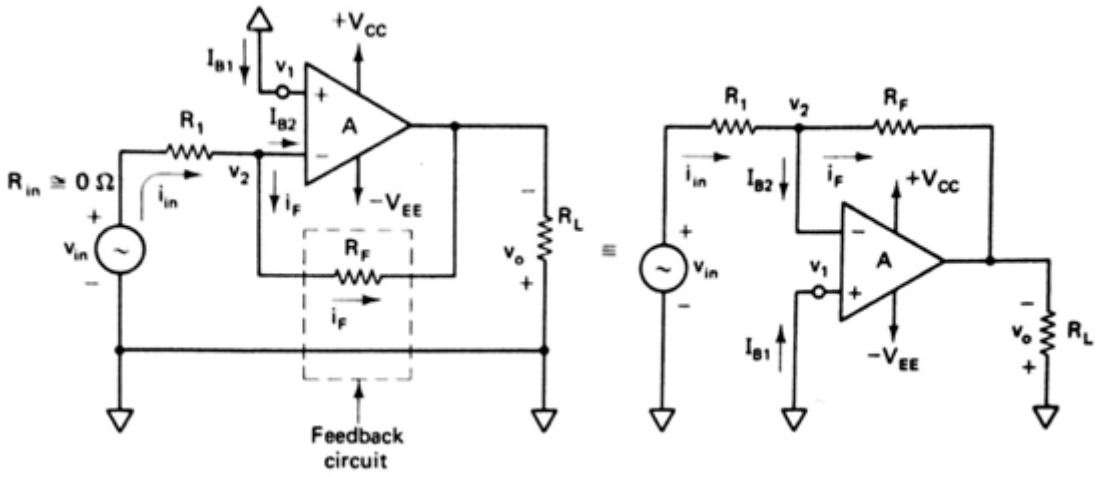

Figure 2.2: Voltage shunt feedback amplifier using opamp

Figure 2 shows the voltage shunt feedback amplifier using op-amp. The input voltage drives the inverting terminal, and the amplified as well as inverted output signal is also applied to the inverting input via feedback resistor RF.This arrangement forms a negative feedback because any increase in the output signal results in a feedback signal into the inverting input, causing a decrease in the output signal.

The noninverting terminal is grounded, and the feedback circuit has only one resistor RF. However, an extra resistor R1 is connected in series with the input signal. The different closed loop parameters for inverting op-amp are:

1. Voltage gain
2. Input and output resistances
3. Bandwidth
4. Total output offset voltage.

Voltage Gain :

Apply KCL at the input node V2,

$I_{in} = I_F + I_B$

Since input impedance is very large IB = 0,

$I_{in} \approx I_F$

$V_{IN} - V_2 R_1 = V_2 - V_0 R_F$

For non saturated output we can write,

$V_O = A V_{id}$

$$A = \frac{V_O}{V_{id}}$$

Open loop gain of op-amp is large Vid = 0 ,

$V_1 = V_2$

$V_1 = 0$, V_2 is also virtually at zero potential.
i.e $V_2 = 0$,

$$\frac{V_{in}}{R_1} = \frac{V_o}{R_F}$$

$$\frac{V_o}{V_{in}} = -\frac{R_F}{R_1} = A_F$$

Input Resistance :

The input resistance is found using millerizing the feedback resistor RF, that is , split RF into two miller component as shown in Figure 2.

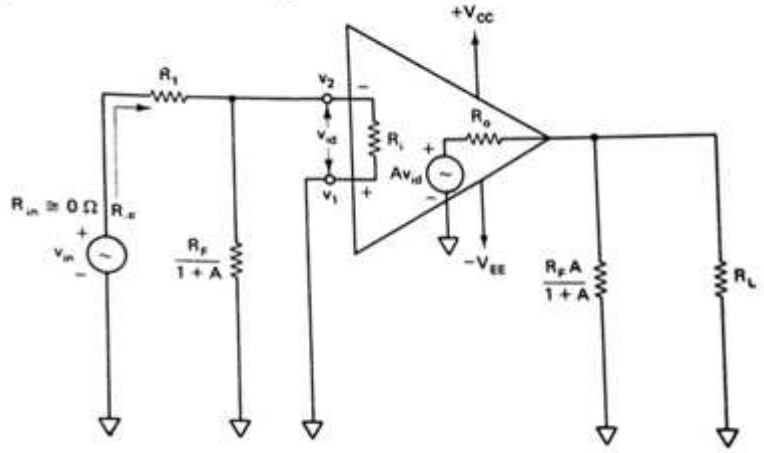

Figure 2.3:Inverting amplifierwih millerised feedback resistor

The input resistance with feedback $R_F = R_1 + \frac{R_F}{1+A} \parallel R_i$

Since Ri and A are very large,

$R_1 + \frac{R_F}{1+A} \parallel R_i = 0$

Hence,

$R_{iF}=R_1$

Output Resistance :

The output resistance with feedback RoFRoF is the resistance measured at the output terminal of the feedback amplifier. The output resistance of the noninverting amplifier was obtained by using Thevenin's theorem. Thevenin's equivalent circuit for RoFRoF of the inverting amplifier is shown in Figure 3. The RoFRoF of the inverting amplifier is identical because the output

connections in both amplifiers are the same.

$$R_{OF} = \frac{R_0}{1 + A\beta}$$

Where,

Ro= output resistance of the op-amp
A= open loop voltage gain of the op-amp

B= gain of the feedback circuit.

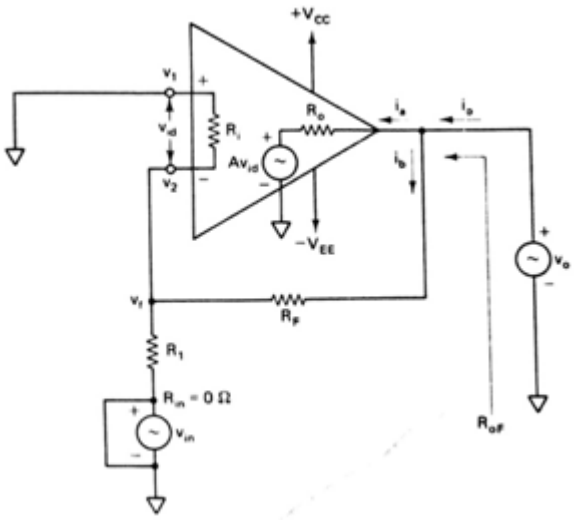

Figure 2.4:Thevenin's equivalent circuit for Ro of inverting amplifier

Bandwidth with Feedback :

The gain-bandwidth product of a single break frequency op-amp is always constant. The gain of the amplifier with feedback is always less than the gain without feedback. Therefore, the bandwidth of the amplifier with feedback fFfF must be larger than that without feedback.

$f_F = f_0(1 + A\beta)$

where

fo = break frequency of the op-amp= unity gain bandwidth / open loop voltage gain

Total Output Offset Voltage with Feedb0ack :

When temperature and power supply voltages are fixed, the output offset voltage is a function of the gain of an op-amp. The output offset voltage with feedback VooTVooT must always be smaller than that without feedback. Specially,
Total output offset voltage with feedback = total output offset voltage without feedback / 1+AB
That is,

$$V_{OOT} = \pm \frac{V_{sat}}{1 + A\beta}$$

Where

±Vsat = saturation voltages
A = open-loop voltage gain of the op-amp

B = Gain of the feedback circuit

$B=R_1/R_1+R_F$

Q3. *Draw the circuit of voltage series feedback amplifier using opamp and derive the expression for closed loop gain , input resistance with feedback, output resistance with feedback and bandwidth with feedback.*

Answer:

In a negative feedback amplifier, a small portion of the output voltage is fed back to the input. When the feedback voltage is applied in series with the signal voltage, the arrangement is Voltage Series Negative Feedback Amplifier.

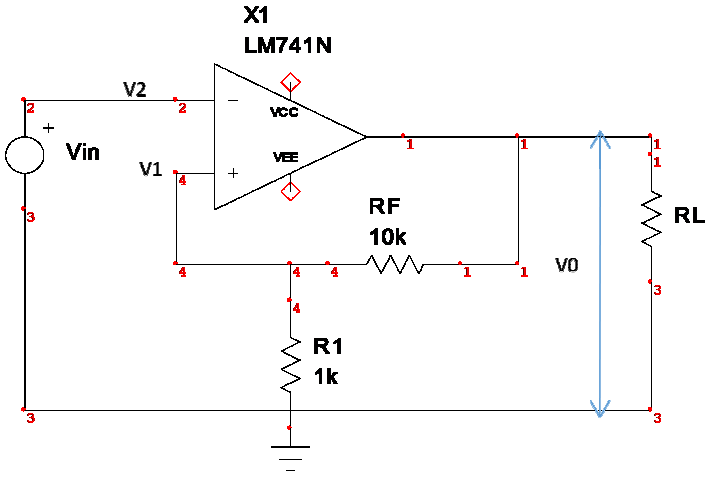

Figure 2.5: voltage series feedback amplifier using opamp

the amplifier has a voltage gain (A_v), and its output voltage (v_o) is applied to a feedback network that reduces v_o by a factor (B) to produce a feedback voltage (v_f). The feedback network may be as simple as the resistive voltage divider shown in Fig.

Negative feedback:

referring to the figure of voltage series feedback amplifier, Kirchoff's voltage equation for input loop is

$$V_{id} = V_{in} - V_f$$

where $V_{in}$is input voltage

V_f is feedback voltage

V_{id} is difference inputs voltage

From the above equation difference voltage is equal to the input voltage V_{in} minus feedback

voltage V_f .In other word feedback voltage always opposes the input voltage(or it is out of phase by 180 with respect to input voltage), hence f eedback is said to be negative.

Close loop Voltage gain :

$$Af = \frac{V0}{Vin}$$

$$V0 = A(V1 - V2)$$

referring to figure

$$V1 = Vin$$

$V2 = \text{Vf} = \frac{\text{R1V0}}{\text{R1+Rf}}$

Therefore

$V0 = A(Vin - \frac{R1Vo}{R1+Rf})$

Rearraging we get $Vo = \frac{A(R1+Rf)Vin}{R1+Rf+AR1}$

Thus $Af = \frac{Vo}{Vin} = \frac{A(R1+Rf)}{R1+Rf+AR1}$

generally A is very large(10^5) therefore

$$AR1 \gg (R1 + Rf) \; and \; R1 + Rf + AR1 \approx AR1$$

$$Af = \frac{Vo}{Vin} = 1 + \frac{Rf}{R1}$$

Gain of the feedback circuit β is the rat of Vf and V0

$$\beta = \frac{\mathrm{Vf}}{\mathrm{V0}} = \frac{\mathrm{R1}}{\mathrm{R1} + \mathrm{Rf}}$$

therefore we conclude that

$$Af = \frac{1}{\beta}$$

Block diagram representation of non inverting amplifier with feedback

close loop voltage gain Af can be expressed in terms of open loop gain and feedback ciruit gain as follows

$$Af = \frac{A(\frac{R1+Rf)}{R1+Rf)}}{\frac{R1+Rf}{R1+Rf} + \frac{AR1}{R1+Rf}}$$

$$Af = \frac{A}{1 + A\beta}$$

Af= Closed loop gain

A= open loop gain

β= gain of the feedback circuit

A β= loop gain

Difference Input voltage Ideally zero:

$$\mathrm{Vid} = \frac{\mathrm{V0}}{\mathrm{A}}$$

Since A is very large (ideally infinite)

$V_{id} \cong 0$ (1)

therefore $V_1 = V_2$ (2)

From the figure $V_1 = V_{in}$

$$V_2 = V_f$$

$$= \frac{R_1 V_o}{R_1 + R_f}$$

Substituting values of V_1 and V_2 in equation (2)

$$V_{in} = \frac{R_1 V_o}{R_1 + R_f}$$

that is

$A_F = \frac{V_0}{V_{in}} = 1 + \frac{R_F}{R_1}$

Input Resistance with Feedback:

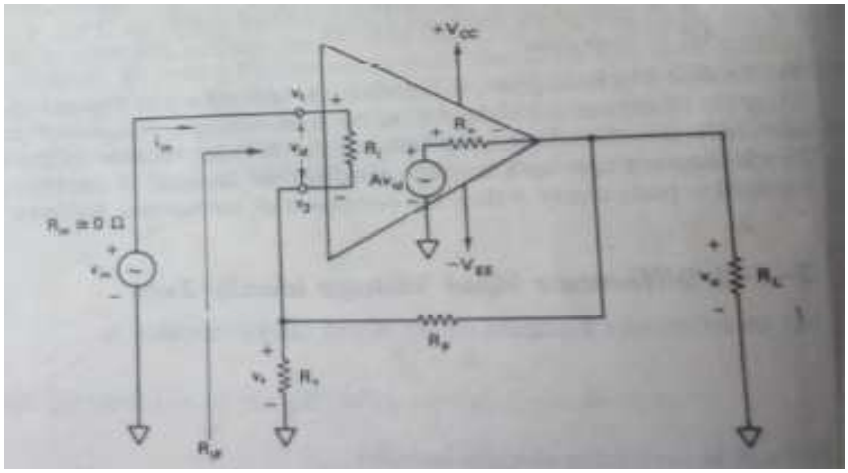

Figure 2.6:input resistance of with feedback

Figure shows voltage series feedback amplifier with the opamp equivalent circuit.In this circuit R_i is the input resistance of the opamp, and R_{iF} is the input resistance of the amplifier with feedback. The input resistance with feedback is defined as

$$R_{iF} = \frac{V_{in}}{I_{in}}$$

$$R_{iF} = \frac{V_{in}}{\frac{V_{id}}{R_i}}$$

However $V_{id} = \frac{V_0}{A}$

And $V_o = \frac{A}{1+A\beta} V_{in}$

Therefore $R_{iF} = R_i \frac{V_{in}}{\frac{V_0}{A}}$

$$= AR_i \frac{V_{in}}{\frac{AV_{in}}{(1+A\beta)}}$$

$$= R_i(1 + A\beta)$$

This means that input resistance of the opamp with feedback is $(1 + A\beta)$ times without feedback.

Output resistance with Feedback:

Output resistance is the resistance determine looking back into the feedback amplifier from output terminal as shown in figure.This resistance can be obtained by Thevenin's theorem for dependent source.To find output resistance with feedback R_{oF} ,reduce independent source V_{in} to zero, apply an external voltage V_o, and then calculate the resulting current i_o.

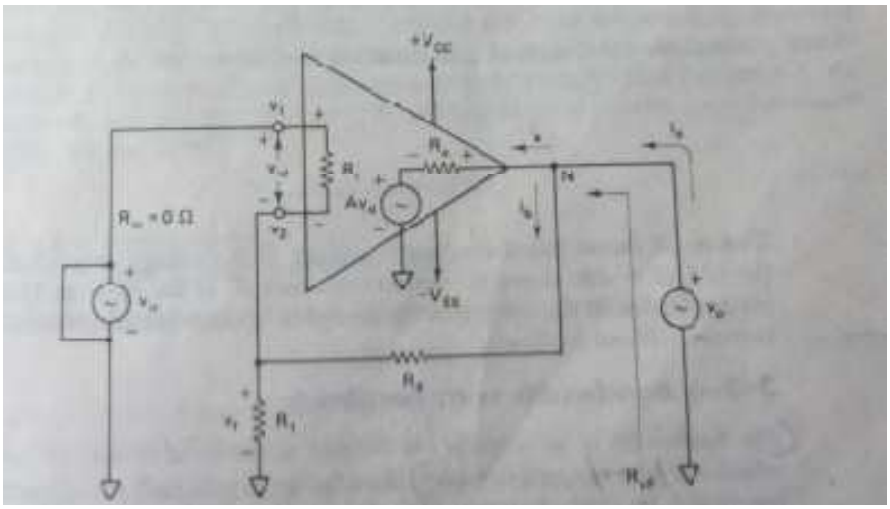

Figure 2.7:Output resistance of with feedback

In short R_{oF} is defined as follows:

$$R_{oF} = \frac{v_o}{i_o} \tag{3}$$

Writing Kirchoff's current equation at output node N, we get

$$i_o = i_a + i_b$$

Since $[(R_F + R_1) \parallel R_i] \gg R_0 \; and \; i_a \gg i_b$ therefore,

$$i_o \cong i_a$$

The current i_o can be found by writing Kirchoff's voltage equation for the output loop

$$v_o - R_o i_o - AV_{id} = 0$$

$$i_o = \frac{v_o - AV_{id}}{R_o}$$

However $V_{id} = V_1 - V_2$

$$= 0 - V_f$$

$$= -\frac{R_1 v_o}{R_1 + R_f} = -\beta v_o$$

Therefore $i_o = \frac{v_o + A\beta v_o}{R_0}$

Substituting values of io in equation 3,we get

$$R_{oF} = \frac{v_o}{\frac{v_o + A\beta v_o}{R_o}}$$

$$R_{oF} = \frac{R_o}{1 + A\beta}$$

This result shows that output resistance of voltage series feedback amplifier is 1/(1+Aβ) times output resistance R_o of the opamp.

Bandwidth with feedback:

The bandwidth of an amplifier is defined as the band of frequencies for which the gain remains constant. Manufacturer generally specify either the gain bandwidth product or supply open loop gain versus frequency curve for the opamp as shown in figure below..For 741 opamp , 5hz is the break ,the frequency at which the gain A is 3 dB down from its value at 0 Hz.

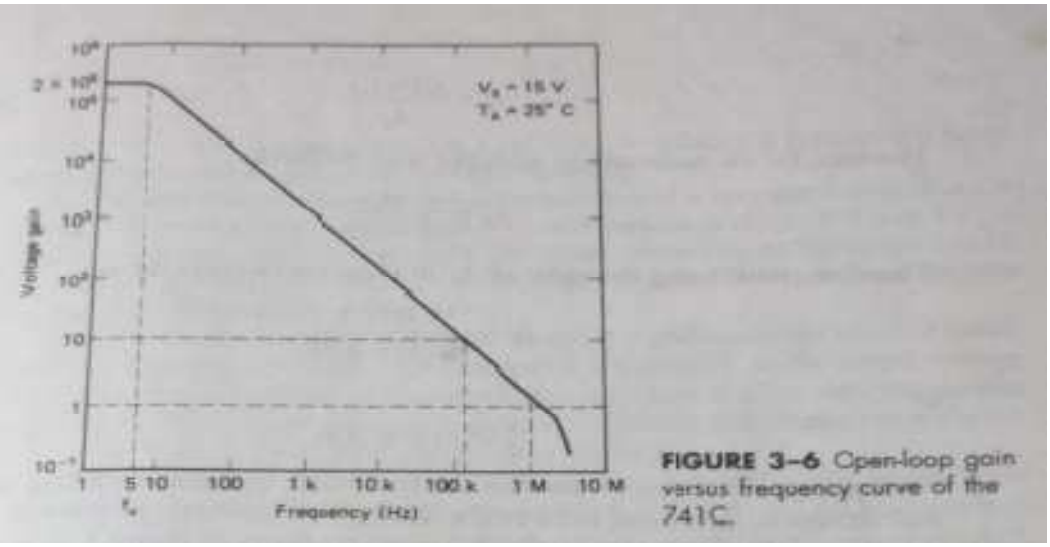

FIGURE 3–6 Open-loop gain versus frequency curve of the 741C.

Figure 2.8:Open loop gain versus frequency curve of the 741C

This is denoted by f_o .On the other hand the frequency at which gain equals to 1 is known as unity gain bandwidth (UGB).The relationship between break frequency f_o ,open loop gain A,bandwidth with feedback f_F and closed loop gain A_F can be established as follows.

$$\mathrm{UGB} = (\mathrm{A})(\mathrm{f_o})$$

Where A= Open loop voltage gain

f_o=Break frequency of opamp

or only for a single break frequency opamp

$$\mathrm{UGB} = (\mathrm{A_F})(\mathrm{F_F})$$

Where $\mathrm{A_F}$ is the close loop gain

$\mathrm{F_F}$ is bandwidth with feedback

Therefore

$(\mathrm{A})(\mathrm{f_o}) = (\mathrm{A_F})(\mathrm{F_F})$

$$f_F = \frac{(\mathrm{A})(\mathrm{f_o})}{A_F} \qquad (4)$$

For the non inverting amplifier with feedback

$$A_F = \frac{A}{1 + A\beta}$$

Therefore substituting values in equation (4),we get

$$f_F = \frac{(\mathrm{A})(\mathrm{f_o})}{\frac{A}{1+A\beta}}$$

$$f_F = f_0(1 + A\beta)$$

This shows that bandwidth of non inverting amplifier with feedback f_F is equal to its bandwidth without feedback $\mathrm{f_o}$ times $(1 + A\beta)$.

Total output offset voltage with Feedback:

$$\text{Total output offset voltage with feedback} = \frac{\text{Total output offset voltage without feedback}}{1 + \mathrm{A\beta}}$$

$$\mathrm{V_{ooT}} = \frac{\pm \mathrm{V_{sat}}}{1 + \mathrm{A\beta}}$$

Where $1/1+\mathrm{A\beta}$ is less than 1 and $\pm\ \mathrm{V_{sat}}$ is saturation voltages, maximum voltages the output of

an opamp can reach.

Q 4. *Draw the circuit of voltage follower using opamp and derive the expression for closed loop gain , input resistance with feedback, output resistance with feedback and banwidth with feedback.*

Answer:

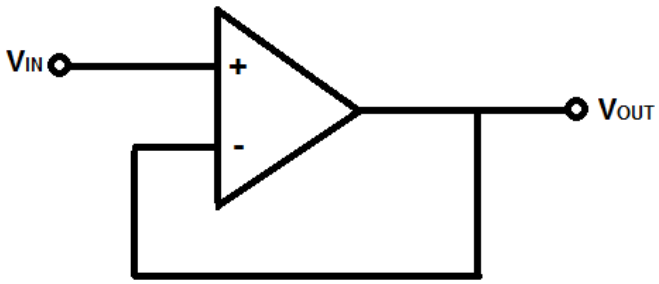

Figure 2.9 : Voltage follower

When noninverting l is configured for unity gain, it is called voltage follower because output voltage is equal to input and in phase with input.The Voltage Follower, also called a buffer does not amplify or invert the input signal but instead provides isolation between two circuits. The input impedance is very high while the output impedance is low avoiding any loading effects within the circuit. As the output is connected back directly to one of the inputs, the overall gain of the buffer is **1** .

$$Af = 1$$

$$Rif = ARi$$

$$Rof = \frac{R_0}{A}$$

$$f_F = Af_0$$

$$V_{00T} = \frac{\pm V_{SAT}}{A}$$

Q 5. *For the non inverting amplifier using opamp R_1=1 KΩ ,R_f=10KΩ and the opamp used has A=2*10^5 , R_i= 2M Ω, R_o=75Ω ,UGB=1MHz, ±V_{sat} =±13v . Determine closed loop gain , input and output resistance with feedback, bandwidth with feedback and total output offset voltage with feedback.*

Answer:

$$\beta = \frac{R1}{R1+Rf} = \frac{1k}{1k+10k} = \frac{1}{11}$$

$$1 + A\beta = 1 + 20000 \times \frac{1}{11} = 18182\,.8$$

$$A_F = \frac{A}{1+A\beta} = \frac{200000}{18182.8} = 10.99$$

$$R_{iF} = R_i(1 + A\beta) = 2M(1 + 18182.8) = 36.4G\Omega$$

$$R_{oF} = \frac{75}{18.182.8} = 4.12m\Omega$$

$$f_F = 5 \times 18182.8 = 90.9\ kHz$$

$$V_{ooT} = \frac{\pm 13}{18182.8} = \pm 0.715\ mV$$

Q 6. *For the inverting amplifier using opamp R_1= 470Ω ,R_f = 4.7KΩ and the opamp used has A=2*10^5 , R_i= 2M Ω, R_o=75Ω ,UGB=1MHz, ±V_{sat} =±13v . Determine closed loop gain , input and output resistance with feedback, bandwidth with feedback and total output offset voltage*

with feedback.

Answer:

$$k = \frac{R_f}{R_1 + R_f} = \frac{4700}{470 + 4700} = \frac{1}{1.1}$$

$$\beta = \frac{R_1}{R_1 + R_f} = \frac{470}{470 + 4700} = \frac{1}{11}$$

$$1 + A\beta = 1 + 20000 \times \tfrac{1}{11} = 18182.8$$

$$A_F = -\frac{R_f}{R_1} = \frac{4700}{470} = -10$$

$$R_{iF} = R_1 + \frac{R_f}{1 + A} \parallel R_i = 470 + \frac{4700}{1 + 20000} \parallel 2M = 470\Omega$$

$$R_{oF} = \frac{R_o}{1 + A\beta} = \frac{75}{18.182.8} = 4.12m\Omega$$

$$f_F = \frac{5 \times 18182.8}{\frac{1}{1.1}} = 100\ kHz$$

$$V_{ooT} = \frac{\pm V_{SAT}}{1 + A\beta} = \frac{\pm 13}{18182.8} = \pm 0.715\ mV$$

Q.7 *For the voltage follower using opamp R_1=1 KΩ ,R_f =10KΩ and the opamp used has A=2*10^5 , R_i= 2M Ω, R_o=75Ω ,UGB=1MHz, ±V_{sat} =±13v . Determine closed loop gain , input and output resistance with feedback, bandwidth with feedback and total output offset voltage with feedback.*

Answer:

$Af = 1$

$R_{if} = ARi = 20000 \times 2M = 400G\Omega$

$Rof = \dfrac{R_0}{A} = \dfrac{75}{20000} = 0.375m\Omega$

$f_F = Af_0 = 20000 \times 5 = 1MHz$

$V_{00T} = \dfrac{\pm V_{SAT}}{A} = \dfrac{\pm 13}{20000} = \pm 65\mu V$

Q 8.*For the inverting amplifier R1= 4.7 k and Rf = 470k .Determine maximum possible output offset voltage due to i) The input offset voltage Vio ii) The input bias current IB iii) What value of ROM is needed to reduce the effect of input bias current IB? Use opamp 741 type.*

Answer:

Inverting Amplifier with R_1= 4.7 k and R_f = 470k, I_{io}=200nA,I_B= 500nA

$Vo_{Iio} = R_f I_{io} = 470k \times 200nA = 94mV$

$Vo_{IB} = R_f I_B = 470k \times 500nA = 235mV$

$R_{oM} = R_1 \parallel R_f = 4.7k \parallel 470k = 4.653k\Omega$

Q. 9.*The op–amp used as non inverting amplifier with R_1 = 47 kΩ R_F = 470 kΩ The opamp has input offset voltage of 10 mv. Calculate the maximum output offset voltage caused by V_{IO}. Also design the compensation network for V_{IO}.*

Answer: Noninverting Amplifier with R_1 = 47 kΩ, R_F = 470 kΩ , V_{IO}= 10mv.

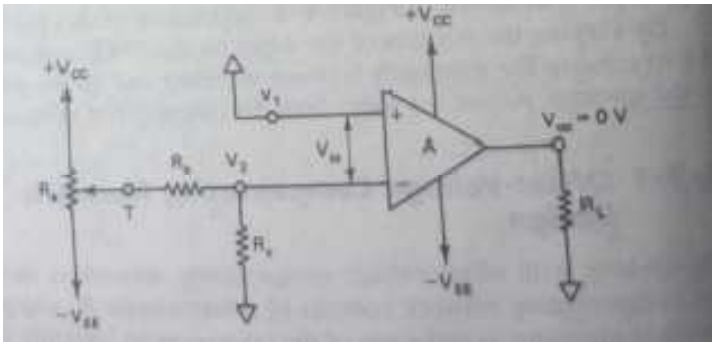

Figure 2.10 : non inverting amplifier with Compensation

$V_{oo} = (1 + \frac{R_f}{R_1})$ V_{IO}

$= \left(1 + \frac{470k}{47k}\right) 10mv = 0.11v$

Compensation network

$V_{IO} = \frac{R_c}{R_b} \times V_{max}$

$V_{max} = \pm V_{cc} = \pm 15v$

Let R_c= 10Ω

$R_b = R_c \frac{V_{max}}{V_{IO}}$

$= 10 \times \frac{15}{10m} = 15k\Omega$

$R_b \gg \frac{R_a}{4}$

$R_b = 10 \times \frac{R_a}{4}$

$R_a = 6K\Omega$

Therefore
$R_a = 6K\Omega$,
$R_b = 15K\Omega$

$R_c = 10\Omega$

Q.10.The *OP-amp used as inverting amplifier has following specification $\Delta V_{io}/\Delta T$ = 25uV/°C, $\Delta I_{io}/\Delta T$ = 15 nA/°C. The amplifier uses R_1 = 100Ω and R_f = 8.2kΩ, $+V_{ss}$ =± 15v and is nulled at 25°C. A sine wave of l0mv peak amplitude at 100 Hz is applied as input to the circuit. Draw the output voltage waveform at 25°C and 45°C.*

Answer: inverting amplifier $\Delta V_{io}/\Delta T$ = 25uV/°C, $\Delta I_{io}/\Delta T$ = 15 nA/°C, R_1 = 100Ω and R_f = 8.2kΩ, $+V_{ss}$ =± 15v

$\Delta T = 45 - 25 = 20$

$$\Delta V_{ooT_{45}} = \left(1 + \frac{R_f}{R_1}\right)\left(\frac{\Delta V_{IO}}{\Delta T}\right) \times \Delta T + R_f \left(\frac{\Delta I_{IO}}{\Delta T}\right) \times \Delta T$$

$$= \left(1 + \frac{8.2k}{100}\right)(25uv) \times 20 + 8.2k \times (15nA\ ) \times 20$$

$$= 0.0415 + 0.00246$$

$$= 43.95mv$$

$$Vo_{25} = -\frac{R_f}{R_1} \times Vin_p$$

$$= -\frac{8.2k}{100} \times 10mv$$

$$= -0.8v$$

$$Vo_{45} = -0.8v \pm 43.95mv$$

$$= -.84395v \; or \; -0.75065v$$

Unit-3

Linear Applications of Operational Amplifier

Q.1. *Draw the circuit of Inverting summer amplifier and derive the expression for output voltage.*

Answer:

The configuration is shown in figure. With three input voltages va, vb & vc. Depending upon the value of Rf and the input resistors Ra, Rb, Rc the circuit can be used as a summing amplifier, scaling amplifier, or averaging amplifier.

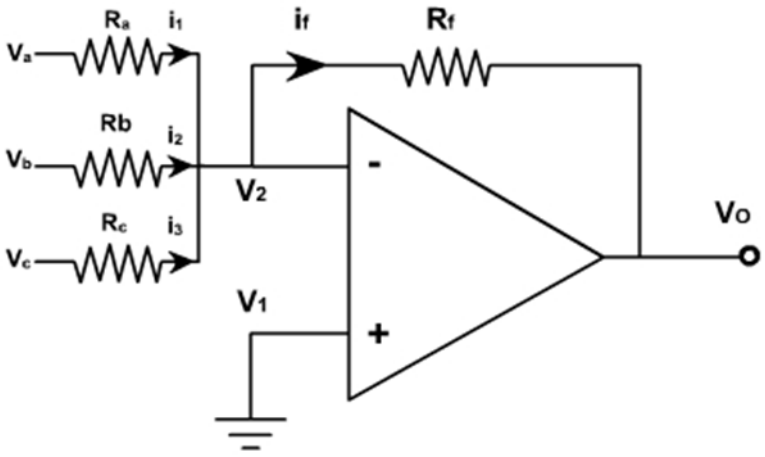

Figure 3. 1 Inverting Summing Amplifier

Again, for an ideal OPAMP, $V_1 = V_2$. The current drawn by OPAMP is zero. Thus, applying KCL at V_2 node

$$i_1 + i_2 + i_3 = i_f$$

$$\frac{V_a}{R_a}+\frac{V_b}{R_b}+\frac{V_c}{R_c}=-\frac{V_o}{R_f}$$

$$V_o=-\left(\frac{R_f}{R_a}V_a+\frac{R_f}{R_b}V_b+\frac{R_f}{R_c}V_c\right)$$

If in the circuit shown $R_a=R_b=R_c=R$

$$V_o=-\frac{R_f}{R}(V_a+V_b+V_c)$$

This means that the output voltage is equal to the negative sum of all the inputs times the gain of the circuit R_f/ R; hence the circuit is called a summing amplifier. When $R_f= R$ then the output voltage is equal to the negative sum of all inputs.

$$V_o=-(V_a+V_b+V_c)$$

If each input voltage is amplified by a different factor in other words weighted differently at the output, the circuit is called then scaling amplifier.

$$\frac{R_f}{R_a}\neq\frac{R_f}{R_b}\neq\frac{R_f}{R_c}$$

$$V_o=-\left(\frac{R_f}{R_a}V_a+\frac{R_f}{R_b}V_b+\frac{R_f}{R_c}V_c\right)$$

The circuit can be used as an averaging circuit, in which the output voltage is equal to the average of all the input voltages.

In this case, $R_a= R_b= R_c = R$ and $R_f / R = 1 / n$ where n is the number of inputs. Here $R_f / R = 1 / 3$.

$$V_o=-\frac{(V_a+V_b+V_c)}{3}$$

In all these applications input could be either ac or dc.

Q.2. *Draw the circuit of Non-Inverting summer amplifier and derive the expression for output voltage.*

If the input voltages are connected to non-inverting input through resistors, then the circuit can be used as a summing or averaging amplifier through proper selection of R_a, R_b, $R_c$and R_f. as shown in fig. 3.

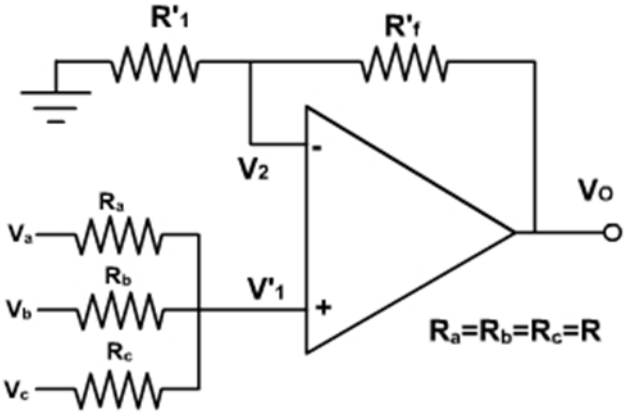

Figure 3. 2 Non-Inverting Summing Amplifier

To find the output voltage expression, V_1 is required. Applying superposition theorem, the voltage V_1 at the non-inverting terminal is given by

$$V_1 = \left(\left(\frac{R_b \| R_c}{R_a}\right)V_a + \left(\frac{R_a \| R_c}{R_b}\right)V_b + \left(\frac{R_a \| R_b}{R_c}\right)V_c\right)$$

For $R_a = R_b = R_c = R$

$$V_1 = \left(\left(\frac{R/2}{R + R/2}\right)V_a + \left(\frac{R/2}{R + R/2}\right)V_b + \left(\frac{R/2}{R + R/2}\right)V_c\right)$$

$$V_1 = \frac{(V_a + V_b + V_c)}{3}$$

Hence the output voltage is

$$V_o = \left(1 + \frac{R_f}{R_1}\right) V_1 = \left(1 + \frac{R_f}{R_1}\right)\left(\frac{(V_a + V_b + V_c)}{3}\right)$$

This shows that the output is equal to the average of all input voltages times the gain of the circuit (1+ Rf / R1), hence the name averaging amplifier.

If (1+Rf/ R1) is made equal to 3 then the output voltage becomes sum of all three input voltages.

$$V_o = V_a + V_b + V_c$$

Hence, the circuit works as non-inverting summing amplifier.

Q.3. *Determine the gain V_O / V_i of the circuit of figure 3.3*

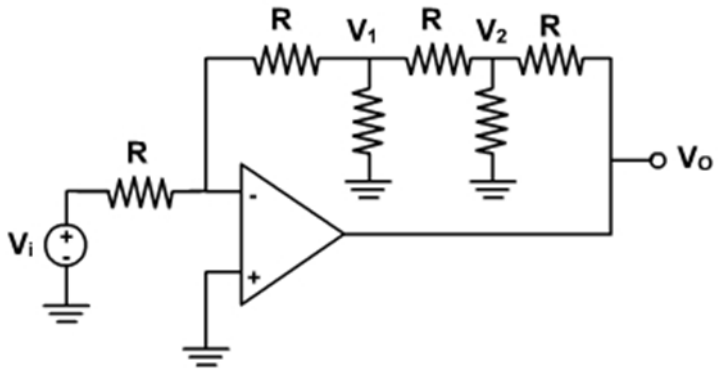

Figure 3. 3 Circuit for Q.3.

Solution:

Applying KCL at inverting node of OP-AMP

$$\frac{V_i - 0}{R} = \frac{0 - V_1}{R}$$

$$\frac{V_i}{R} = \frac{-V_1}{R}$$

$$V_1 = -V_i$$

Applying KCL to node V_1,

$$\frac{0 - V_1}{R} = \frac{V_1}{R} + \frac{V_1 - V_2}{R}$$

$$\frac{V_2}{R} = \frac{-3V_1}{R}$$

$$V_2 = -3V_1 = -3V_i$$

Applying KCL to node V_2,

$$\frac{V_1 - V_2}{R} = \frac{V_2}{R} + \frac{V_2 - V_0}{R}$$

$$\frac{V_o}{R} = \frac{3V_2}{R} - \frac{V_1}{R}$$

$$\frac{V_o}{R} = \frac{9V_i}{R} - \frac{V_i}{R}$$

$$V_o = -8V_i$$

$$\frac{V_o}{V_i} = -8$$

Q.4. *Find the relationship between V_O and V_1 through V_6 in the circuit of* ***figure 3.4***

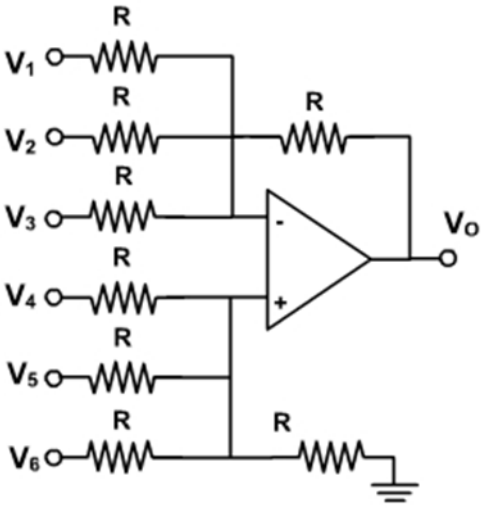

Figure 3. 4 Circuit for Q.4

Solution:

Let's consider of V1 (singly) by shorting the others i.e. the circuit then looks like as shown in **fig. 3.5.**

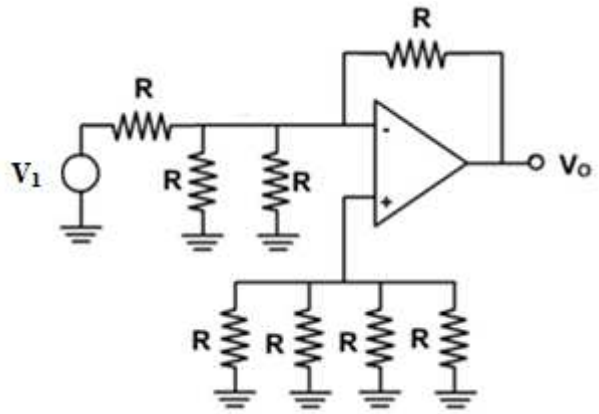

Figure 3. 5 Circuit with superposition theorem-1

The circuit behaves as simple inverting amplifier and V_{o1} is given by

$$V_{o1} = -\frac{R}{R}V_1 = -V_1$$

The circuit considering V_2 and V_3 is also same and output V_{o2} and V_{o3} is given by

$$V_{o2} = -\frac{R}{R}V_2 = -V_2 \text{and} V_{o3} = -\frac{R}{R}V_3 = -V_3$$

Let as now consider the case of V_4 with other inputs shorted, circuit looks like as shown in **figure 3.6**

V_4

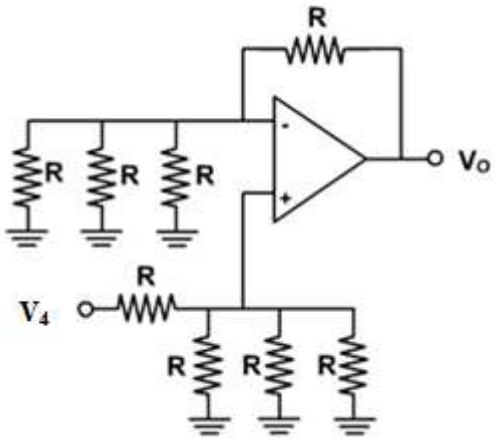

Figure 3. 6 Circuit with superposition theorem-2

The non-inverting potential is now given by

$$V_{N4} = \frac{R/_3}{R + R/_3} V_4$$

The output voltage Vo_4 due to V_4 if of non-inverting given by

$$V_{o4} = \left(1 + \frac{R}{R/_3}\right) V_{N4}$$

$$V_{o4} = \left(1 + \frac{R}{R/_3}\right) \times \frac{R/_3}{R + R/_3} V_4$$

$$V_{o4} = V_4$$

The circuit considering V_5 and V_6 is also same and output V_{o5} and V_{o6} is given by

$$V_{o5} = V_5 \qquad \text{and} \qquad V_{o6} = V_6$$

The total output voltage is given by

$$V_o = V_{01} + V_{02} + V_{03} + V_{04} + V_{05} + V_{06}$$

$$V_o = -V_1 - V_2 - V_3 + V_4 + V_5 + V_6$$

Q.5. *Show that the circuit of **figure 3.7** has $A = V_O / V_i = - K (R_2 / R_1)$ with $K = 1 + R_4 / R_2 + R_4 / R_3$, and $R_i = R_1$.Also specify resistance not larger than 100 K to achieve $A = -200$ V / V and $R_i = 100$ K.*

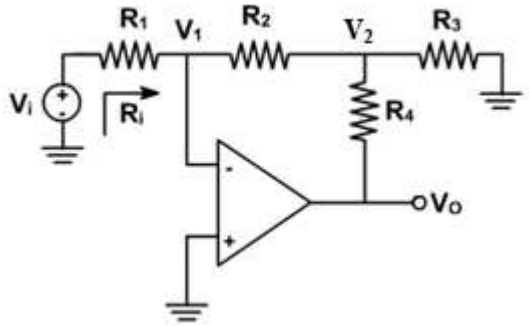

Figure 3. 7 Circuit for Q.5

Solution:

Applying KCL at inverting node,

$$\frac{V_i - V_1}{R_1} = \frac{V_1 - V_2}{R_2}$$

$$\frac{V_i}{R_1} = \frac{-V_2}{R_2}$$

$$V_2 = -V_i \frac{R_2}{R_1}$$

Applying KCL at feedback node V_2,

$$\frac{V_1 - V_2}{R_2} = \frac{V_2 - V_o}{R_4} + \frac{V_2}{R_3}$$

$$\frac{-V_2}{R_2} = \frac{V_2 - V_o}{R_4} + \frac{V_2}{R_3}$$

$$\frac{V_i}{R_1} = \frac{-V_i \frac{R_2}{R_1} - V_o}{R_4} + \frac{-V_i \frac{R_2}{R_1}}{R_3}$$

$$\frac{V_i}{R_1} = \frac{-V_i R_2 - V_o R_1}{R_1 R_4} + \frac{-V_i R_2}{R_1 R_3}$$

$$V_i R_3 R_4 = -V_i R_2 R_3 - V_o R_1 R_3 - V_i R_2 R_4$$

$$V_i(R_3 R_4 + R_2 R_3 + R_2 R_4) = -V_o R_1 R_3$$

$$\frac{V_o}{V_i} = -\left(\frac{R_3 R_4 + R_2 R_3 + R_2 R_4}{R_1 R_3}\right)$$

$$\frac{V_o}{V_i} = -\frac{R_2}{R_1}\left(\frac{R_4}{R_2} + \frac{R_4}{R_3} + 1\right)$$

$$\frac{V_o}{V_i} = -\frac{R_2}{R_1}\left(1 + R_4\left(\frac{R_2 + R_3}{R_2 R_3}\right)\right)$$

$$\frac{V_o}{V_i} = -k\frac{R_2}{R_1}$$

where

$$k = \left(1 + R_4\left(\frac{R_2 + R_3}{R_2 R_3}\right)\right)$$

The circuit is inverting configuration therefore $R_i=R_1=100K\Omega$

Given $R_i=100K$ and $R_1= R_2= R_4=100K$

$$\left|\frac{V_o}{V_i}\right| = \frac{R_2}{R_1}\left(1 + R_4\left(\frac{R_2 + R_3}{R_2 R_3}\right)\right) = 200$$

$$1 + 100K\left(\frac{100K + R_3}{100K R_3}\right) = 200$$

$$R_3 = 505\Omega$$

Q.6. *Find V_{out} and i_{out} for the circuit shown in figure 3.8 . The input voltage is sinusoidal with amplitude of 0.5 V.*

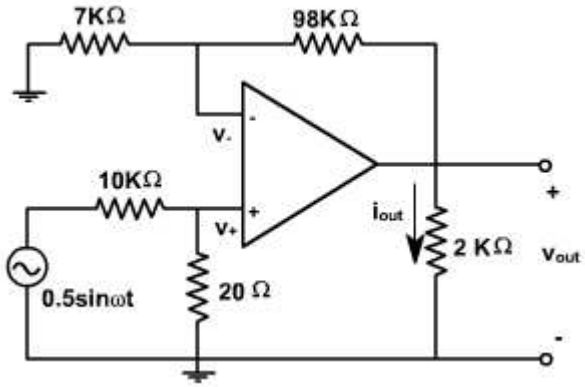

Figure 3. 8 Circuit for Q.6

Solution:

We begin by writing the KCL equations at both the + and – terminals of the op-amp.

Apply KVL at the inverting terminal,

$$\frac{V_- - V_{out}}{9.8 \times 10^4} + \frac{V_- - 0}{7000} = 0$$

Therefore,

$$15V_- = V_{out}$$

For the positive terminal,

$$\frac{V_+ - V_{in}}{10^4} + \frac{V_+ - 0}{2 \times 10^4} = 0$$

This yields two equations in three unknowns, V_{out}, V_+ and V_-. The third equation is the relationship between V_+ and V_- for the ideal OPAMP,

$V_+ = V_-$

Solving these equations, we find

$$V_{out} = 10V_{in} = 5 \sin \omega t \; V$$

Since 2 kΩ resistor forms the load of the op-amp, then the current i_{out} is given by

$$i_{out} = \frac{V_{out}}{R_L} = \frac{5 \sin \omega t}{2K\Omega} = 2.5 \sin \omega t \;\; mA$$

Q.7. *For the different amplifier shown in* ***figure3.9*** *verify that* $\boldsymbol{V_o = -\left(1 + \frac{2R_2}{R_3}\right)\frac{R_f}{R_1}\left(V_x - V_y\right)}$

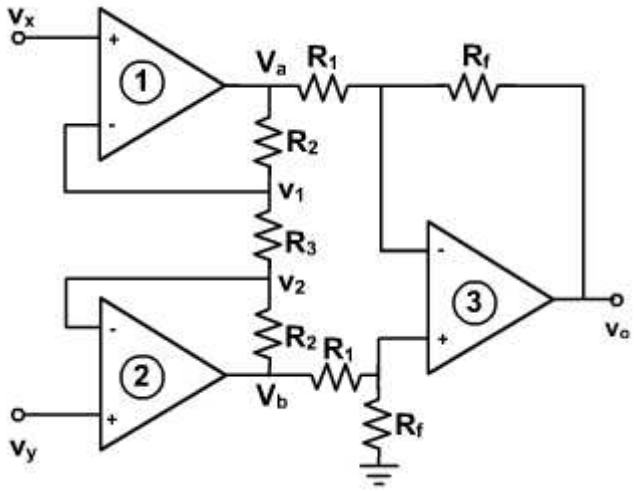

Figure 3. 9 Circuit for Q.7

Solution:

Since the differential input voltage of OPAMP is negligible, therefore,

$V_1 = V_x$
and $V_2 = V_y$

The input impedance of OPAMP is very large and, therefore, the input current of OPAMP is negligible.

Thus

$$\frac{V_a - V_1}{R_2} = \frac{V_1 - V_2}{R_3}$$

$$\frac{V_a - V_x}{R_2} = \frac{V_x - V_y}{R_3}$$

$$V_a = \frac{R_2}{R_3}(V_x - V_y) + V_x$$

And

$$\frac{V_1 - V_2}{R_3} = \frac{V_2 - V_b}{R_2}$$

$$\frac{V_x - V_y}{R_3} = \frac{V_y - V_b}{R_2}$$

$$V_b = V_y - \frac{R_2}{R_3}(V_x - V_y)$$

The OPAMP3 is working as differential amplifier, therefore,

$$V_o = \frac{R_f}{R_1}(V_b - V_a)$$

$$V_o = \frac{R_f}{R_1}\left\{V_y - V_x - 2\frac{R_2}{R_3}(V_x - V_y)\right\}$$

$$V_o = -\left(1 + \frac{2R_2}{R_3}\right)\frac{R_f}{R_1}(V_x - V_y)$$

Q.8. *Prove that the network shown in figure is a non-inverting integrator with.*

$$\boldsymbol{V_o = \frac{2}{RC}\int V_s(t)dt}$$

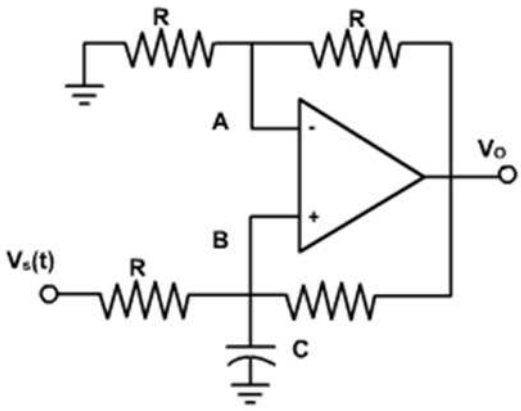

Figure 3. 10 Circuit for Q.8

Solution:

The voltage at point A is V_O / 2 and it is also the voltage at point B because difference input voltage is negligible.

$V_B = V_O / 2$

Therefore, applying Node current equation at point B,

$$\frac{V_B - V_A}{R} + \frac{V_B - V_o}{R} + C\frac{dV_B}{dt} = 0$$

$$\frac{2V_B}{R} - \frac{V_s}{R} - \frac{V_o}{R} + C\frac{dV_B}{dt} = 0$$

$$\frac{V_o}{R} - \frac{V_s}{R} - \frac{V_o}{R} + \frac{C}{2}\frac{dV_o}{dt} = 0$$

$$\frac{dV_o}{dt} = \frac{2V_s}{RC}$$

$$V_o = \frac{\mathbf{2}}{\boldsymbol{RC}}\int \boldsymbol{V_s(t)dt}$$

Q.9. *For the circuit shown in figure 3.11 prove that*

$$\boldsymbol{V_o = \left(1 + \frac{R_2}{R_1}\right)\left(V_2 - \frac{1+{R_3}/{R_4}}{1+{R_1}/{R_2}}\right)}$$

Also verify that if $R_3 / R_4 = R_1 / R_2$, the circuit is an instrumentation amplifier with gain $A = 1 + R_2 / R_1$.

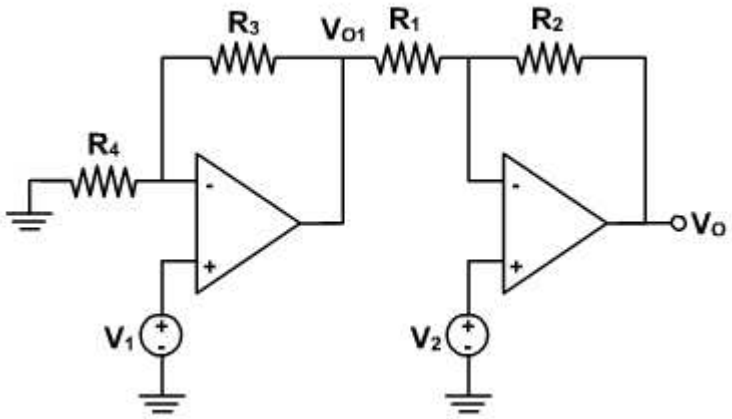

Figure 3. 11 Circuit for Q.9

Solution:

Here

$$V_{o1} = \left(1 + \frac{R_3}{R_4}\right) V_1$$

$$V_o = -\frac{R_2}{R_1} V_{o1} + \left(1 + \frac{R_2}{R_1}\right) V_2$$

$$V_o = -\frac{R_2}{R_1}\left(1+\frac{R_3}{R_4}\right)V_1 + \left(1+\frac{R_2}{R_1}\right)V_2$$

$$V_o = \left(1+\frac{R_2}{R_1}\right)\left(V_2 - \frac{\frac{R_2}{R_1}\left(1+\frac{R_3}{R_4}\right)}{\left(1+\frac{R_2}{R_1}\right)}V_1\right)$$

$$V_o = \left(1+\frac{R_2}{R_1}\right)\left(V_2 - \frac{\left(1+\frac{R_3}{R_4}\right)}{\left(1+\frac{R_1}{R_2}\right)}V_1\right)$$

b). If $\frac{R_3}{R_4} = \frac{R_1}{R_2}$

$$V_o = \left(1+\frac{R_2}{R_1}\right)\left(V_2 - \frac{\left(1+\frac{R_1}{R_2}\right)}{\left(1+\frac{R_1}{R_2}\right)}V_1\right)$$

$$V_o = \left(1+\frac{R_2}{R_1}\right)(V_2 - V_1)$$

So in this condition circuits as an instrument amplifier with gain $\left(1+\frac{R_2}{R_1}\right)$

Q.10. *Obtain an expression of the type $i_O = V_i / R - V_O / R_O$ for the circuit shown in fig. 6. Hence verify that if $R_4 / R_3 = R_2 / R_1$ the circuit is a V-I converter with $R_O = \infty$* and $R = R_1 R_5 / R_2$.

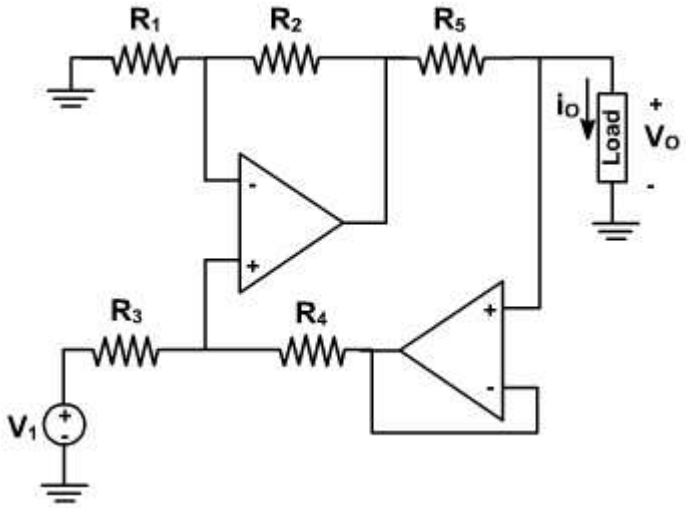

Figure 3. 12 Circuit for Q.10

Solution:

Here

$$V_x = V_0 + \frac{V_i - V_0}{R_3 + R_4} . R_4$$

$$= V_0 + \frac{V_i R_4}{R_3 + R_4} - \frac{V_0 R_4}{R_3 + R_4}$$

$$= \frac{V_i R_4}{R_3 + R_4} + \frac{V_0 R_3}{R_3 + R_4}$$

$$V_{01} = \left(1 + \frac{R_2}{R_1}\right) V_x = \frac{R_4}{R_3 + R_4} \left(1 + \frac{R_2}{R_1}\right) V_i + \frac{R_3}{R_3 + R_4} \left(1 + \frac{R_2}{R_1}\right) V_0$$

i_O = current through the resistor.

$$= \frac{V_{01} - V_0}{R_5}$$

$$= \frac{R_4}{R_5(R_3 + R_4)}\left(1 + \frac{R_2}{R_1}\right)V_i + \frac{R_3}{R_5(R_3 + R_4)}\left(1 + \frac{R_2}{R_1}\right)V_0 - \frac{V_0}{R_5}$$

$$= \frac{1 + (R_2/R_1)}{R_5\left(1 + \frac{R_3}{R_4}\right)}V_i + \frac{\left(1 + \frac{R_2}{R_1}\right)V_0}{R_5\left(1 + \frac{R_4}{R_3}\right)} - \frac{V_0}{R_5}$$

$$= \frac{V_i}{R} - \frac{V_0}{R_0}$$

Where

$$R = \frac{R_5\left(1 + \frac{R_3}{R_4}\right)}{\left(1 + \frac{R_2}{R_1}\right)}$$

$$R_0 = \frac{R_5}{\frac{1 + R_2/R_1}{1 + R_4/R_3} - 1}$$

So when

$$\frac{R_4}{R_3} = \frac{R_2}{R_1}$$

then,

$$R = \frac{R_5\left(1+\dfrac{R_3}{R_4}\right)}{\dfrac{R_1}{R_2}\left(1+\dfrac{R_2}{R_1}\right)} = \frac{R_5\,R_2}{R_1}$$

$$R_0 = \frac{R_5}{\dfrac{1+R_2/R_1}{1+R_4/R_3}-1} = \frac{R_5}{1-1} \to \infty$$

UNIT No 4

ACTIVE FILTERS Of Operational Amplifier

Q1. *Draw the circuit of First order low pass filter and derive the expression for cut-off frequency*
Answer:

First order low pass filter uses an RC network for filtering. Resistor R_1 and R_F determine gain of the filter.

According to the voltage divider rule , voltage at the noninverting terminal is

$$v_1 = \frac{-jX_c}{R - jX_c} v_{in} \qquad (1)$$

Where $j = \sqrt{-1}$ and $-jX_c = \frac{1}{j2\pi fC}$

Simplifying equation (1) we get

$$v_1 = \frac{v_{in}}{1 + j2\pi fRC}$$

And output voltage $v_o = \left(1 + \frac{R_F}{R_1}\right) v_1$

That is $v_0 = \left(1 + \frac{R_F}{R_1}\right) \frac{v_{in}}{1+j2\pi fRC}$

Or $\frac{v_o}{v_{in}} = \frac{A_F}{1+j(\frac{f}{f_H})}$

Where $\frac{v_o}{v_{in}}$ = gain of the filter

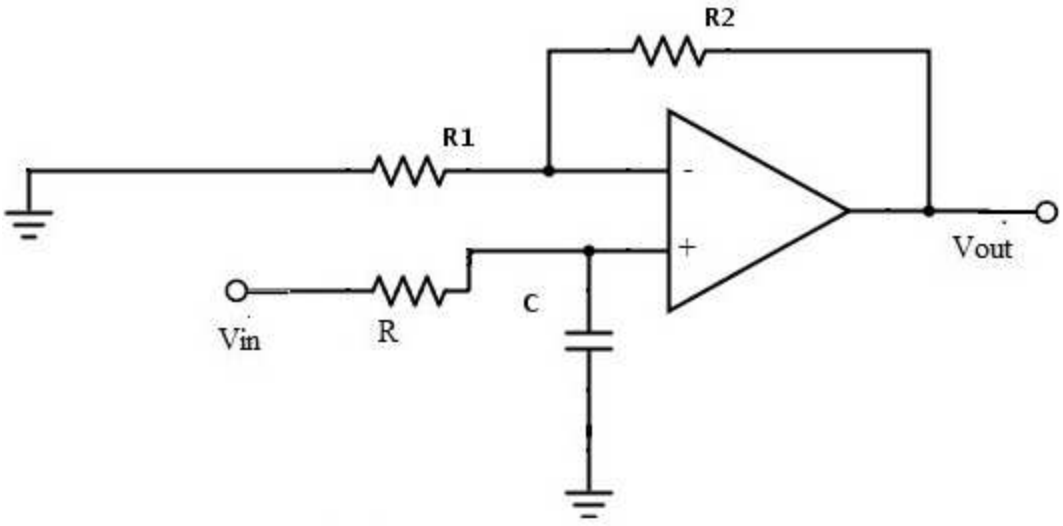

Figure 4.1: First order low pass butterworth filter circuit

The gain angd phase angle equation of low pass filter can be obtained as

$$\left|\frac{v_0}{v_{in}}\right| = \frac{A_F}{\sqrt{1+\left(\frac{f}{f_H}\right)^2}}$$

$$\varphi = -tan^{-1}\left(\frac{f}{f_H}\right)$$

Where φ is phase angle in degrees.

The operation of low pass filter can be verified from the gain magnitude equation as

1. At very low frequencies ,that is $f < f_H$,

$$\left|\frac{v_0}{v_{in}}\right| \cong A_F$$

2. At $f = f_H$,

$$\left|\frac{v_0}{v_{in}}\right| \cong \frac{A_F}{\sqrt{2}} = 0.707A_F$$

3. $f > f_H$,

$$\left|\frac{v_0}{v_{in}}\right| > A_F$$

Thus low pass filter has a constant gain A_F from 0 Hz to high cut off frequency $f_{H.}$ At f_H the gain is 0.707 A_F and after f_H it decreses at a constant rate with an increase in frequency.The frequency $f = f_H$ is called cut off frequency because the gain of the filter at high frequency is down by 3 db from 0 Hz.

Q.2 Design a low cut off frequency of 1 kHz with a passband gain of 2.

Answer:

Select f_H =1 kHz.

Let C= 0.01uF

$$R = \frac{1}{2\pi f_H C} = \frac{1}{2\pi(1k)(10^{-8})} = 15.9k\Omega$$

Since passband gain is 2, R_1 and R_F must be equal .

Let $R_1 = R_F$ = 10 kΩ

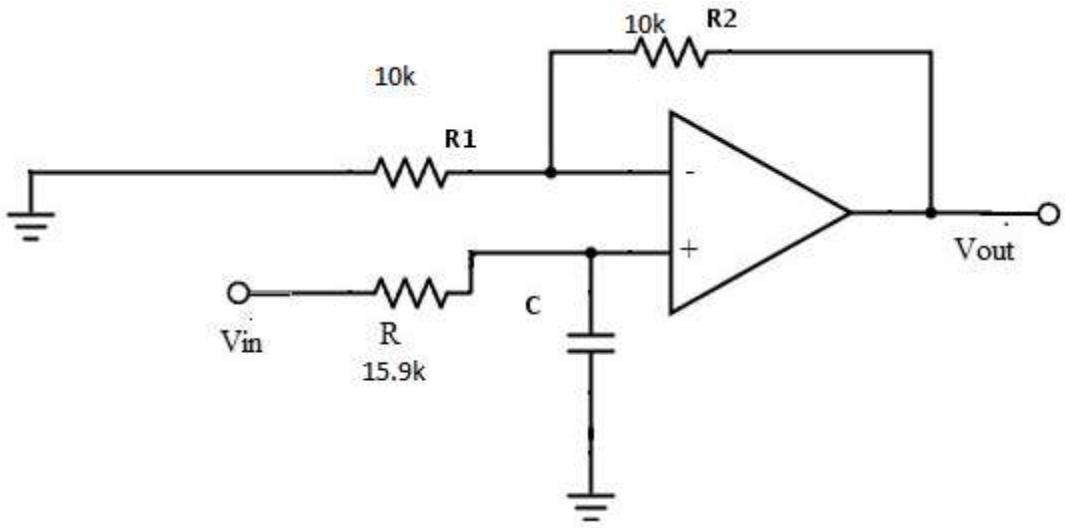

Figure 4.2: Design of First order low pass butterworth filter circuit

Q.3 Draw the circuit of second order high pass filter and derive the expression for cut-off requency show that the gain roll off rate in stop band is 40db/decade.

Answer:

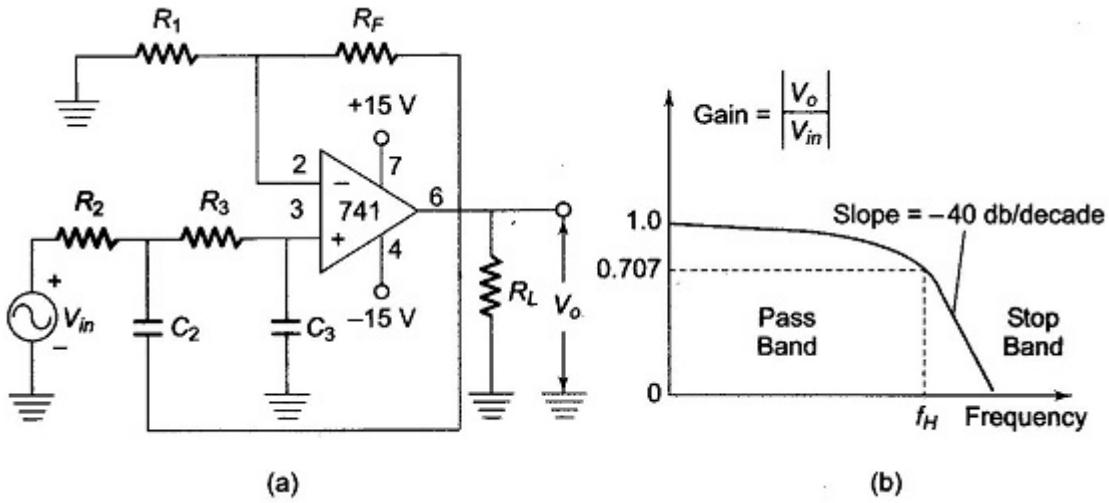

Figure 4.3 : (a) second order low pass butterworth filter circuit (b) second order low pass butterworth filter frequency responce

A first order low pass filter can be converted into a second order type simply by using an additional RC network.Second order filter are important because higher order filters can be designed using them.the gain of second order filter is set by R_1 and R_F while high cutoff frequency f_H is determined by R_2,C_2,R_3,C_3 as follows

$$f_H = \frac{1}{2\pi\sqrt{R_2R_3C_2C_3}}$$

In the circuit all the components and the circuit parameters are expressed in the S domain where S = jw.

Writing Kirchoff's current law at node $V_A(S)$,

$$I_1 = I_2 + I_3$$

Or

$$\frac{V_{in} - V_A}{R_2} = \frac{V_A - V_0}{\frac{1}{SC_2}} + \frac{V_A - V_0}{R_3} \quad (1)$$

For simplicity in this equation omit S ,Applying voltage divider rule

$$V_1 = \frac{\frac{1}{SC_3}}{R_3 + \left(\frac{1}{SC_3}\right)} V_A$$

Since $R_{iF} \cong \propto, I_B \cong 0A$

$$V_1 = \frac{V_A}{R_3 C_3 S + 1}$$

Or

$$V_A = (R_3 C_3 S + 1) V_1$$

Substituting value of V_A in equation (1) and solving for V_1 we get

$$V_1 = \frac{(R_3)(V_{in}) + (R_3 R_2 C_{2S})(V_0)}{(R_3 C_3 S + 1)(R_2 + R_3 + R_2 R_3 C_2 S) - R_2}$$

However $V_0 = (A_F) V_1$

Where $A_F = 1 + \left(\frac{R_F}{R_1}\right)$

Therefore

$$V_0 = \frac{(A_F)(R_3)(V_{in}) + (R_3R_2C_{2S})(V_0)}{(R_3C_3S + 1)(R_2 + R_3 + R_2R_3C_2S) - R_2}$$

Solving this equation for $\frac{v_0}{v_{in}}$ we have

$$\frac{v_0}{v_{in}} = \frac{A_F}{S^2 + \frac{(R_3C_3 + R_2C_3 + R_2C_2 - A_FR_2C_2)S}{R_2R_3C_2C_3} + \frac{1}{R_2R_3C_2C_3}}$$

For frequencies above f_H the gain of the second order low pass filter rolls off at the rate of -40 dB per decade.This means that

$$(w_H)^2 = \frac{1}{R_2R_3C_2C_3}$$

Or

$$w_H = \frac{1}{\sqrt{R_2R_3C_2C_3}}$$

$$f_H = \frac{1}{2\pi\sqrt{R_2R_3C_2C_3}}$$

For the second order low pass butterworth response voltage gain magnitude equation is

$$\left|\frac{v_0}{v_{in}}\right| = \frac{A_F}{\sqrt{1 + \left(\frac{f}{f_H}\right)^4}}$$

Where $A_F = 1 + \left(\frac{R_F}{R_1}\right)$= pass band gain of the filter

f= frequency of input signal(Hz)

$f_H = \frac{1}{2\pi\sqrt{R_2 R_3 C_2 C_3}}$ = high cutoff frequency

Q. 4 Design a second order low pass filter at a high cut off frequency of 1 kHz.

Answer:

f_H= 1 kHz

Let C_2= C_3= 0.047µF

$$R_2 = R_3 = \frac{1}{(2\pi)(10^3)(47)(10^{-10})} = 33.86k\Omega$$

R_F must be 0.586 R_1 ,let R_1=27kΩ ,therefore

$$R_F = (0.586)(27k) = 15.82k\Omega$$

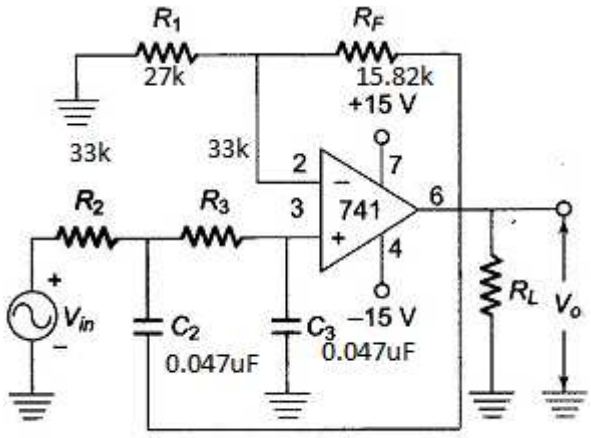

Figure 4.4:Design of second order low pass filter

Que.5 . Design second order High-pass filter with cut-off frequency 5 KHz

Ans. f_L= 5kHz

Let C_2= C_3= 0.01µF

$$R2 = R3 = \frac{1}{2\pi f_L C} = \frac{1}{2\pi(5k)(10^{-8})} = 3.183k\Omega$$

Gain component R_1 and R_F ,

Damping coefficient α = 3-A_F = 1.414

A_F = 1.586

$$A_F = 1 + \left(\frac{R_F}{R_1}\right)$$

Let R_1= 10kΩ, therefore **R_F = 5.86kΩ**

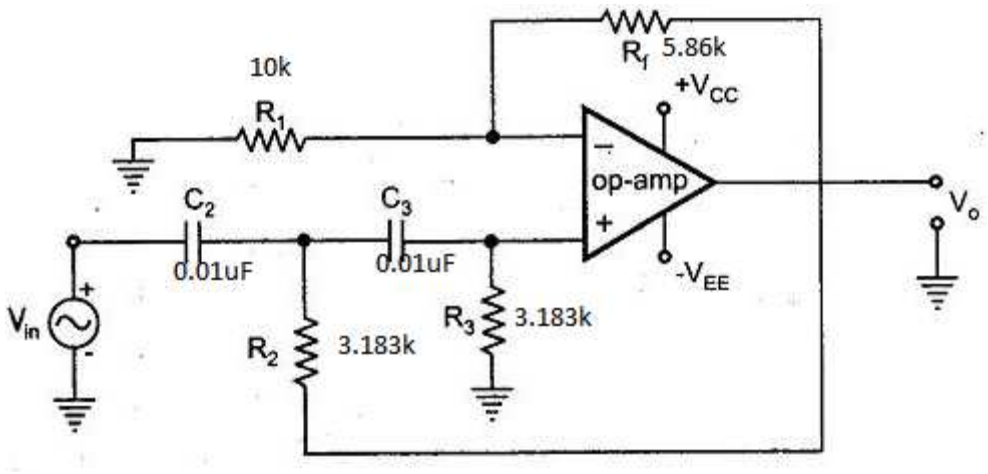

Figure 4.5: Design of second order high pass filter

Q.6 . Design a fourth order Butter worth low-pass filter whose band width is 20 KHz. Use all capacitors of 1000 nf.

Answer:

f_H=20 kHz

Let C= 1000nF,

For fourth order equation is $(S^2 + 0.765S + 1)(S^2 + 1.848S + 1)$

$$R = \frac{1}{2\pi f_H C} = \frac{1}{2\pi(20k)(1000)(10^{-9})} = 7.59\Omega$$

For gain

Stage 1: $\alpha_1 = 0.765$

$\alpha_1 = 3 - A_{F1} = 0.765$

A_{F1}= 2.235

$A_F = 1 + \left(\frac{R_F}{R_1}\right) = 2.235$

Let R_1 =10kΩ , R_F = 12.35kΩ

Stage 2: α_1 = 1.848

α_1 = 3- A_{F1}= 1.848

A_{F1}= 1.152

$A_F = 1 + \left(\frac{R_F}{R_1}\right)$ =1.152

Let R_1 =10kΩ , R_F = 1.52kΩ

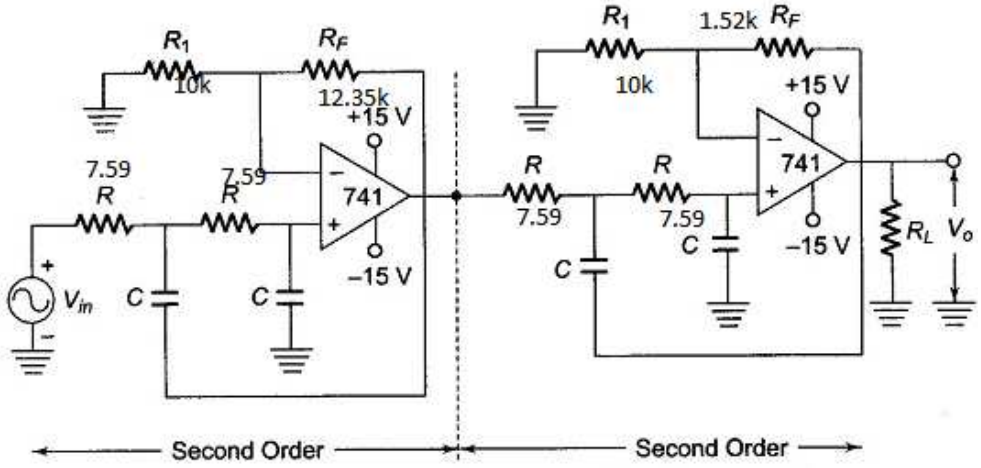

Figure 4.6: Design of fourth order Butter worth low-pass filter

Q.7 Design first order wide-band pass filter with f_L = 400Hz & f_H = 2 KHz

Answer:

f_L = 400Hz & f_H = 2 KHz

A_{F1}* A_{F2} = 4

First order low pass filter frequency component:

f_H =2 kHz.

Let C= 0.01uF

$$R = \frac{1}{2\pi f_H C} = \frac{1}{2\pi(1k)(10^{-8})} = 7.957k\Omega$$

Since passband gain is 2, R_1 and R_F must be equal .

Let R_1= R_F = 10 kΩ

First order high pass filter frequency component:

F_L = 400 Hz.

Let C= 0.01uF

$$R' = \frac{1}{2\pi f_L C} = \frac{1}{2\pi(400)(10^{-8})} = 39.788k\Omega$$

Since passband gain is 2, R_1 and R_F must be equal .

Let R_1'= R_F' = 10 kΩ

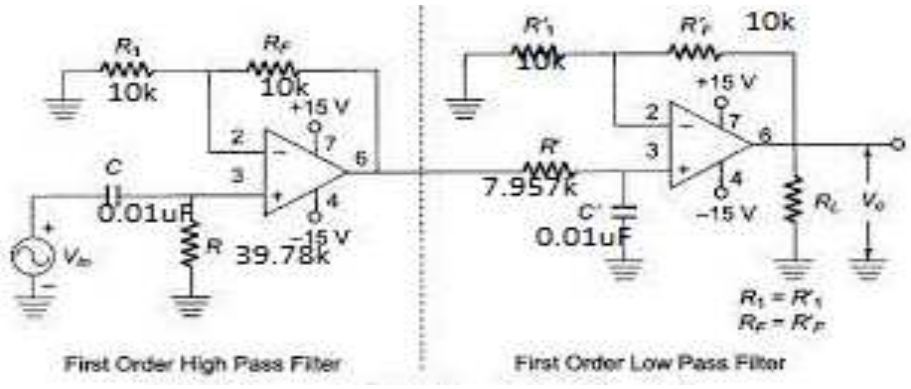

Figure 4.7: Design of first order wide-band pass filter

Q.8 *Design Second order wide-band reject filter with f_L = 4 KHz & f_H = 1 KHz.*

Answer: Second order low pass filter:

f_H = 1 KHz

Let C= 0.01uF

$$R = \frac{1}{2\pi f_H C} = \frac{1}{2\pi(1k)(10^{-8})} = 15.915k\Omega$$

C_1,C_2 =0.01uF

R_2,R_3 = 15.915kΩ

Second order High pass filter:

F_L = 4 kHz.

Let C= 0.01uF

$$R' = \frac{1}{2\pi f_L C} = \frac{1}{2\pi(4k)(10^{-8})} = 3.9788k\Omega$$

C_1',C_2 '= 0.01uF

R_2',R_3' = 3.978 kΩ **,**Gain component of second order low pass and high pass filter:

$$S^2 + 1.414S + 1$$

$$\alpha = 1.414 = 3 - A_F$$

$$A_F = 1.586$$

Let R_1= R_1'=10kΩ , R_F = R_F '= 5.86kΩ

For adder all resistance of 10 kΩ each.

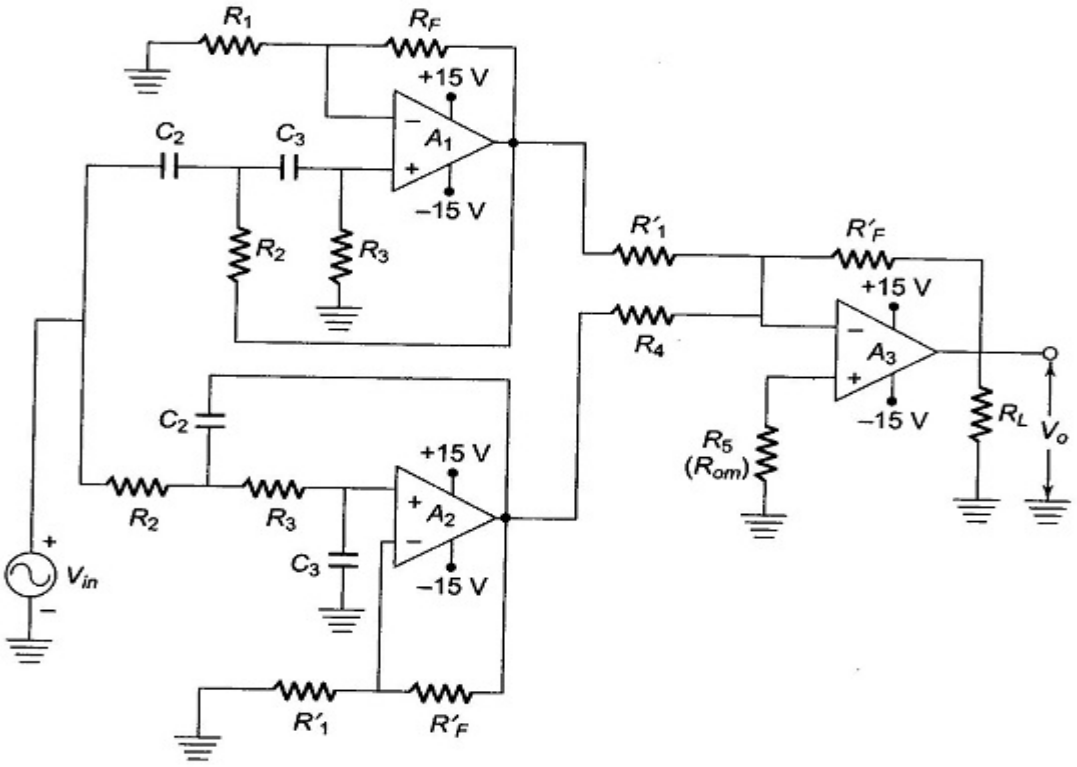

Figure 4.8: Design of Second order wide-band reject filter

Q 9.*Design narrow band pass filter shown in figure so that fc= 1 kHz,Q=3, and A_F=10.*

Answer: Let $C_1 = C_2 = C = 0.01uF$.

$$R_1 = \frac{Q}{2\pi f_c C A_F}$$

$$R_1 = \frac{3}{(2\pi)(10^3)(10^{-8})(10)} = 4.77k\Omega$$

$$R_2 = \frac{Q}{2\pi f_c (2Q^2 - A_F)}$$

$$R_2 = \frac{3}{(2\pi)(10^3)(10^{-8})[2(3)^2 - 10]} = 5.97k\Omega$$

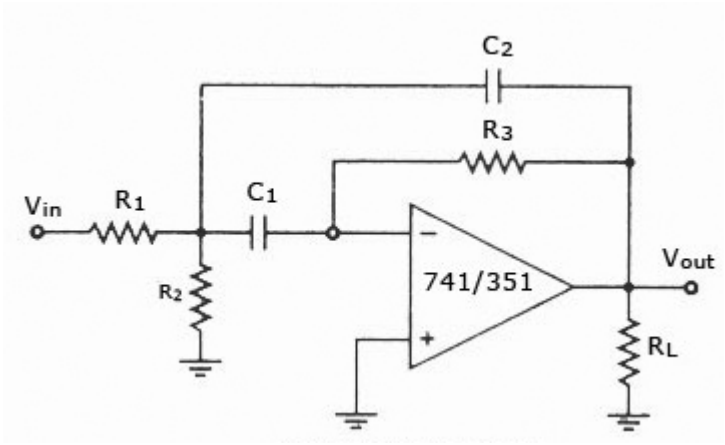

Figure 4.9: Design of narrow band pass filter

$$R_3 = \frac{Q}{\pi f_c C}$$

$$R_3 = \frac{3}{(\pi)(10^3)(10^{-8})} = 95.5k\Omega$$

Use R_1 = 4.7kΩ ,R_2 = 6.2kΩ and R_3 = 100kΩ.

Q.10 *Design a 60 Hz active notch filter.*

Answer:

Let C= 0.068uF

$$R = \frac{1}{2\pi f_N C} = \frac{1}{(2\pi)(60)(68)(10^{-9})} = 30.01k\Omega$$

For R/2 parallel two 39 kΩ resistors for the 2C component parallel two 0.068uF capacitors.

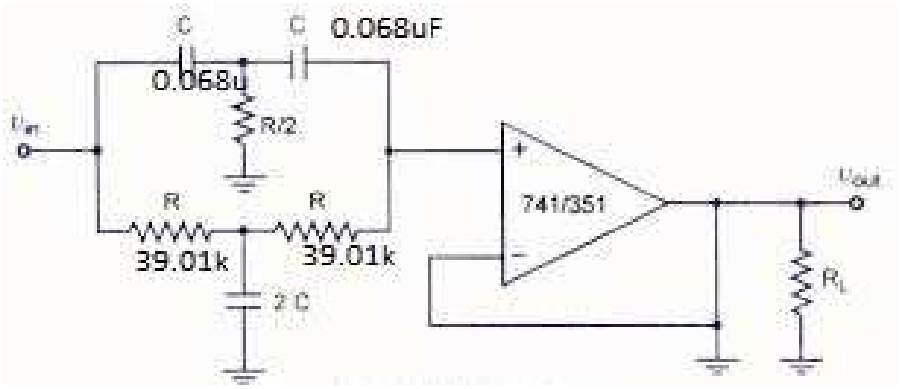

Figure 4.10: Design of active notch filter

Unit-5

Nonlinear Circuits And Waveform Generators

Q.1. *Draw the circuit of Active Clipper and explain its working with waveforms.*

Answer:

By slightly modifying the circuit, an active diode ideal clipper circuit is obtained Figure 5.1, shows an active clipper which clips the input voltage below V_R.

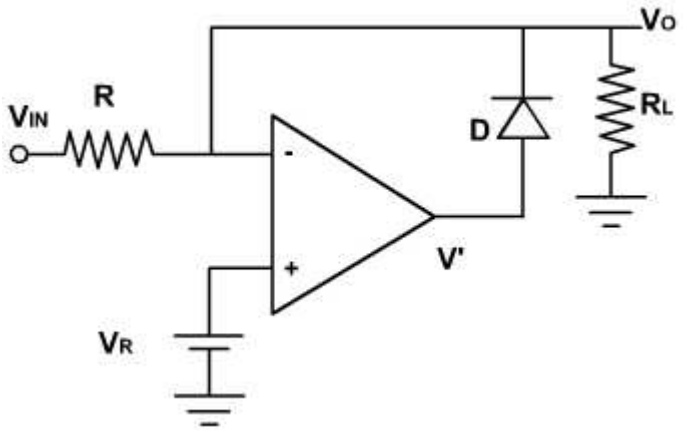

Figure 5. 1 Active Clipper using OP-AMP

When Vin $<V_R$, then v' is positive and D conducts. Under these conditions, the OPAMP works as a buffer and the output voltage equals the voltage at non-inverting terminal

Vout = V_R.

If Vin> V_R, then v' is negative and D is OFF and V_O = Vin R_L / (R_L + R) » Vi if R << R_L Thus,

output follows input for Vin > V_R and v_O is clamped to $V_R$if vin < V_R by about 60 mV. **Figure 5.2** , shows the output waveform of clipper circuit.When D is reverse biased a large differential voltage may appear between inputs and the OPAMP must be capable to withstand this voltage.

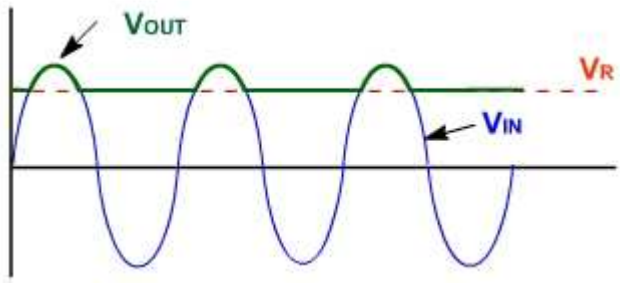

Figure 5. 2 The output waveform of Clipper circuit

Q.2. *Draw the circuit of Active Clamper and explain its working with waveforms.*

Answer:

Figure 5.3 shows an active positive clamper circuit.

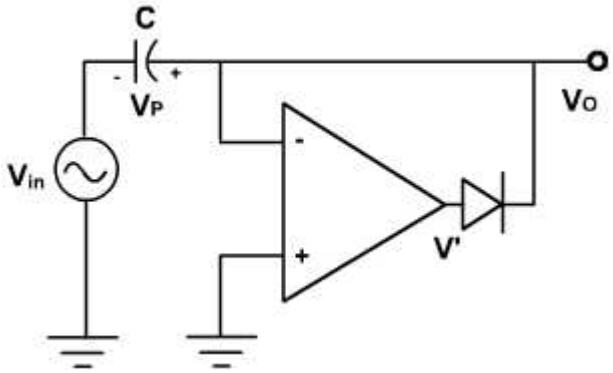

Figure 5. 3 Active Positive Clamper Circuit

The first negative half cycle produces a positive OPAMP output, which turns ON the diode. This capacitor charges to the peak of the input with the polarity shown in **Figure 5.3.** Just beyond the

negative peak the diode turns off, the feedback loop opens, and the virtual ground is lost. Therefore,

$V_{out} = V_{in} + V_P$

Since V_P is being added to a sinusoidal voltage, the final output waveform is shifted positively through V_P volts. The output wave form swing from 0 to $2V_P$ as shows in **Figure 5.4.** Again the reduction of the diode-offset voltage allows clamping with low-level inputs.

During most of the cycle, the OPAMP operates in negative saturation. Right at the negative input peak, the OPAMP produces a sharp positive going pulse that replaces any change lost by the clamping capacitor between negative input peaks.

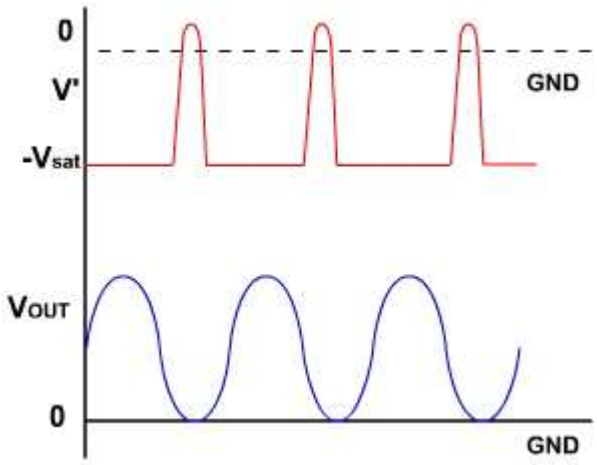

Figure 5. 4 Output Waveforms of Active Positive Clamper

Q.3. *Draw the circuit of Comparator and explain its working with related waveforms.*

Answer:

An analog comparator has two inputs one is usually a constant reference voltage V_R and other is a time varying signal V_i and one output V_O. The basic circuit of a comparator is shown in **Figure 5.5.**

When the noninverting voltage is larger than the inverting voltage the comparator produces a high output voltage ($+V_{sat}$). When the non-inverting output is less than the inverting input the output is low ($-V_{sat}$). **Figure 5.5** , also shows the output of a comparator for a sinusoidal.

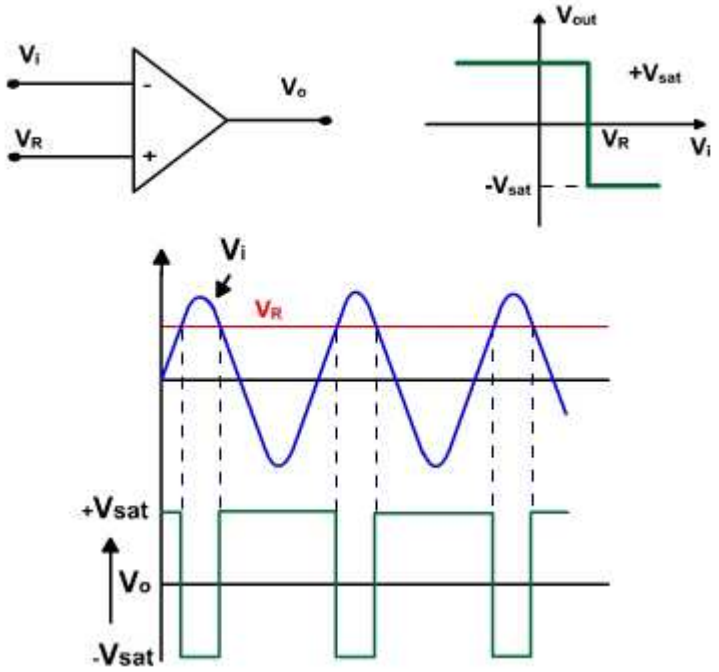

Figure 5. 5 Basic Comparator and its output waveform

$V_O = -V_{sat}$ if $V_i > V_R$

$= + V_{sat}$ if $V_i < V_R$

If $V_R = 0$, then slightest input voltage (in mV) is enough to saturate the OPAMP and the circuit acts as zero crossing detector as shown in **Figure 5.6**. If the supply voltages are ±15V, then the output compliance is from approximate – 13V to +13V. The more the open loop gain of OPAMP, the smaller the voltage required to saturate the output. If $v_d$required is very small then the characteristic is a vertical line as shown in **Figure 5.6**.

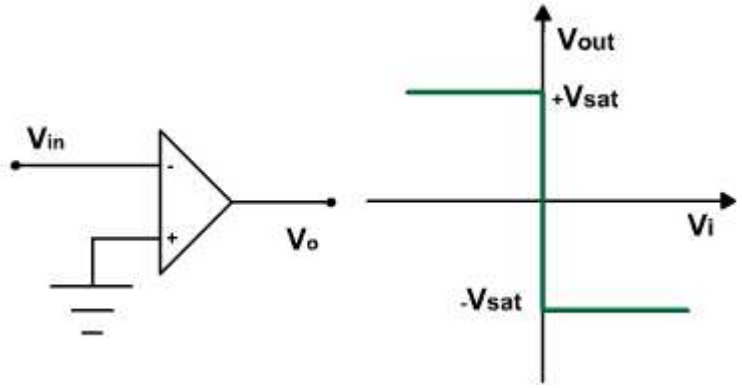

Figure 5. 6 Zero crossing detector

If we want to limit the output voltage of the comparator two voltages (one positive and other negative) then a resistor R and two zener diodes are added to clamp the output of the comparator. The circuit of such comparator is shown in **Figure 5.7**, The transfer characteristics of the circuit is also shown in **Figure 5.7**.

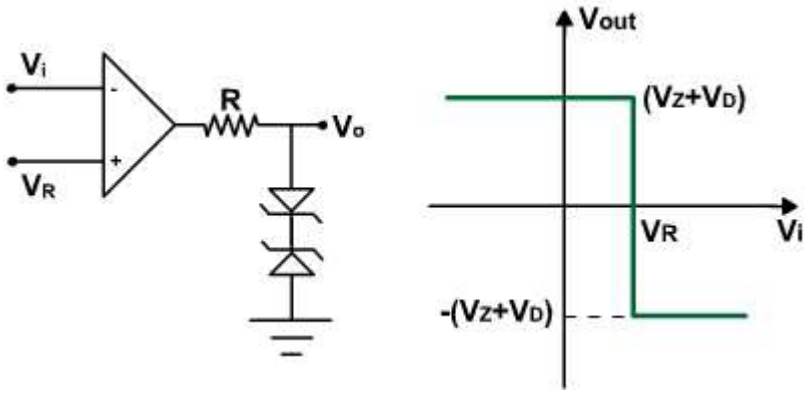

Figure 5. 7 Comparator with limiting output using zener diode

The resistance is chosen so that the zener operates in zener breakdown region. When V_R= 0 then the output changes rapidly from one state to other very rapidly every time that the input passes through zero as shown in **Figure 5.8**

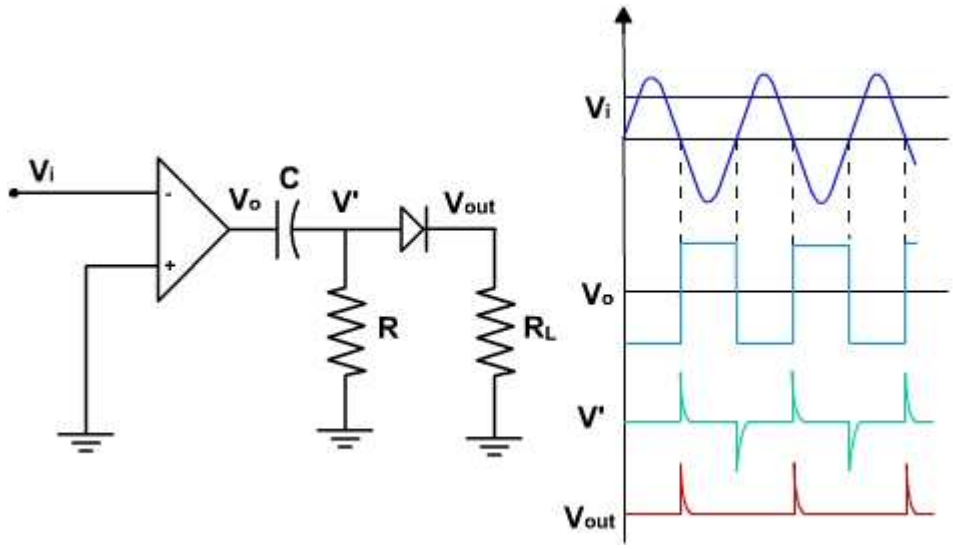

Figure 5. 8 Zero crossing detector

Such a configuration is called zero crossing detector. If we want pulses at zero crossing then a differentiator and a series diode is connected at the output. It produces single pulses at the zero crossing point in every cycle.

Q.4. *Draw the circuit of Inverting Schmitt Trigger and explain its working. Also explain how the hysteresis curve can be shifted on x-axis.*

Answer:

If the input to a comparator contains noise, the output may be erractive when v_{in} is near a trip point. For instance, with a zero crossing, the output is low when v_{in} is positive and high when v_{in} is negative. If the input contains a noise voltage with a peak of 1mV or more, then the comparator will detect the zero crossing produced by the noise **Figure 5.9** shows the output of zero crossing detection if the input contains noise.

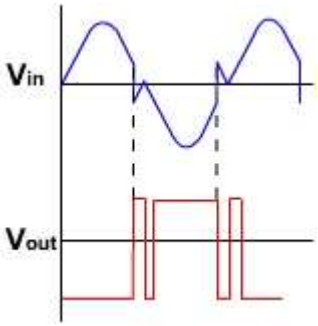

Figure 5. 9 Zero crossing detector output with noise

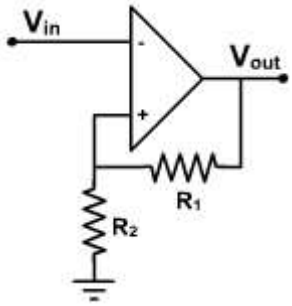

Figure 5. 10 Schmitt trigger

This can be avoided by using a Schmitt trigger, circuit which is basically a comparator with positive feedback. **Figure 5.10**, shows an inverting Schmitt trigger circuit using OPAMP.

Because of the voltage divider circuit, there is a positive feedback voltage. When OPAMP is positively saturated, a positive voltage is feedback to the non-inverting input, this positive voltage holds the output in high stage. ($V_{in}<V_f$). When the output voltage is negatively saturated, a negative voltage feedback to the inverting input, holding the output in low state.

When the output is $+V_{sat}$ then reference voltage V_{ref} is given by

$$V_{ref} = \left(\frac{R_2}{R_1 + R_2}\right) \times (+V_{sat}) = +\beta V_{sat}$$

If V_{in} is less than V_{ref} output will remain $+V_{sat}$.

When input V_{in} exceeds $V_{ref} = +V_{sat}$ the output switches from $+V_{sat}$ to $-V_{sat}$. Then the reference voltage is given by

$$V_{ref} = \left(\frac{R_2}{R_1 + R_2}\right) \times (-V_{sat}) = -\beta V_{sat}$$

The output will remain $-V_{sat}$ as long as $v_{in}>V_{ref}$.

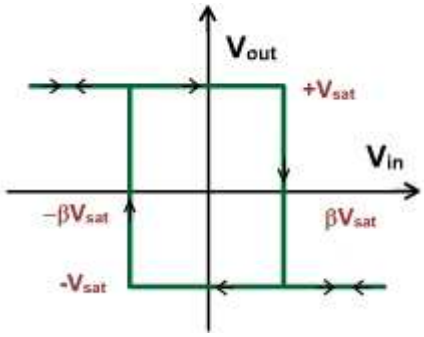

Figure 5. 11 Transfer Characteristics of Schmitt trigger

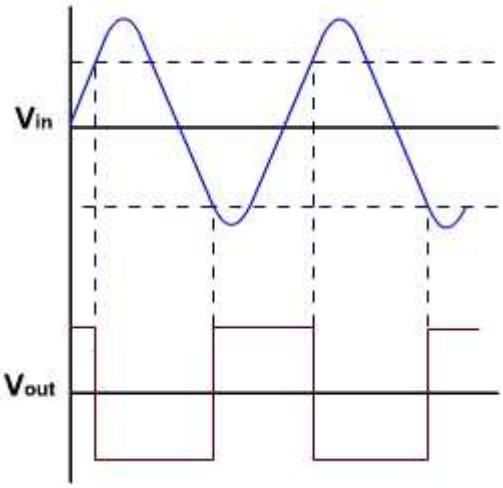

Figure 5. 12 Output Waveforms of Schmitt trigger

If $V_{in}<V_{ref}$ i.e. V_{in} becomes more negative than $-V_{sat}$ then again output switches to $+V_{sat}$ and so on. The transfer characteristic of Schmitt trigger circuit is shown in **Figure 5.11**. The output is also shown in **Figure 5.12** for a sinusoidal wave. If the input is different than sine even then the output will be determined in a same way.

Positive feedback has an unusual effect on the circuit. It forces the reference voltage to have the same polarity as the output voltage, The reference. voltage is positive when the output voltage is high (+Vsat) and negative when the output is low (–Vsat).

In a Schmitt trigger, the voltages at which the output switches from +vsat to –vsat or vice versa are called upper trigger point (UTP) and lower trigger point (LTP). the difference between the two trip points is called hysteresis.

$$UTP = \left(\frac{R_2}{R_1 + R_2}\right) \times (+V_{sat}) = +\beta V_{sat}$$

$$LTP = \left(\frac{R_2}{R_1 + R_2}\right) \times (-V_{sat}) = -\beta V_{sat}$$

$$V_{hys} = UTP - LTP$$

$$V_{hys} = \left(\frac{R_2}{R_1 + R_2}\right) \times (+V_{sat}) - \left(\frac{R_2}{R_1 + R_2}\right) \times (-V_{sat})$$

$$V_{hys} = 2\left(\frac{R_2}{R_1 + R_2}\right) V_{sat}$$

$$V_{hys} = 2\beta V_{sat}$$

The hysteresis loop can be shifted to either side of zero point by connecting a voltage source as shown in **Figure 5.13**.

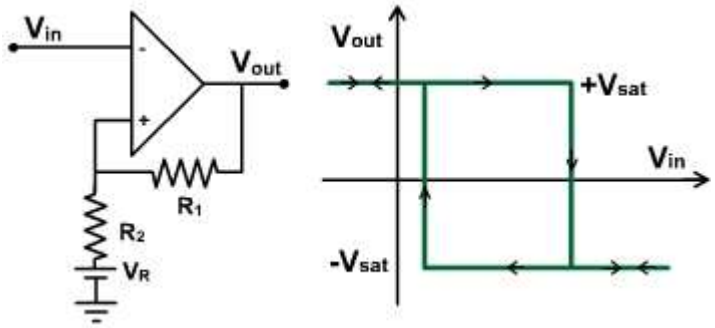

Figure 5. 13 Schmitt trigger with shifted Hysterisis curve

When V_O= +Vsat , the reference. Voltage (UTP) is given by

$$UTP = \left(\frac{R_2(+V_{sat} - V_R)}{R_1 + R_2}\right) + V_R$$

$$UTP = \beta V_{sat} + \left(\frac{R_1}{R_1 + R_2} V_R\right)$$

When V_O= -Vsat , the reference. Voltage (UTP) is given by

$$LTP = \left(\frac{R_2(-V_{sat} - V_R)}{R_1 + R_2}\right) + V_R$$

$$LTP = -\beta V_{sat} + \left(\frac{R_1}{R_1 + R_2} V_R\right)$$

If V_R is positive the loop is shifted to right side; if V_R is negative, the loop is shifted to left side. The hysteresis voltage V_{hys} remains the same.

Q.5. *Draw the circuit of Non-inverting Schmitt Trigger and explain its working.*

Answer:

In this circuit the feedback is given at non-inverting terminal. The inverting terminal is grounded and the input voltage is connected to non-inverting input. **Figure 5.14**, shows an non-inverting schmitt trigger circuit.

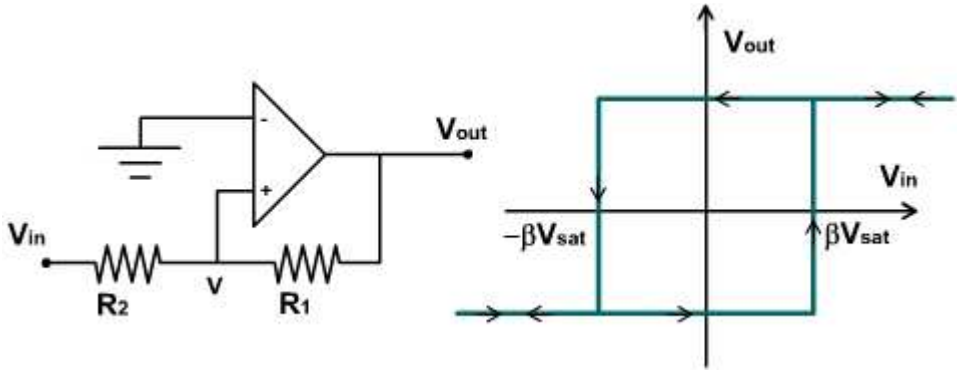

Figure 5. 14 Non-Inverting Schmitt trigger & its Traansfer Characteristics

To analyze the circuit behaviour, let us assume the output is negatively saturated. Then the feedback voltage is also negative (-Vsat). Then the feedback voltage is also negative. This feedback voltage will hold the output in negative saturation until the input voltage becomes positive enough to make voltage positive.

$$V_{NI} = \left(\frac{R_2(-V_{sat} - V_{in})}{R_1 + R_2}\right) + V_{in}$$

$$V_{NI} = -V_{sat}\frac{R_2}{R_1 + R_2} + V_{in}\frac{R_1}{R_1 + R_2}$$

$$V_{NI} = \frac{R_1}{R_1 + R_2}(-R_2V_{sat} + R_1V_{in})$$

$$V_{NI} = \frac{R_1}{R_1 + R_2}\left(-\frac{R_2}{R_1}V_{sat} + V_{in}\right)$$

When Vin becomes positive and its magnitude is greater than (R2 / R1) Vsat, then the output switches to +Vsat. Therefore, the UTP at which the output switches to +Vsat, is given by

$$UTP = \frac{R_2}{R_1}V_{sat}$$

Simillarly, when the output is in positive saturation, feedback voltage is positive. To switch output states, the input voltage has to become negative enough to make. When this input transition takes place, the output changes to the negative state from positive saturation to negative saturation voltage.

$$V_{NI} = \left(\frac{R_2(+V_{sat} - V_{in})}{R_1 + R_2}\right) + V_{in}$$

$$V_{NI} = +V_{sat}\frac{R_2}{R_1 + R_2} + V_{in}\frac{R_1}{R_1 + R_2}$$

$$V_{NI} = \frac{R_1}{R_1 + R_2}(R_2V_{sat} + R_1V_{in})$$

$$V_{NI} = \frac{R_1}{R_1 + R_2}\left(\frac{R_2}{R_1}V_{sat} + V_{in}\right)$$

When Vin becomes negative and its magnitude is greater than R2 / R1 Vsat, then the output switches to -Vsat. Therefore,

$$LTP = -\frac{R_2}{R_1}V_{sat}$$

The difference of UTP and LTP gives the hysteresis of the Schmitt trigger.

$$V_{hys} = UTP - LTP$$

$$V_{hys} = 2\left(\frac{R_2}{R_1}\right)V_{sat}$$

$$V_{hys} = 2\beta V_{sat}$$

In non inverting Schmitt trigger circuit, the β is defined as

$$\beta = \frac{R_2}{R_1}$$

Q.6. *Draw the circuit of Astablemultivibrator using OP-AMP and explain its working with neat waveforms and derive necessary expressions.*

Answer:

The Schmitt trigger circuit with negative feedback loop of RC can be used as Astable multivibrator as shown in **figure 5.15**. The circuit produces a square wave at the output whose frequency depends on the timing RC combination used.

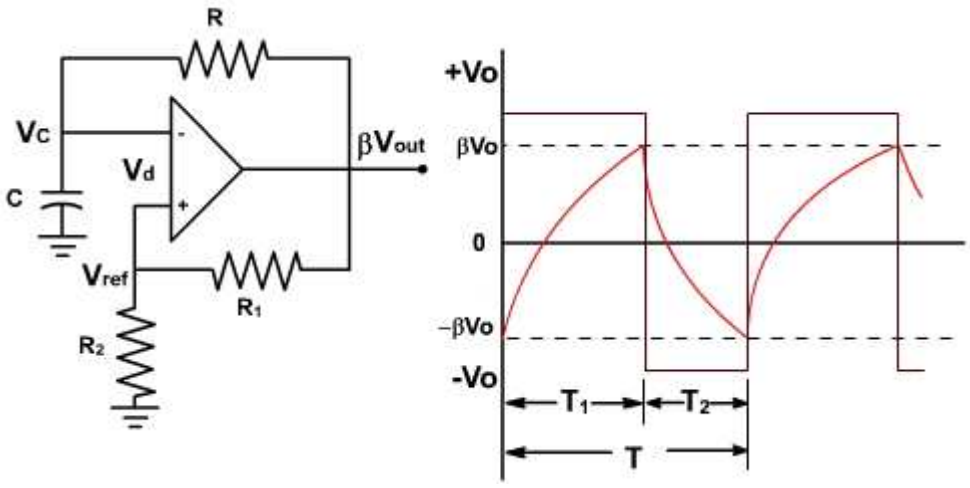

Figure 5. 15 Astable multivibrator Circuit and output waveforms

In this circuit a fraction $R_2/ (R_1 + R_2) = \beta$ of the output is feedback to the non-inverting input terminal. The operation of the circuit can be explained as follows:

Assume that the output voltage is $+V_{sat}$. The capacitor will charge exponentially toward $+V_{sat}$. The feedback voltage is $+\beta V_{sat}$. When capacitor voltage exceeds $+\beta V_{sat}$ the output switches from $+V_{sat}$ to $-V_{sat}$. The feedback voltage becomes $-V_{sat}$ and the output will remain $-V_{sat}$. Now the capacitor charges in the reverse direction. When capacitor voltage decreases below $-\beta V_{sat}$ (more negative than $-\beta V_{sat}$) the output again switches to $+V_{sat}$.This process continues and it produces a square wave. Under steady state conditions, the output voltage and capacitor voltage are shown in **Figure 5.15**. The frequency of the output can be obtained as follows:

The capacitor charges from $-\beta V_{sat}$ to $+\beta V_{sat}$ during time period T/2. The capacitor charging voltage expression is given by

$$V_c(t) = V_f + (V_i - V_f)e^{-t/RC}$$

$V_c(t)$ is the voltage across the capacitor at time t.

V_f is final voltage to which capacitor is expected to charge

V_i is the initial voltage across the capacitor from which it starts charging or discharging

At $t = T/2$, $V_c(t) = +\beta V_{sat}$ $V_f = +V_{sat}$ $V_i = -\beta V_{sat}$

$$+\beta V_{sat} = V_{sat} + (-\beta V_{sat} - V_{sat})e^{-T/2RC}$$

$$\beta V_{sat} = V_{sat} - (1+\beta)V_{sat}e^{-T/2RC}$$

$$(1+\beta)V_{sat}e^{-T/2RC} = (1-\beta)V_{sat}$$

$$e^{-T/2RC} = \frac{(1-\beta)}{(1+\beta)}$$

$$\frac{T}{2RC} = \frac{(1+\beta)}{(1-\beta)}$$

$$T = 2RC\ln\left(\frac{(1+\beta)}{(1-\beta)}\right)$$

The frequency of square wave is given by

$$f = \frac{1}{T} = \frac{1}{2RC\ln\left(\frac{(1+\beta)}{(1-\beta)}\right)}$$

This square wave generator is useful in the frequency range of 10Hz to 10KHz. At higher frequencies, the slew rate of the OPAMP limits the slope of the output square wave.

Q.7. *Draw the circuit of RC phase shift oscillator and derive the expression for frequency of oscillation and condition on gain for sustained oscillations.*

Answer:

The circuit consists of inverting amplifier as amplifier block and three R-C network as feedback network. The amplifier produces 180 phase shift and remaining 180 required for 360 phase shift is provided by R-C network 60 each.

The frequency at which the phase shift is 360 is decided by R-C network. To determine frequency of operation solving R-C network using Laplace transform. The R-C network in Laplace domain is as shown in **figure 5.16**.

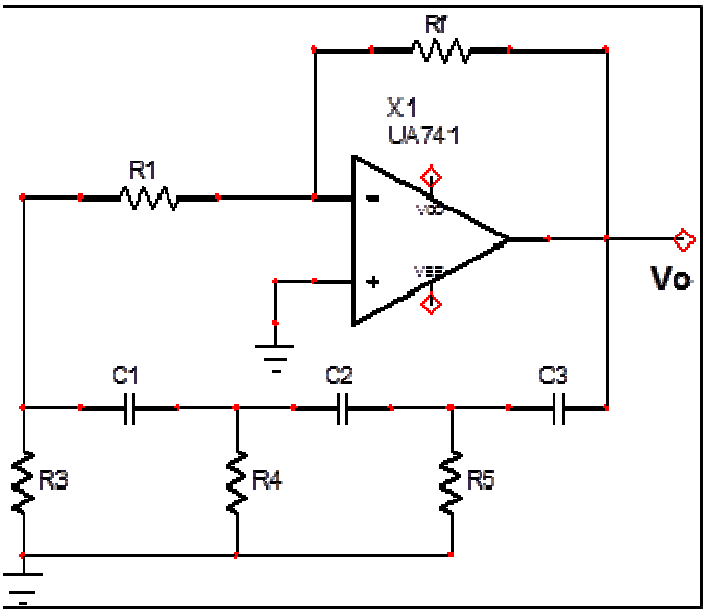

Figure 5. 16 R-C phase shift oscillator

To derive the expression of frequency solving the feedback network first as shown in **figure 5.17**.

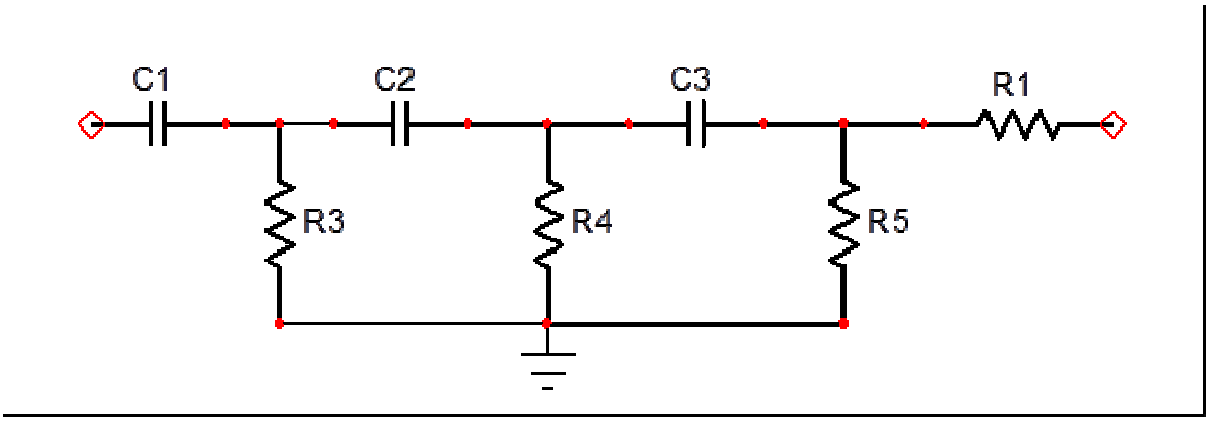

Figure 5. 17 Feedback network of R-C phase shift oscillator

Applying KCL at node $V_1(s)$,

$$I_1(s) = I_2(s) + I_3(s)$$

$$\frac{V_o(s) - V_1(s)}{1/sC} = \frac{V_1(s)}{R} + \frac{V_1(s) - V_2(s)}{1/sC}$$

$$\frac{V_1(s)}{R} + \frac{2V_1(s)}{1/sC} = \frac{V_o(s) + V_2(s)}{1/sC}$$

$$V_1(s)\left(\frac{1}{R} + 2sC\right) = (V_o(s) + V_2(s)).sC$$

$$V_1(s)\left(\frac{1 + 2RsC}{R}\right) = (V_o(s) + V_2(s)).sC$$

$$V_1(s) = \frac{(V_o(s) + V_2(s)).RsC}{1 + 2RsC} \quad \text{----------} \quad (1)$$

Applying KCL at node $V_2(s)$

$$I_3(s) = I_4(s) + I_5(s)$$

$$\frac{V_1(s) - V_2(s)}{1/sC} = \frac{V_2(s)}{R} + \frac{V_2(s) - V_f(s)}{1/sC}$$

$$\frac{V_1(s)}{1/sC} = \frac{V_2(s)}{R} + \frac{2V_2(s)}{1/sC} - \frac{V_f(s)}{1/sC}$$

$$V_1(s).sC = V_2(s)\left(\frac{1}{R} + sC\right) - V_f(s).sC$$

$$V_1(s) = V_2(s)\left(\frac{1+2RsC}{RsC}\right) - V_f(s) \text{ - - - - - - - - - - - - - - } \quad (2)$$

If R_1 is very greater than R then current drawn by R_1 is negligibly small.

$$I_7(s) = 0$$

$$I_5(s) = I_6(s)$$

Applying voltage divider rule to find $V_f(s)$

$$V_f(s) = \left(\frac{R}{R + \frac{1}{sC}}\right).V_2(s)$$

$$V_2(s) = \left(\frac{1+RsC}{RsC}\right).V_f(s)$$

Substitute V_2 in equation 1 & 2

$$V_1(s) = \frac{RsC\ .}{1+2RsC}\left(V_o(s) + \left(\frac{1+RsC}{RsC}\right).V_f(s)\right)$$

$$V_1(s) = \left(\frac{RsC}{1+2RsC}\right)V_o(s) + \left(\frac{1+RsC}{1+2RsC}\right).V_f(s) \text{ - - - - - - - }$$

and

$$V_1(s) = \left(\frac{1+2RsC}{RsC}\right)\left(\frac{1+RsC}{RsC}\right)V_f(s) - V_f(s) \quad \text{(4)}$$

Equating equations 3 & 4

$$\left(\frac{RsC}{1+2RsC}\right)V_o(s) + \left(\frac{1+RsC}{1+2RsC}\right).V_f(s) = \left(\frac{1+2RsC}{RsC}\right)\left(\frac{1+RsC}{RsC}\right)V_f(s) - V_f(s)$$

$$\left(\frac{RsC}{1+2RsC}\right)V_o(s) = \left(\frac{1+2RsC}{RsC}\right)\left(\frac{1+RsC}{RsC}\right)V_f(s) - V_f(s) - \left(\frac{1+RsC}{1+2RsC}\right).V_f(s)$$

$$\left(\frac{RsC}{1+2RsC}\right)V_o(s) = V_f(s)\left[\frac{(1+2RsC)(1+RsC)}{(RsC)^2} - 1 - \left(\frac{1+RsC}{1+2RsC}\right)\right]$$

$$\left(\frac{RsC}{1+2RsC}\right)V_o(s) = V_f(s)\left[\frac{(1+2RsC)^2(1+RsC) - (RsC)^2(1+2RsC) - (RsC)^2(1+RsC)}{(RsC)^2(1+2RsC)}\right]$$

$$\left(\frac{RsC}{1+2RsC}\right)V_o(s) = V_f(s)\left[\frac{(1+4RsC+4R^2C^2s^2)(1+RsC) - 3R^3C^3s^3 - 2R^2C^2s^2}{R^2C^2s^2(1+2RsC)}\right]$$

$$\left(\frac{RsC}{1+2RsC}\right)V_o(s) = V_f(s)\left[\frac{1+4RsC+R^2C^2s^2+RsC+4R^2C^2s^2+4R^3C^3s^3-3R^3C^3s^3-2R^2C^2s^2}{R^2C^2s^2(1+2RsC)}\right]$$

$$\left(\frac{RsC}{1+2RsC}\right)V_o(s) = V_f(s)\left[\frac{1+5RsC+6R^2C^2s^2+R^3C^3s^3}{R^2C^2s^2(1+2RsC)}\right]$$

$$\frac{V_f(s)}{V_o(s)} = \left[\frac{R^2C^2s^2(1+2RsC)}{1+5RsC+6R^2C^2s^2+R^3C^3s^3}\right]\left(\frac{RsC}{1+2RsC}\right)$$

$$\beta = \frac{R^3C^3s^3}{1+5RsC+6R^2C^2s^2+R^3C^3s^3}$$

The amplifier used is inverting amplifier with feedback, its gain is given by,

$$A_F = -\frac{R_F}{R_1} \qquad A_F \times \beta = 1$$

For sustained oscillations

$$-\left(\frac{R_F}{R_1}\right)\left(\frac{R^3C^3s^3}{1+5RsC+6R^2C^2s^2+R^3C^3s^3}\right) = 1$$

$$-\left(\frac{R_F}{R_1}\right)R^3C^3s^3 = 1+5RsC+6R^2C^2s^2+R^3C^3s^3$$

Substitue s=jω

$$-\left(\frac{R_F}{R_1}\right)\left(-jR^3C^3\omega^3\right) = 1+5jRC\omega-6R^2C^2\omega^2-jR^3C^3\omega^3$$

Equating real parts we get

$$0 = 1-6R^2C^2\omega^2$$

$$\omega^2 = \frac{1}{6R^2C^2} \qquad \omega = \frac{1}{RC\sqrt{6}} \qquad \boxed{f = \frac{1}{2\pi RC\sqrt{6}}}$$

Equating imaginary parts we get,

$$\left(\frac{R_F}{R_1}\right)\left(R^3C^3\omega^3\right) = 5RC\,\omega - R^3C^3\omega^3$$

$$\left(\frac{R_F}{R_1}\right) = \frac{5}{R^2C^2\omega^2} - 1$$

Substitute ω in above expression

$$\left(\frac{R_F}{R_1}\right) = \frac{5}{R^2C^2\left(\frac{1}{6R^2C^2}\right)} - 1$$

$$\left(\frac{R_F}{R_1}\right) = 5(6) - 1 = 29 \qquad \boxed{R_F = 29\,R_1}$$

Q.8. *For the Schmitt trigger circuit shown in* ***figure 5.18*** *determine UTP, LTP, hysteresis voltage and center of hysteresis if* R_1*=10KΩ and* R_2*=5KΩ, use* $\pm V_{sat} = \pm 15$ *V and* $V_R = +5V$.

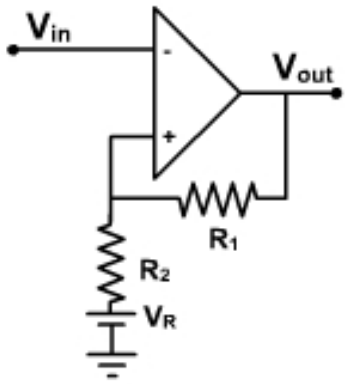

Figure 5. 18 Circuit for Q.8

Solution:

The feedback factor β is given by,

$$\beta = \frac{R_2}{R_1 + R_2}$$

$$\beta = \frac{\mathbf{5K\Omega}}{\mathbf{10K\Omega + 5K\Omega}} = 0.3333$$

The upper threshold voltage UTP is given by,

$$UTP = \beta V_{sat} + \left(\frac{R_1}{R_1 + R_2} V_R\right)$$

$$UTP = 0.3333 \times 15 + \left(\frac{\mathbf{10K\Omega}}{\mathbf{10K\Omega + 5K\Omega}} \times 5\right)$$

$$UTP = 5.6667\,V$$

The lower threshold voltage LTP is given by,

$$LTP = -\beta V_{sat} + \left(\frac{R_1}{R_1 + R_2} V_R\right)$$

$$LTP = -\beta V_{sat} + \left(\frac{R_1}{R_1 + R_2} V_R\right)$$

$$LTP = -0.3333 \times 15 + \left(\frac{\mathbf{10K\Omega}}{\mathbf{10K\Omega + 5K\Omega}} \times 5\right)$$

$$LTP = -1.6667\,V$$

The hysteresis voltage is given by

$$V_{hys} = UTP - LTP$$

$$V_{hys} = 5.6667 - (-1.6667)$$

$$V_{hys} = 7.3334\,V$$

The center of hysteresis is given by,

$$V_C = \frac{UTP + LTP}{2}$$

$$V_C = \frac{5.6667 - 1.6667}{2}$$

$$V_C = 4\,V$$

The hysteresis curve is as shown in **figure 5.19**,

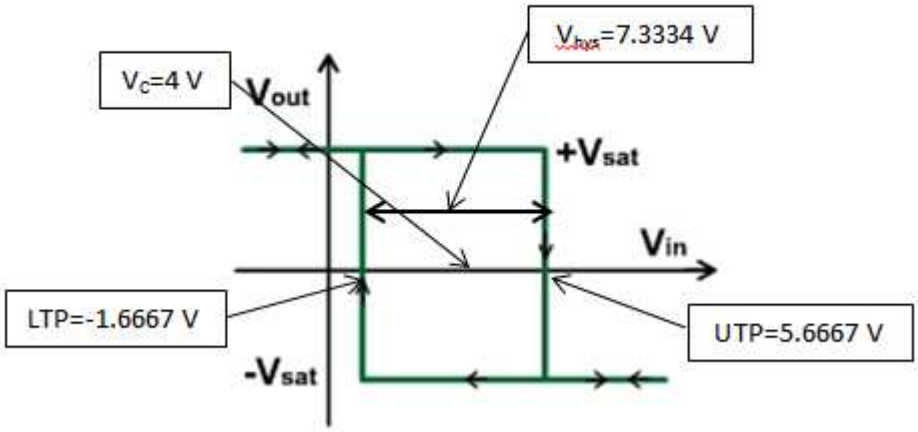

Figure 5. 19 The hysteresis curve of Schmitt Trigger

Q.9. *Design the circuit of square wave generator using OP-AMP for frequency of operation 1KHz.*

Solution:

The square wave generator using op-amp is nothing but astable multivibrator, so using the equations of astable multivibrator for design for the circuit as shown in **figure 5.20**.

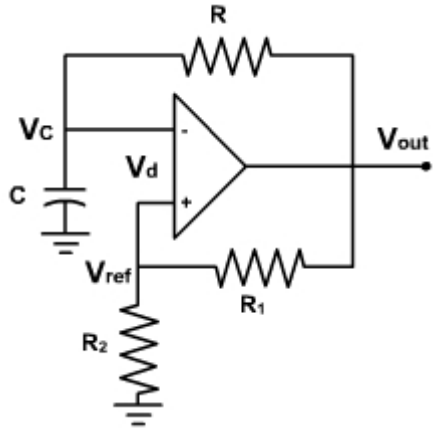

Figure 5. 20 Astable Multivibrator

The frequency of operation is 1 KHz, therefore time period is T=1ms.

The equation for time period is given by,

$$T = 2RC \ln\left(\frac{(1+\beta)}{(1-\beta)}\right)$$

where the feedback factor β is given by,

$$\beta = \frac{R_2}{R_1 + R_2}$$

For design simplification let R_1=R_2=10KΩ, therefore the feedback factor β becomes,

$$\beta = 0.5$$

The equation for time period is modified as given by,

$$T = 2RC \ln\left(\frac{(1+0.5)}{(1-0.5)}\right)$$

$$T = 2RC \ln(3)$$

$$T = 2.197RC$$

We have time period T=1ms.

Assume standard value of capacitor less than 1µF.

Let C=0.1µF

Substituting T and C in equation of time period we get,

R=4.551KΩ

The designed values of components are

R_1=R_2=10KΩ

C=0.1 µF

R=4.551KΩ

Q.10. *Draw the circuit of Wien Bridge oscillator and derive the expression for frequency of oscillation and condition on gain for sustained oscillations.*

Answer:

Wien bridge oscillator is the most commonly used audio frequency oscillator due to its inherent simplicity and stability. **Figure 5.21** shows the wien bridge oscillator using op-amp. Since the op-amp is connected to operate in non-inverting mode, it produces no phase-shift at the output. The wien bridge circuit is connected between the input and output terminals of the amplifier. The bridge consists of a series RC network shown as $Z_s(s)$ forming one arm of the bridge circuit, a parallel RC network shown as $Z_p(s)$ forming the second arm, input resistance R_1, and feedback resistance R_f reforming the third and fourth arms of the bridge circuit respectively.

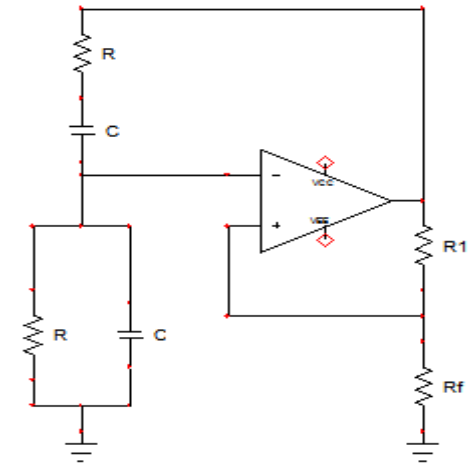

Figure 5. 21 Wien Bridge Oscillator

The feedback circuit of the wien bridge oscillator is shown in **figure 5.22**.

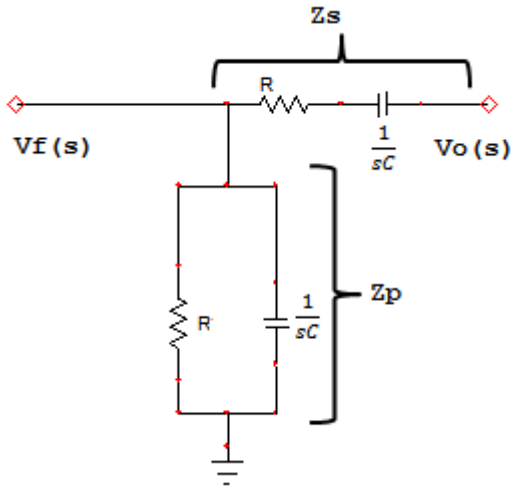

Figure 5. 22 The feedback circuit of the Wien BridgeOscillator

It is known that the total phase-shift around the circuit must be 0° for oscillations to occur. It is achieved when the bridge is balanced, i.e. at resonance. Thus the frequency of oscillation is the resonant frequency of the balanced wien bridge.

The feedback voltage $V_f(s)$ is given by voltage divider rule,

$$V_f(s) = \frac{Z_p}{Z_s + Z_p} V_o(s)$$

where the impedance of series and parallel arm is given by

$$Z_p(s) = \frac{R \times \frac{1}{sC}}{R + \frac{1}{sC}} = \frac{R}{RCs + 1}$$

$$Z_s(s) = R + \frac{1}{sC} = \frac{RCs + 1}{sC}$$

Therefore the feedback factor β is given by

$$\beta = \frac{V_f(s)}{V_o(s)} = \frac{Z_p(s)}{Z_s(s) + Z_p(s)} = \frac{RCs}{(RCs + 1)^2 + RCs}$$

$$\beta = \frac{RCs}{R^2C^2s^2 + 3RCs + 1}$$

The voltage gain of the non-inverting amplifier is given by,

$$A_f = \left(1 + \frac{R_f}{R_1}\right)$$

For satisfying Barkhausen's criteria

$$A_f \times \beta = 1$$

$$\left(1 + \frac{R_f}{R_1}\right) \times \frac{RCs}{R^2C^2s^2 + 3RCs + 1} = 1$$

Substitute $s = j\omega$

$$\left(1 + \frac{R_f}{R_1}\right) \times j\omega RC \ = -\omega^2R^2C^2 + 3j\omega RC + 1$$

Equating real parts, we get

$$\omega^2R^2C^2 = 1$$

Therefore

$$\boldsymbol{f = \frac{1}{2\pi RC}}$$

Equating imaginary parts, we get

$$\left(1 + \frac{R_f}{R_1}\right) \times j\omega RC \ = 3j\omega RC$$

which gives

$\boldsymbol{A_f = \left(1 + \frac{R_f}{R_1}\right) = 3}$ or $\boldsymbol{R_f = 2R_1}$

Unit 6

Monolithic timer IC555 and D-A AND A-D CONVERTERS

Q.1 *Explain in detail explanation of binary weighted resistor type D/A converter*

Answer: Figure shows binary weighted resistor type D/A converter using opamp as a summing amplifier.It employes binary weighted resistor to generate the terms $bi2^{-i}$ where i= 1,2,3…..n.The circuit also uses n electronic switches controlled by the binary input word b_1, b_2,…..b_n and a reference voltage V_R.The switches are of single pole double throw type.If binary input to a switch is 1,then switch connects the resistor voltage - V_R. When the input to the switch is 0,it connects the resistor to ground.

Considering an ideal opamp A, output current I_0 is given by

$$I_0 = I_1 + I_2 + \cdots + I_n$$

$$I_0 = \frac{V_R}{2^1 R} b_1 + \frac{V_R}{2^2 R} b_2 + \cdots + \frac{V_R}{2^n R} b_n$$

$$I_0 = \frac{V_R}{R} [b_1 2^{-1} + b_2 2^{-2} + \cdots + b_n 2^{-n}$$

Thus the output voltage

$$V_0 = I_0 R_f = \frac{V_R}{R} [b_1 2^{-1} + b_2 2^{-2} + \cdots + b_n 2^{-n}$$

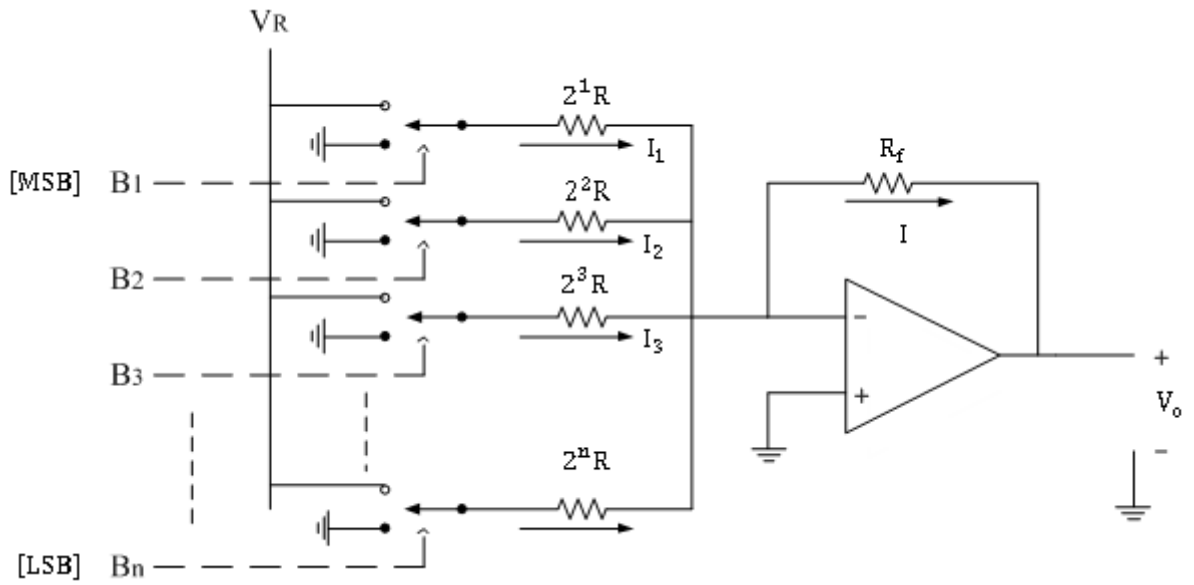

Figure 6.1:Circuit diagram of n bit weighted resistor D/A converter

The n bit D/A conveter circuit uses negative reference voltage , thus producing positive staircase voltage.The analog output voltage waveform for 3 bit weighted resistor D/A converter is shown in transfer charecteristics.

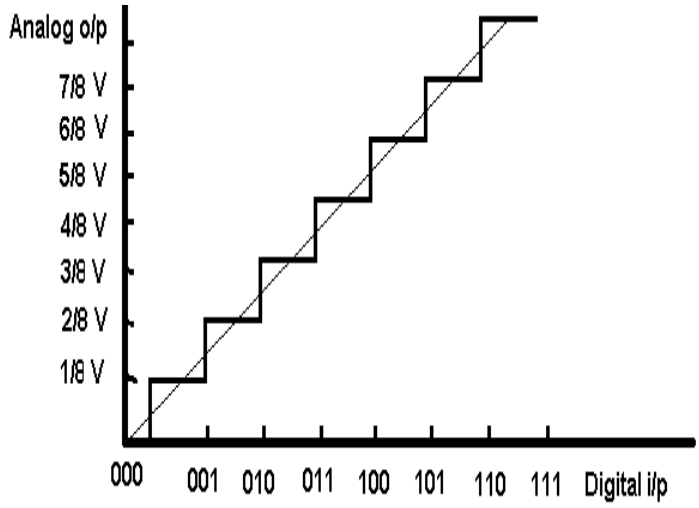

Figure 6.2: Transfer charectristics of n bit weighted resistor D/A converter

Q.2 *A 4 bit R-2R ladder type /A converter having resistor values of R=10 KΩ ,uses V_R of 10v. Find a.The resolution of D/A converter , b.I_0 for a digital input of 1101.*

Answer: Given n = 4, R=10 kΩ, V_R = 10v.

a. Resolution of 1 LSB $= \frac{1}{2^n} \times \frac{V_R}{R} = \frac{1}{2^4} \times \frac{10}{10\times10^3} = \frac{1}{16} \times 1\text{mA} = 62.5\text{uA}$

b. I_0 for a digital input of 1101

$$I_0 = 62.5\text{uA} \times 13 = 0.8125\text{mA}$$

Q.3 *Discuss in detail R-2R ladder D/A converter*

Answer:

R-2R ladder D/A converter: In R-2R ladder D/A conveter resistor of only two values i.e. R and 2R are used.The principle of operation of ladder type network for 4 bit D/A conversion is shown in figure.

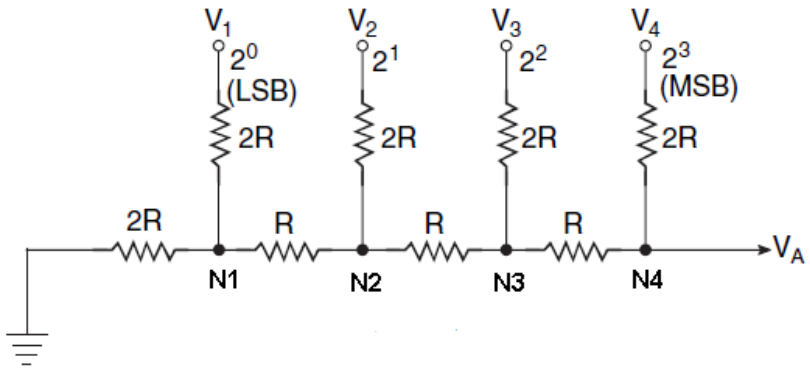

Figure 6.3: 4 bit R-2R ladder D/A converter

In ladder circuit the output voltage is also weighted sum of the corresponding digital input. Let take an example to understand how it works? As we can see the above network is a 4-bit ladder network so we take an example to convert analog signal correspond of **1000** digital bit. For **1000** bit we can see only MSB got 1 and rest all bits got 0. See the bellow picture to understand how it work if it got **1000**.

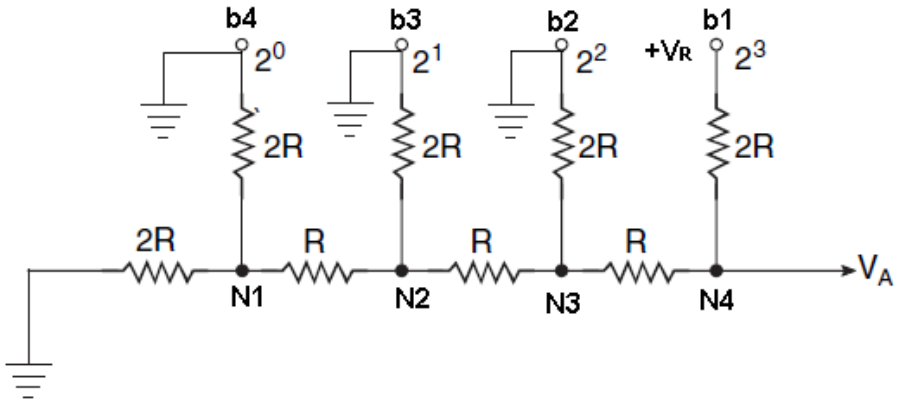

Figure 6.4:Equivant circuit for binary input 1000

Now see at node1 (N1) resistor 2R connecting in b4 parallel with resistor 2R. And those 2R parallel 2R resistors make equivalent register of R shown in bellow diagram.

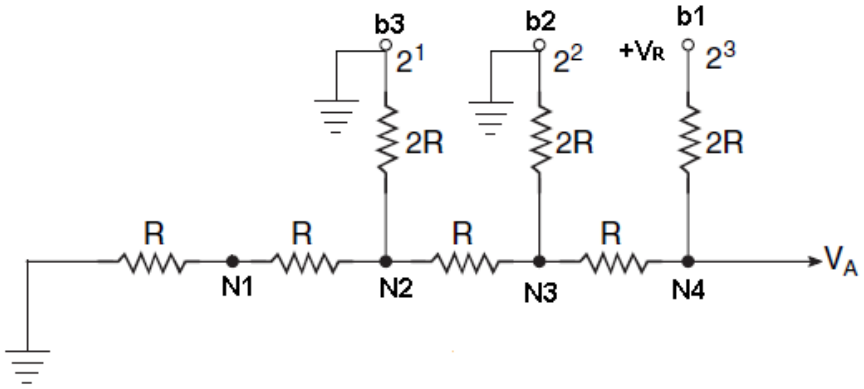

Figure 6.5:Equivant circuit of 1st stage

Now for N2 same thing happen B3 series with 2R and parallel with R + R resistors. It will also make equivalent resistor R at N3. g the bellow diagram

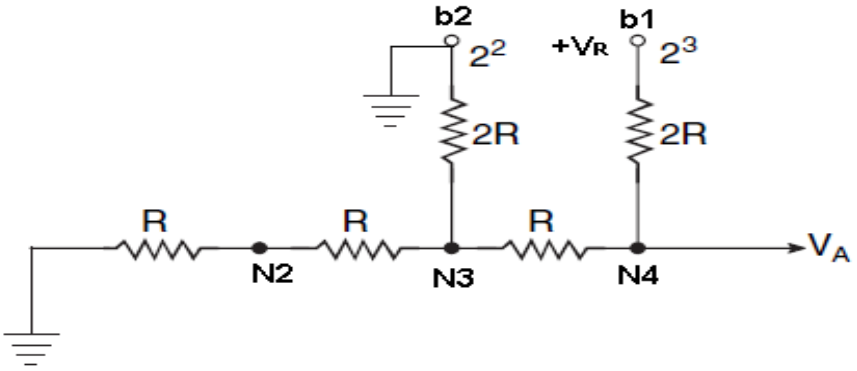

Figure 6.6:Equivant circuit of 2nd Stage

Repeating the same process we got equivalent of R resistor at N4

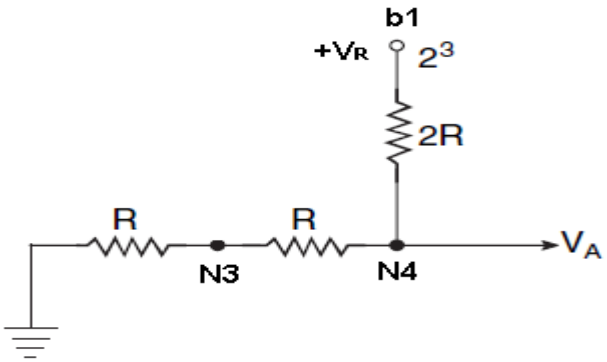

Figure 6.7:Equivant circuit of 3rd stage

$$V_A = \frac{V_R \times 2R}{R + R + 2R} = \frac{V_R}{2}$$

Thus for digital input $b_1b_2b_3b_4$ =1000 when MSB =1 , output is $V_R/2$, when second MSB is 1 output is $V_R/4$,for $b_1b_2b_3b_4$ =0010, output is $V_R/8$,and for $b_1b_2b_3b_4$ =0001, output is $V_R/16$. For n bit D/A converter

$$V_0 = \frac{V_R}{2^1} + \frac{V_R}{2^2} + \frac{V_R}{2^3} + \cdots + \frac{V_R}{2^n}$$

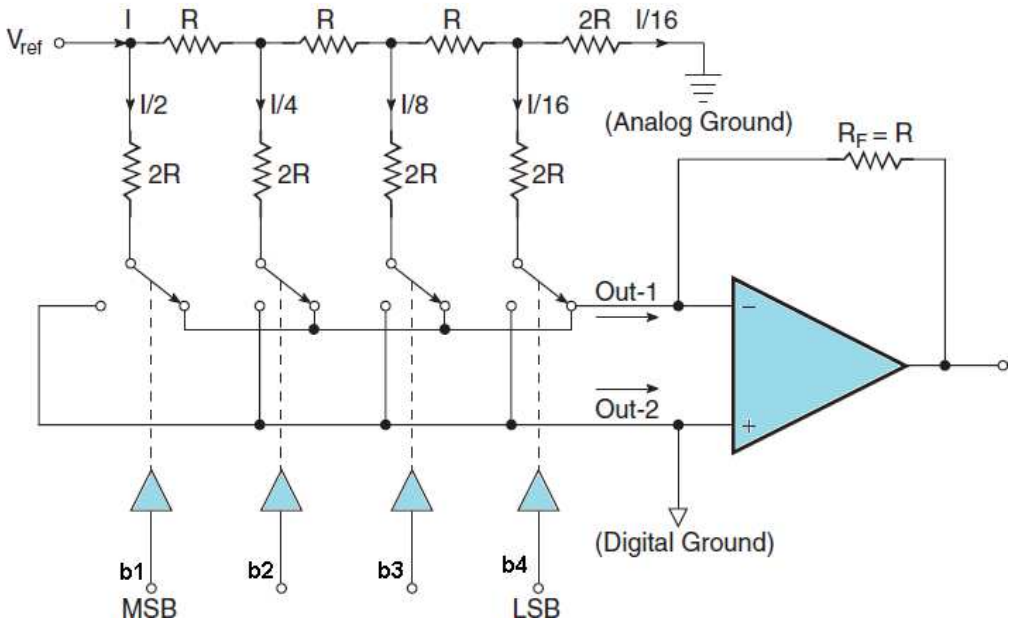

Figure 6.8:Equivant circuit for4 bit R-2R ladder D/A converter

Figure:Four bit R-2R ladder D/A converter

Figure shows 4 bit D/A converter using opamp. The inverting input terminal of the opamp acts as summing junction for the ladder for the ladder inputs. The output voltages V_o is expressed as

$$V_0 = -V_R \frac{R_f}{R}\left(\frac{b_1}{2^1} + \frac{b_2}{2^2} + \frac{b_3}{2^3} + \frac{b_4}{2^4}\right)$$

$$V_0 = -V_R \frac{R_f}{R \times 2^4}(b_1 2^3 + b_2 2^2 + b_3 2^1 + b_4 2^0)$$

More generally for an n bit input signal assuming R_f =R

$$V_0 = -\frac{V_R}{2^n}(b_1 2^{n-1} + b_2 2^{n-2} + \cdots . + b_n 2^0)$$

The resolution of R/2R ladder type D/A converter with current output is given as

$$\text{Resolution I} = \frac{1}{2^n} \times \frac{v_R}{R}$$

The resolution of R/2R ladder type D/A converter with voltage output is given as

$$\text{Resolution V} = \frac{1}{2^n} \times \frac{v_R}{R} \times R_f$$

Q.4 *Consider R-2R 4 bit converter and assume that feedback resistor Rf of the opamp is variable , the resistance R= 10kΩ and V_R = 10V.Determine the value of Rf that should be connected to achieve the following output condition.a) The value of 1 LSB at the output is 0.5V. b)An analog output of 6V for a binary input of 1000. c) The full scale output voltage of 12 V. d)The actual maximum output voltage of 10 V.*

Answer: R= 10kΩ and V_R = 10V, n=4

a) The value of 1 LSB at the output is 0.5V

$$\frac{\mathrm{R_f} \times 10}{10^4 \times 2^4} = 0.5$$

$$R_f = \frac{10^4 \times 2^4}{10} \times 0.5 = 8k\Omega$$

b) for a binary input of 1000, b_1=1 and b_2=b_3=b_4=0

$$6 = \frac{R_f \times 10 \times 2^{-1}}{10^4}$$

$$R_f = \frac{10^4}{10 \times 2^{-1}} \times 6 = 12k\Omega$$

c) For V_{FS} =12V

$$\frac{R_f \times 10}{10^4} = 12$$

$$R_f = \frac{10^4}{10} \times 12 = 12k\Omega$$

d) $b_1=b_2=b_3=b_4=1$,Thus for getting a full scale voltage 10v,

$$\frac{R_f \times 10}{10^4}(2^{-1} + 2^{-2} + 2^{-3} + 2^{-4}) = 10$$

$$R_f = \frac{10^4}{10 \times 0.9375} \times 10 = 10.66k\Omega$$

Q.5 *Explain the working of Counter type analog to digital converter with advantages and disadvantages.*

Answer: Counter type A/D converter is constructed using only one comparator with variable reference voltage.The variable reference voltage can be obtained by a sequence counter and D/A converter. The block diagram for an n bit counter type A/D converter is shown in figure.

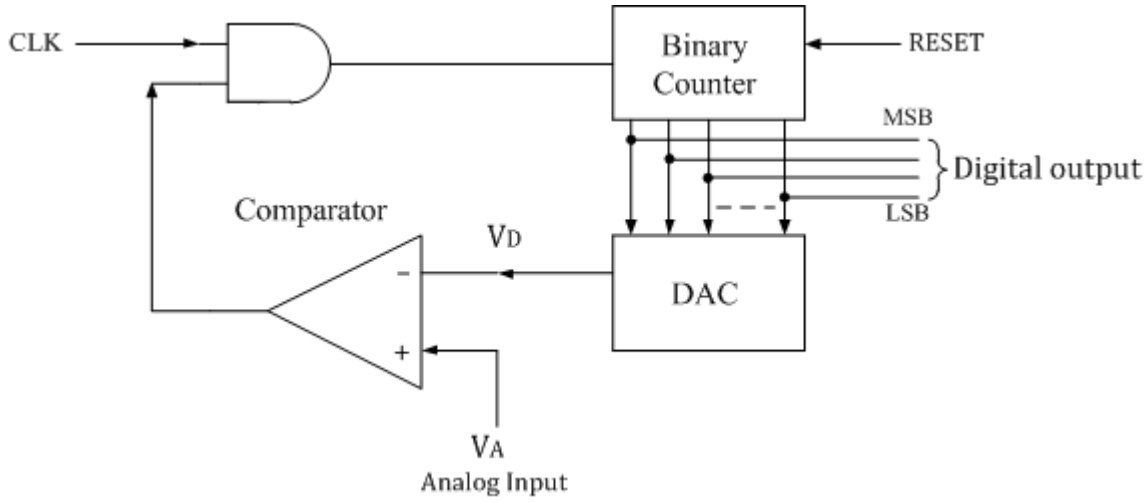

Figure 6.9: Counter type analog to digital converter

The n-bit binary counter is initially set to 0 by using reset command. Therefore the digital output is zero and the equivalent voltage VD is also 0V.

When the reset command is removed, the clock pulses are allowed to go through AND gate and are counted by the binary counter.

The D to A converter (DAC) converts the digital output to an analog voltage and applied as the inverting input to the comparator. The output of the comparator enables the AND gate to pass the clock. The number of clock pulses increases with time and the analog input voltage VD is a rising staircase waveform as shown in figure below.

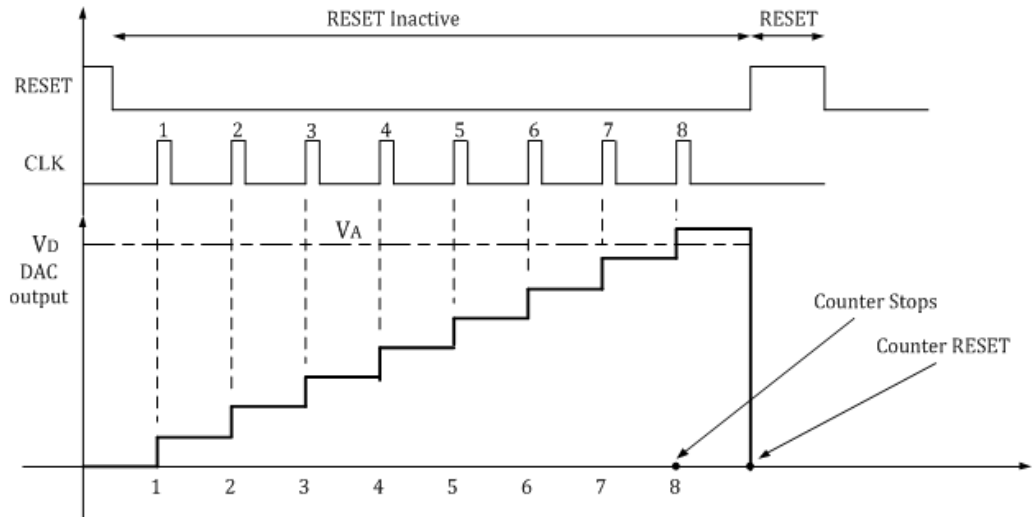

Figure 6.10: output *wavwform of* Counter type analog to digital converter

The counting will continue until the DAC output VD, equals and just rises more than unknown analog input voltage VA. Then the comparator output becomes low and this disables the AND gate from passing theclock. The counting stops at the instance VA< VD, and at that instant the counter stops its progress and the conversion is said to be complete.

Advantages:

1. The counter type A/D converter is very simple and needs less hardware compared to the simultaneous type A/D conveter.
2. This is suitable for digitizing application with high resolution.

Disadvantages:

In counter type A/D converter conversion time is very long , variable and proportional to amplitude of analog input voltages.

Q.6 *An 8 bit A/D converter accepts an input voltage signal of range 0 to 10V.a) What is the minimum value of input voltage required to generate a change of 1 LSB? b)What input voltage will generate all 1's at A/D converter output? c)What is the digital output for an input voltage of 4.8V.*

Answer:

a) ΔV_i for LSB $= \frac{V_{FS}}{2^n}$
$= \frac{10V}{2^8} = 39.1mV$

b) $Vi_{FS} = V_{FS} - 1LSB$
$V_{FS} = 10V - 39.1V = 9.961V$

c) digital output for an input voltage of 4.8V is given as

$$D = \frac{4.8V}{39.1mV} = 122.76 \cong 123$$

Q.7 *Design an astable multivibrator using 555 timer for a frequency of 1 kHz and a duty cycle of 70%. Assume C=0.1uF.*

Answer: The ON period $T_{ON} = 0.693(R_A + R_B)C_1$

The OFF period $T_{OFF} = 0.693(R_B)C_1$

The total time period T is given as $T = T_{ON} + T_{OFF} = 0.693(R_A + 2R_B)C_1$

Therefore Duty cycle D is given by

$$\text{Duty cycle } D = \frac{T_{ON}}{T} = \frac{R_A + R_B}{R_A + 2R_B}$$

$$D = \frac{R_A + R_B}{R_A + 2R_B} = \frac{7}{10}$$

Therefore

$$R_A = \frac{4}{3}R_B$$

The period of oscillation

$$T = 0.693 \times \frac{10}{3} R_B \times 10^{-7}$$

$$R_B = \frac{1 \times 10^4}{0.693 \times \frac{10}{3}} = 4.7k\Omega$$

Therefore

$$R_A = \frac{4}{3} \times 4700 = 6.8k\Omega$$

Q.8 *For the astable multivibrator shown in figure ,R_A = 2.2KΩ, R_B = 3.9 KΩ, and C= 0.1uF. Determine the positive pulse width t_c, negative pulse width t_d and free running frequency f_0.*

Answer:

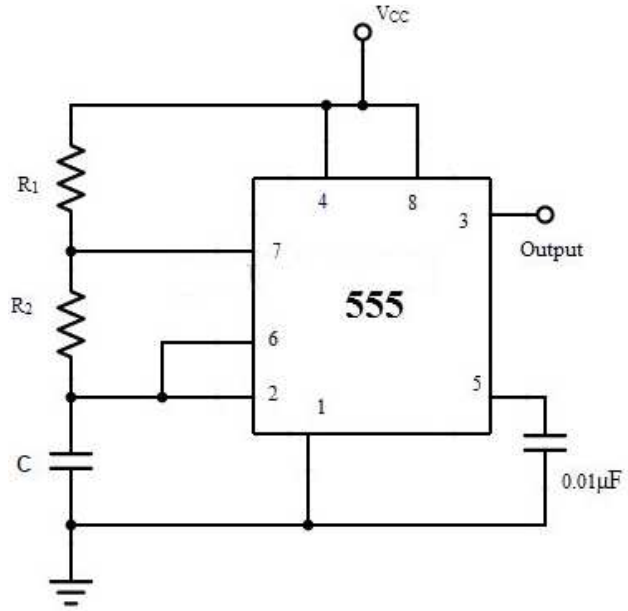

Figure 6.11: Astable multivibrator using IC 555

$$t_c = 0.69(R_A + R_B)C$$

$$t_c = (0.69)(2.2k + 3.9k)(0.1)(10^{-6}) = 0.421ms$$

$$t_d = 0.69(R_B)C$$

$$t_d = (0.69)(3.9k)(0.1)(10^{-6}) = 0.269ms$$

Therefore

$$f_0 = \frac{1}{T} = \frac{1.45}{\left((R_A + 2R_B)C\right)}$$

$$f_0 = \frac{1}{(0.421 + 0.269)(10^{-3})} = 1.45\text{kHz}$$

Q.9 Draw the block diagram of PLL and explain the working of each block in brief.

Phase Locked Loop **(PLL)** is one of the vital blocks in linear systems. It is useful in communication systems such as radars, satellites, FMs, etc.

A Phase Locked Loop (PLL) mainly consists of the following **three blocks** −

- Phase Detector
- Active Low Pass Filter
- Voltage Controlled Oscillator (VCO)

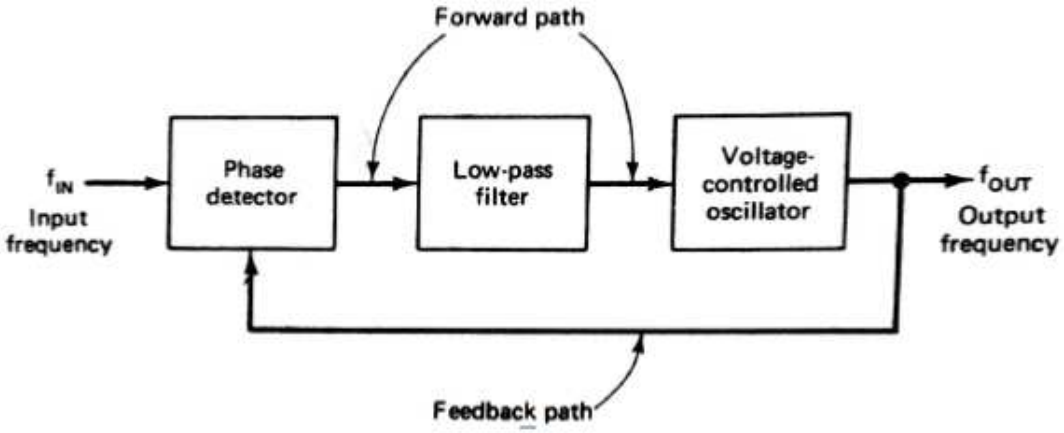

Figure 6.12: Block diagram of PLL

1. Phase DetectorThis comparator circuit compares the input frequency and the VCO output frequency and produces a dc voltage that is proportional to the phase difference between the two frequencies. The phase detector used in PLL may be of analog or digital type. Even though most of the monolithic PLL integrated circuits use analog phase detectors, the majority of discrete phase detectors are of the digital type. One of the most commonly used analog phase detector is the double balanced mixer circuit. Some of the common digital type phase detectors are

1.1 Exclusive OR Phase Detector

An exclusive OR phase detector is shown in the figure below.

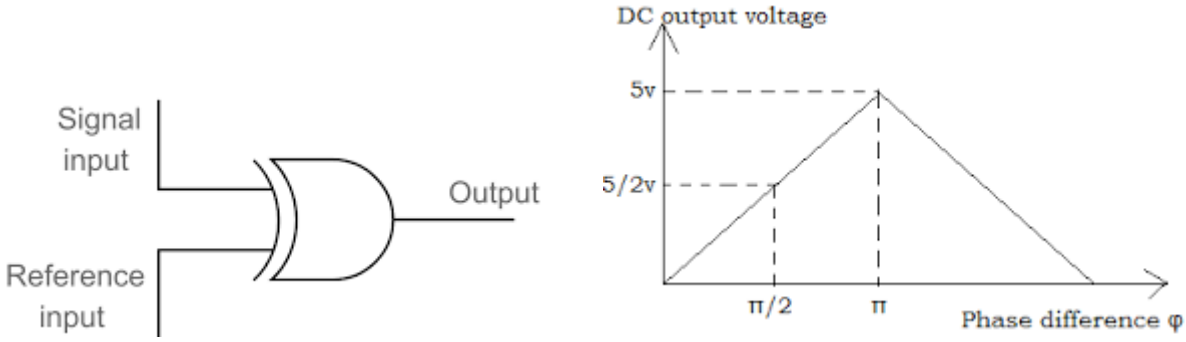

Figure 6.13: a)Exclusive-OR Phase Detector b) Exclusive-OR Phase Detector-Waveform

It is obtained as a CMOS IC of type 4070. Both the frequencies are provided as an input to the EX OR phase detector. Obeying the EX-OR concept the output becomes HIGH only if either of the inputs fi or fo becomes HIGH. All other conditions will produce a LOW output. Let us consider a waveform where the input frequency leads the output frequency by θ degrees. That is, fi and fo has a phase difference of θ degrees. The dc output voltage of the comparator will be a function of the phase difference between its two inputs.

The figure shows the graph of DC output voltage as a function of the phase difference between fi and fo. The output DC voltage is maximum when the phase detector is 180°.This type of phase detector is used when both fi and fo are square waves.

Exclusive-OR Phase Detector-Waveform

1.2 Edge Triggered Phase Detector

Edge triggered phase detector is used when fi and fo are pulse waveforms with less than 50% duty cycles. The figure of such a phase detector using an R-S Flip Flop is shown below. Two NOR Gate (CD4001) are cross-coupled to form an R-S Flip Flop. The output of the phase detector changes it's logic state by triggering of the R-S Flip Flop. That is, the output of the phase detector changes its logic state on the positive edge of the input fi and fo. The advantage of such a detector can be understood from the graph below. It is clear that the DC output voltage is linear over 360°.

1.3 Monolithic Phase Detectors

The monolithic type phase detector uses a CMOS type 4044 IC ,Which is highly advantages as the harmonic sensitivity and duty cycle problems are neglected and the circuit will be respond only to the transition in the input signals. This is the most preferred phase detector in the critical applications as the phase error and the output error voltage are independent of variations in the amplitude and duty cycles of the input waveforms.

2. Low Pass Filter (LPF)

A Low Pass Filter (LPF) is used in Phase Locked Loops (PLL) to get rid of the high frequency components in the output of the phase detector. It also removes the high frequency noise. All these features make the LPF a critical part in PLL and helps control the dynamic characteristics of the whole circuit. The dynamic characteristics include capture and lock ranges, bandwidth, and transient response. The lock range is the tracking range where the range of frequencies of the PLL system follows the changes in the input frequency. The capture range is the range in which the Phase Locker Loops attains the Phase Lock.

When the filter bandwidth is reduced, the response time increases .But this reduces the capture range. But it also helps in reducing noise and in maintaining the locked loop through momentary losses of signal. Two types of passive filter are used for the LPF circuit in a PLL. An amplifier is used also with LPF to obtain gain. The active filter used in PLL is shown below.

3. Voltage Controlled Oscillator (VCO)

The main function of the VCO is to generate an output frequency that is directly proportional to the input voltage. The connection diagram of a SE/NE 566 VCO is shown in the figure below. The macimum frequency of the VCO is 500 KHz.

This VCO provides simultaneous square wave and triangular wave outputs as a function of the input voltage. The frequency of oscillation is determined by the resistor R and capacitor C along with the voltage Vc applied to the control terminal.

A. Monolithic Phase Locked Loop

PLL is now readily available as IC's which were developed in the SE/NE 560 series. Some of the commonly used ones are the SE/NE 560,561,562,564,565 and 567.The difference between each one of them is in the different parameters like operating frequency range, power supply requirements, and frequency and bandwidth ranges. Out of all the series the SE/NE 565 is the most famous. It is available as a 14-pin DIP and also as a 10-pin metal can package. The 14-pin DIP and its characteristics are given below.

Q.10 *Design a circuit to initiate the signal to operate blinking of traffic alert signal On for 0.25ms and OFF for 0.75 ms using IC 555 timer.*

Answer:

Astable multivibrator design

T_{ON}= 0.25ms ,T_{OFF} = 0.75 ms

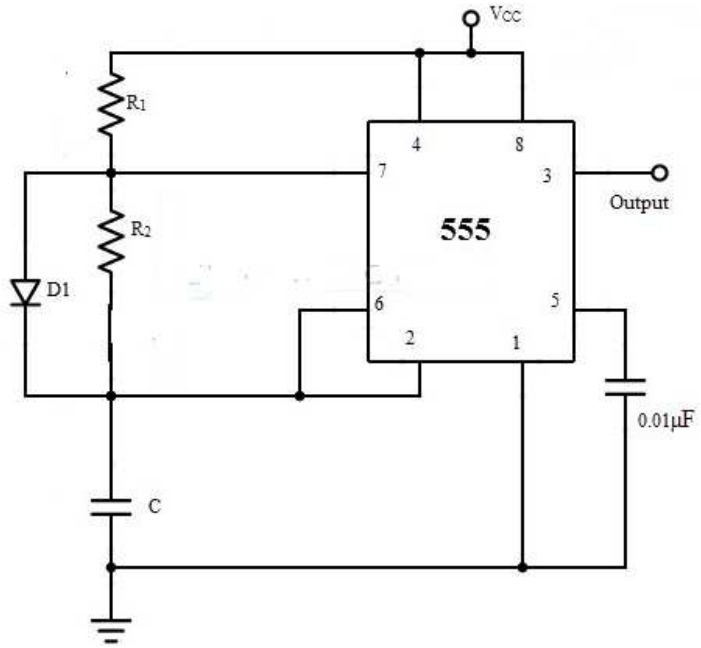

Figure 6.14: 555 Timer

$$\%D = \frac{T_{on}}{T_{on} + T_{OFF}} \times 100 = 25\%$$

Duty cycle is less than 50% therefore using astable with diode across R_B

$T_{ON} = 0.69(R_A)C$

$T_{OFF} = 0.69(R_B)C$

Assume C= 0.1uF

$$R_A = \frac{T_{ON}}{0.693 \times C} = 3.607k\Omega$$

$$R_B = \frac{T_{OFF}}{0.693 \times C} = 10.822k$$

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Author Profile

A.V.Gokhale

Y.A.Gaidhani