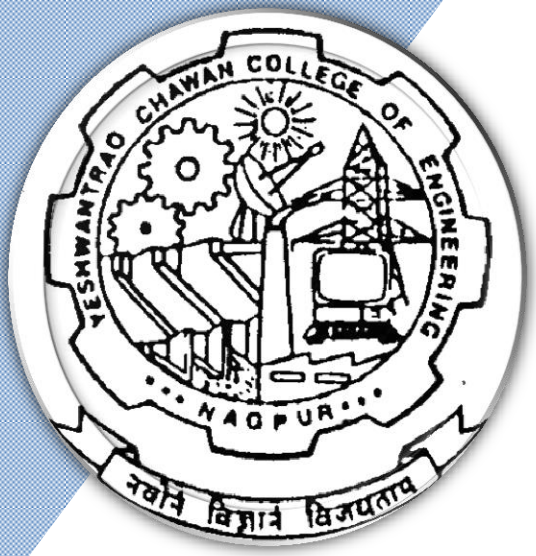
Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

(Accredited 'A' Grade by NAAC with a score of 3.25)

Hingna Road, Wanadongri, Nagpur - 441 110



Bachelor of Engineering
Honors in VLSI Design
Offered by Electronics Engineering
SoE & Syllabus 2018

28 June 2020

Nagar Yuwak Shikshan Sanstha's

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B.E. MINORS SCHEME OF EXAMINATION 2018

(Revised Scheme of Examination w.e.f. 2020-21 onward)

B.E Honors VLSI Design

Offered by Electronics Engineering

SN	Sem	Type	Sub. Code	Subject	T/P	Contact Hours				Credits	% Weightage			ESE Duration Hours
						L	T	P	Hrs		MSEs*	TA**	ESE	
B.E Honors VLSI Design														
1	5	PC	EE2501	Synthesis & Optimization of VLSI Circuits	T	3	0	0	3	3	30	30	40	3 Hours
2	5	PC	EE2502	Advanced Digital System Design	T	3	0	0	3	3	30	30	40	3 Hours
3	5	PC	EE2503	Lab: Advanced Digital System Design	P	0	0	2	2	1		60	40	
4	6	PC	EE2511	VLSI Testing	T	3	0	0	3	3	30	30	40	3 Hours
5	6	PC	EE2512	Digital IC Design	T	3	0	0	3	3	30	30	40	3 Hours
6	6	PC	EE2513	Lab: Digital IC Design	P	0	0	2	2	1		60	40	
7	7	PC	EE2521	Low Power CMOS VLSI Design	T	3	0	0	3	3	30	30	40	3 Hours
8	7	PC	EE2522	Lab: Low Power CMOS VLSI Design	P	0	0	2	2	1		60	40	
					TOTAL	**15**	**0**	**6**	**21**	**18**				

MSEs* = Three MSEs of 15 Marks each will conducted and marks of better 2 of these 3 MSEs will be considered for Continuous Assessment

TA ** = for Theory : 20 marks on lecture quizzes, 8 marks on assignments, 2 marks on class performance

TA = for Practical : MSPA will be 15 marks each**

		June 2020	**1.02**	**Applicable for AY 2020-21 Onwards**
Chairperson	**Dean (Acad. Matters)**	**Date of Release**	**Version**	

V Semester
Synthesis & Optimization of VLSI Circuits

Objective	Outcomes
➢ The objective of this course is to acquaint concept of Optimization of Very Large Scale Integration (VLSI) circuit and. systems design	At the end of this course, students will 1. Understand basic Boolean functions, their representations and different CAD based synthesis and optimization issues. 2. Understand, able to analyze and solve the algorithms which underpin behavioral synthesis including scheduling, allocationand binding. 3. Understand and able to analyze high level synthesis issues, twolevel logic optimization, multilevel logic optimization, andsequential logic optimization. 4. Understand and able to apply the Satisfiability (SAT) concept.

Unit-I

Microelectronics, semiconductor technologies and circuit taxonomy, microelectronic design styles, computeraided synthesis and optimization. Graphs Notation, undirected graphs, directed graphs, combinatorialoptimization, Algorithms, tractable and intractable problems, algorithms for linear and integer programs, graphoptimization problems and algorithms, Boolean algebra and Applications.

Unit – II

Hardware Modeling Languages, distinctive features, structural hardware language, Behavioral hardwarelanguage, HDLs used in synthesis, abstract models, structures logic networks, state diagrams, data flow andsequencing graphs, compilation and optimization techniques.

Unit - III

Logic optimization, principles, operation on two level logic covers, algorithms for logic minimization, symbolic minimization and encoding property, minimization of Boolean relations. Multiple level combinationaloptimizations: Models and transformations

Unit - IV

combinational networks, algebraic model, Synthesis of testable network, algorithm for delay evaluation andoptimization, rule based system for logic optimization. Sequential circuit optimization, Sequential circuitoptimization using state based models, sequential circuit optimization using network models.

Unit – V

A model for scheduling problems, Scheduling with resource and without resource constraints, Schedulingalgorithms for extended sequencing models, Scheduling Pipe lined circuits. Cell library binding, Problemformulation and analysis, algorithms for library binding, specific problems and algorithms for library binding(lookup table F.P.G.As and Antifuse based F.P.G.As), rule based library binding.

Unit –VI

Simulation, Types of simulators, basic components of a simulator, fault simulation Techniques, Automatic testpattern generation methods (ATPG), design for Testability (DFT) Techniques.

References:

1 "Synthesis and Optimization of Digital Circuits" ,Giovanni De Micheli, 110 st Edition, Tata McGraw-Hill, 2003.
2 "Logic Synthesis" SrinivasDevadas, AbhijitGhosh, and Kurt Keutzer,1st Edition, McGraw-Hill, USA, 1994.

V Semester
Advanced Digital System Design

Objective	Outcomes
➢ To expose students to the advanced design techniques and methodology and industrial standard EDA tools in Digital Circuits and Systems design	After study through lectures and assignments, 1. Graduates will be able to design and analyse combinational and sequential logic circuits. 2. Graduates will understand hardware description language and able to design and simulate digital systems using different abstraction levels 3. Graduates will be able to understand and apply timing issues in multiple contexts and design the circuit. 4. Graduates will understand programmable devicesand able to design digital systems using modern design tools

Unit - I

Digital Design Fundamentals, Combinational & Sequential design issues, Introduction to finite state machines,Moore& Mealy Machine, Introduction to programmable devices, PLA, PAL, PROM, Structure of CPLDs,Introduction to FPGA, Architecture, CLB, IOB, Programmable Interconnect Points, Different type ofprogrammable switches used in PLDs.[8 Hours]

Unit - II

HDL Based Design flow, Requirements of HDL, Design Methodologies, Different Modelling styles, Introductionto Verilog, Elements of Verilog, Verilog Module definition, Elements of Module.[6 Hours]

Unit – III

Basic Concepts in Verilog, Reserved Keywords, Syntax & Semantics, Comments, Identifiers, NumberRepresentation, System Representation, Verilog Ports, Verilog Data Types, Wire & Variables, Physical &Abstract, Constants, Parameter, Verilog Data Operators, Design entry in Verilog &Testbench, Compilationand synthesis, Timing analysis.
[7 Hours]

Unit – IV

Data Flow Modelling, Delay, Continuous Assignment, Delayed Continuous assignment, Structural ModellingFeature, Module Instantiation, Gate level Primitives, Gate Delays, Switch Level Primitives, User DefinedPrimitives.
[6 Hours]

Unit - V

Behavioral Modelling, Initial, Always, Procedural Assignment, Blocking and Non- Blocking assignments,Sequential& Parallel Blocks, Race around Condition, Timing Control, Procedural Statements, ConditionalStatements if case loop repeat forever etc, Zero Delay Control, Event Based Timing Control, CompilerDirectives, Assign Deassign, Force Release, Latch Models, FF Models, State Machine Coding ,Moore andMealy Machines.[8 Hours]

Unit - VI

Combinational & sequential system Design examples like Shift Registers, Counters, LFSR, Stacks andQueues, Multi bit Adders & Multiplier, Huffman Coding, Processor and Memory Model , CPU, System Tasksand Functions, Design Verification.[6 Hours]

Text books:

1. "Verilog Digital System Design" - ZainalabedinNavabi , Second Edition, Tata McGraw Hill , 2009
2. "Verilog HDL : A Guide to Digital Design and Synthesis" ,Samir Palnitkar, 2nd Edition 2003.

V Semester

Lab: Advanced Digital System Design

Objective	Outcomes
➢ To expose students to the advanced design techniques and methodology and industrial standard EDA tools in Digital Circuits and Systems design	After study through lectures and assignments, 1. Graduates will be able to design and analyse combinational and sequential logic circuits. 2. Graduates will understand hardware description language and able to design and simulate digital systems using different abstraction levels 3. Graduates will be able to understand and apply timing issues in multiple contexts and design the circuit. 4. Graduates will understand programmable devicesand able to design digital systems using modern design tools

Exp No	Name of Experiment
1	Verilog Code using Bitwise Operator .Test it with test stimuli generated by test bench
2	Using GATE level primitive write verilog code and test it with test stimuli generated by test bench
3	Verilog code using DATA flow modelling style. Test it with test stimuli generated by test bench
4	Write verilog code using conditional assignment statement. Test it with test stimuli generated by test bench
5	Write verilog code using Structural Modeling style. Test it with test stimuli generated by test bench.
6	Verilog code using Behavioural modeling style. Test it with test stimuli generated by test bench
7	Write UDP for A. Combinational Circuit B.Sequential circuit
8	Write Verilog code using switch level modeling for a. NAND gate b. Full adder using transmission gate
9	Write verilog code using while loop
10	Write Verilog code for Mealy and Moore sequence detector.(using overlapping allowed and not allowed)

VI Semester
VLSI Testing

Objectives	Outcomes
To gain a knowledge from the area of applying diagnostic principles in the design of modern Electronic systems	1. .Students develop an understanding of VLSI design verification and testing issues. 2. 2. Students learn how to generate test patterns for faults in a system and how to design a system for testability. 3. 3. Ability to model different faults and carry out fault simulation in digital circuits. 4. 4. Ability to know about importance of testing and its types in VLSI circuits.

Unit I : Overview Of Testing: Design Process, Verification, Faults & Their Detection, Test Pattern Generation, Fault Coverage, Types Of Tests, Test Application, Testing Economics. Defects, Failures, and Faults: Physical Defects, Failures Modes, Faults, Fault Equivalence and Dominance, Fault Collapsing

Unit II : Design Representation: Graphical representation, Graphs, Binary Decision diagrams, Netlists, VLSI Design Flow: CAD tools, Design Methodologies, Semicustom Design

Unit III : Simulation: Logic Simulation, Approaches to Simulation, Fault Simulation & Their Results. Automatic Test Pattern Generation: D-Algorithm, Critical Path Extensions to D-Algorithm PODEM

Unit IV : Ad Hoc Techniques, Scan–Path Design, Test pattern generation, Test Pattern Application, Scan architectures, multiple scan chains, Partial Scan Testing

Unit V : Boundary-Scan Testing: Boundary Scans Architecture, Test Access Port, Registers, Tap Controller, Modes of Operation. Built In Self Test: Pseudorandom Test Pattern Generation, Response Compaction, BIST Architectures

Unit VI : Memory Testing: Types of Memory Testing, Functional Testing Schemes, Testing FPGAs and Microprocessors: Testability Of FPGAs, Testing RAM- Based FPGAs, Testing Microprocessors, Synthesis For Testability.

Resources:
1. "Principles of Testing Electronic Systems", 2nd edition SamihaMourad, YervantZorian
2. "Essentials of Electronic Testing for Digital, Memory, and Mixed-Signal VLSI Circuits",MichaelL.Bushnell and Vishwani D. Agrawal, B.S.Publications, 20003.
3. "Digital Systems Testing and Testable Design" ,MironAbramovici, Melvin Breuer and Arthur Friedman, IEEE press,
4. "A Guide to VHDL" by Stanley Mazor,2nd Edition, Kluwer Academic Press, 20075. "HDL Chip Design" by Douglas Smith, 3rd Edition, Doone Publications, 2008 6. "Rapid Prototypin

VI Semester
Digital IC Design

Objectives	Outcomes
➢ The aim of this course is to give knowledge and skills in the area of CAD design of digital circuits, units and systems oncurrently usable VLSI chips.	1. Graduates will able to demonstrate issues related to the 2. development of digital integrated circuits including fabrication, circuit design, implementation methodologies 3. Graduates will able to Solve complex circuit problems and optimization techniques 4. Graduates will able to design CMOS combinational, sequential logic design 5. Graduates will able to designprogrammable logic arrays

UNIT-1:CMOS processing technology: (8 Hours)

MOS transistors, CMOS logic, NAND gate, combinational logic, NOR gate, Compound gates, Pass transistor and transmissiongates, tri-states, multiplexers, latches and flip flops, inverter cross section, fabrication process, Layout design rules, CMOSprocessing technology, CMOS Process enhancements, stick diagram, VLSI design flow ,Euler path in a CMOS gate.

UNIT-2:MOS transistor theory: (7 Hours)

MOS transistor theory, Working of NMOS enhancement transistor & PMOS enhancement transistor, Ideal Current voltagecharacteristics, threshold voltage , non-ideal current voltage effects, velocity saturation, mobility degradation, channel lengthmodulation, Body effect, sub-threshold conduction, Junction leakage, Tunneling, Temperature dependence, Geometrydependence, Small signal AC characteristics, CMOS inverter DC transfer characteristics, Beta ratio effects, noise margin,Ratioed inverter transfer function, switch level RC delay models

UNIT-3 : **Circuit characterization and performance estimation:** (7 Hours)

Delay estimation, RC delay models, linear delay model, logical effort, parasitic delay, Delay in a logic gate, delay in a multistagelogic networks, power dissipation, interconnect, design margin, Reliability, Scaling

UNIT-4:Combinational circuit design: (8 Hours)

Circuit families, static CMOS, Ratioed circuits, Cascode voltage switch logic, dynamic circuits, pass transistor circuits, differentialcircuits, sense amplifier circuits, Bi-CMOS circuits

UNIT-5:Sequential Circuit design: (8 Hours)

Sequencing static circuits, Sequencing methods, Max-delay constraints, Min-delay constraints, Time borrowing, clock skew,circuitdesign of latches and Flip flops, static sequencing element methodology, Two phase timing types, characterizing sequencingelement delays, sequencing dynamic circuits, Synchronizers.

UNIT-6:Array subsystems: (8 Hours)

Static Random access memory, Dynamic random access memory, serial access memories,Content addressable memoryProgrammable logic arrays.

Textbooks:

1. "CMOS VLSI design: A Circuits and Systems Perspective", Neil H. E. Weste, David F. Harris, A.Banerjee, 3rd Edition, Addison Wesley
Publication, 2008
2. "CMOS Digital Integrated Circuits: Analysis and Design", Sung-Mo Kang, Yusuf Lebeleci, 3rd Edition, McGraw-Hill Publications, 2002

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Chairperson	Dean (Acad. Matters)	Date of Release	Version	

VI Semester
Lab: Digital IC Design

Objectives	Outcomes
➢ To design & analyze the performance of MOS circuits	1. Graduates will able to design layout of basic gates, 2. Graduates will able to design layout of combinational &sequential logic circuits for the given technology using EDA tools 3. Graduates will able to optimize complex circuits 4. Graduate will be able to apply lambda/micron rules for designinglayout

Exp No.	Name of Experiment
1	a) Plot current voltage characteristics of NMOS transistor using 0.5 micron technology b) Plot current voltage characteristics of PMOS transistor using 0.5 micron technology
2	To design and simulate CMOS inverter using 0.5 micron technology
3	A plot transfer characteristic of Pseudo-NMOS inverter with w/l for PMOS is equal to twice w/l of NMOS.
4	Design and simulate two input CMOS NAND gate
5	Design two input CMOS NOR gate.
6	Design CMOS transmission gate.
7	Design and simulate D-Latch using transmission gate
8	Design 2:1 MUX using transmission gate.
9	Design two input CMOS XOR gate
10	Design function f=not(A+B+C+D) using Euler path approach

VII Semester
Low Power CMOS VLSI Design

Objective	Outcomes
➢ To expose students to the advanced design techniques and methodology and industrial standard EDA tools in Digital Circuits and Systems design	1. Graduates will understand the concepts of sources of power dissipation and basics of CMOS Physics. 2. Graduates will understand the concepts of levels of abstraction and its power dissipation. 3. Graduates will understand the Power Optimization methods at Behaviour, Logic and Circuit Level design. 4. Graduates will understand the principles for low power designs, and have the capabilities to analyze power consumption and develop low power strategies for a given system.

Unit I

Need for low power VLSI chips, Sources of power dissipation: Short circuit dissipation, dynamic dissipation,designing Techniques for low power. Physics of power dissipation in MOSFET devices, MOS Capacitance analysis, low power figure of merits, brief overview of low power VLSI design limits.

Unit II

Probabilistic power analysis: random logic signals, probability and frequency, probabilistic power analysis techniques, signal entropy, Low power circuits: transistor and gate sizing, equivalent pin ordering, network reconstruction and reorganization, Glitching Power, special latches and flip-flops.

Unit III

Behavioural, Logic and circuit level approaches. Algorithm level transforms. Circuit activity drivenarchitectural transformations, voltage scaling, operation reduction and substitution, pre-computation, Logic:gate reorganization, signal gating, logic encoding.

Unit IV

Design style, Leakage current in Deep sub-micron transistors, device design issues, minimizing shortchannel effect. Low voltage design techniques using reverse Vgs. Steep sub threshold swing and multiple threshold voltages. Multiple threshold CMOS based on path critically, multiple supply voltages.

Unit V

Low energy computing, Energy dissipation in transistor channel. Energy recovery circuit design, designs with reversible and partially reversible logic, energy recovery in adiabatic logic and SRAM core, Design of peripheral circuits – address decoder, level shifter and IO Buffer, supply clock generation

Unit VI

Introduction, sources of software power dissipation, power estimation and optimization. Co-design for low power

Test Books:

1."Solid State Electronic Devices", 6th Edition, Ben Streetman, Sanjay Benerjee.
2. "Low-Power CMOS VLSI Circuit Design", Kaushik Roy, Sharat C. Prasad, 1st Edition, Wiley India,2009
3. "Practical Low Power Digital VLSI Design", Gary K. Yeap, Kluwer Academic Publisher, 2002
4. "Low-Power CMOS Circuits-Technology, Logic Design and CAD Tools" Christian Piguet, 2006 by Taylor & Francis Group, LLC
5. "Energy Efficient Microprocessor Design", T. D. Burd and R. A. Brodersen, Boston: Springer, 2002.
6. "Low-Power Digital CMOS Design", A. Chandrakasan and R. Brodersen, Boston: Springer, 1995.
7. "Digital Integrated Circuits: A Design Perspective", 2nd ed., J. Rabaey, A. Chandrakasan, B. Nikolic.

VII Semester
Lab: Low Power CMOS VLSI Design

Objective	Outcomes
➢ To expose students to the advanced design techniques and methodology and industrial standard EDA tools in Digital Circuits and Systems design	1. Graduates will understand the concepts of sources of power dissipation and basics of CMOS Physics. 2. Graduates will understand the concepts of levels of abstraction and its power dissipation. 3. Graduates will understand the Power Optimization methods at Behaviour, Logic and Circuit Level design. 4. Graduates will understand the principles for low power designs, and have the capabilities to analyze power consumption and develop low power strategies for a given system.

Exp No	Name of Experiment
1	Plot current voltage characteristics of NMOS transistor using CMOS technology
2	Design 4:1 MUX using basic gates and with complementary CMOS Logic.
3	Design function $F=\overline{(A*B*C)+(D*E)}$ with complementary CMOS Logic and pseudo NMOS Logic.
4	Design function $F=\overline{(A+B)*(C+D)}$ with complementary CMOS Logic and pseudo NMOS Logic.
5	Design two input CMOS XOR gate
6	Design two input CMOS XNOR gate
7	Design adiabatic Half Adder
8	Design adiabatic Full Adder
9	Design adiabatic 4:1 Multiplexer