

YESHWANTRAO CHAVAN COLLEGE OF ENGINEERING

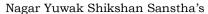
(An Autonomous Institution affiliated to R T M Nagpur University Nagpur) Accredited by NAAC (1stCycle) with 'A' Grade (Score 3.25 on 4 Point Scale)

Wanadongri, Hingna Road, Nagpur-441110

Department of Electronics & Communications Engineering (Honors in VLSI Design)



B.E. Honors in VLSI Design (NPTEL) SoE & Syllabus 2021-22





Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

Department of Electronics & Telecommunication Engineering SoE and Syllabus B.E Honors in VLSI Design(NPTEL)

SoE No. HON-101

B.E Honors in VLSI Design (NPTEL Based)

Information Brochure of Honor Program

1. Title of Program: VLSI Design

2. Type of Program: Honor

3. Department offering the program: Electronics & Telecommunication Engineering

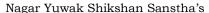
4. Industry / Association / Collaboration: NPTEL / SWAYAM based Course

5. Department/s eligible to opt for the program: Only Department of Electronics & Telecommunication Engineering students are permitted to opt for this program.

6. General information about courses in program:

The electronics industry has achieved a phenomenal growth over the last two decades, mainly due to the rapid advances in integration technologies, large-scale systems design - in short, due to the advent of VLSI. The number of applications of integrated circuits in high-performance computing, telecommunications, and consumer electronics has been rising steadily, and at a very fast pace. Typically, the required computational power (or, in other words, the intelligence) of these applications is the driving force for the fast development of this field. The current leading-edge technologies (such as low bit-rate video and cellular communications) already provide the end-users a certain amount of processing power and portability. This trend is expected to continue, with very important implications on VLSI and systems design. One of the most important characteristics of information services is their increasing need for very high processing power and bandwidth (in order to handle real-time video, for example). The other important characteristic is that the information services tend to become more and more personalized (as opposed to collective services such as broadcasting),

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| Chairperson | Dean (Acad. Matters) | Date of Release | Version | 7112021 22 011110a100 | |





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which means that the devices must be more intelligent to answer individual demands, and at the same time they must be portable to allow more flexibility/mobility.

As more and more complex functions are required in various data processing and telecommunications devices, the need to integrate these functions in a small system/package is also increasing. The level of integration as measured by the number of logic gates in a monolithic chip has been steadily rising for almost three decades, mainly due to the rapid progress in processing technology and interconnects technology.

7. Advance knowledge or research orientation of Program:

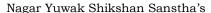
- > Very Large Scale Integrated (VLSI) Circuit Design is the process of designing a large computer chip (more specifically, an integrated circuit, or IC), using computer-aided design (CAD) tools on a workstation or a personal computer (PC).
- > The course demands learning the principles of VLSI design, designing and fabricating the state of-the-art VLSI chips, understanding the complete design flow and expertise to design CMOS chips for industrial requirements.
- > Well balanced curriculum catering to the needs of industry as well as the research community.
- > The curriculum focuses on employing hierarchical design methods and understanding the design issues at the various levels of hierarchy.
- > Students are exposed to various design softwares in this programme. Also, they learn to design, simulate, implement and test complex digital systems using FPGAs (Field Programmable Gate Arrays).
- > Students are trained in several topics that cut across different domain, starting from lowermost level of physical devices to the top level of application development.

8. Employability potential of program:

> Increasing Importance Of VLSI

Today, VLSI gadgets can be found all around us. We can find progressed VLSI contributions to our vehicles, mobile phones, electronic appliances, cameras, medicinal machines, and many different places. This rapidly growing sector is opening its doors in verification based

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employment opportunities for those with solid basics in electronic circuit structure and hardware description languages, VLSI designing and verification.

With the development in electronic gadgets, higher technology like utilities, procedure geometries, and product innovation consistently, there is a constant requirement to design, build and re-make integrated circuits (ICs). Since devices like cell phones are being made with new features in a very short time. There is a high demand for skilled VLSI (Very Large Scale Integration) designers to take a shot at these products. Thus, there is a huge demand for qualified VLSI professionals in semiconductor industry.

> Career Prospects On VLSI

As the design and manufacturing industries are expanding, hence the demand for VLSI skilled professionals is also enhancing. If the students are planning to begin a career in the semiconductor industry then you should have a sound knowledge of jobs and growth opportunities in the VLSI domain.

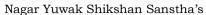
9. Departmental Steering committee: For proper publicity / conduct of program

| SN | Name of the Faculty | Post | Designation | e-mail ID | Contact | | | | | | |
|----|---------------------|------------------------|--------------|---------------------------|------------|--|--|--|--|--|--|
| | Member | | | | Number | | | | | | |
| 1. | Dr. M. S. Narlawar | HoD | Chairman BoS | hod_et@ycce.edu | 9763822298 | | | | | | |
| 2. | Dr. M.S. Dorle | Assistant Professor | Co-ordinator | mdorle@gmail,com | 9881711748 | | | | | | |
| 3. | Dr. D. B. Bhoyar | Assistant Professor | Member | Dinesh.bhoyar23@gmail.com | 9923448822 | | | | | | |
| 4. | Dr. B.Y. Masram | Assistant Professor | Member | bharatimasram@gmail.com | 9970879459 | | | | | | |

10. Program Coordinator:

| SN | Name of the Faculty Po | | Designation | e-mail ID | Contact |
|----|------------------------|-----------|-------------|------------------|------------|
| | Member | | | | Number |
| | Dr. M.S. Dorle | Assistant | Со- | mdorle@gmail,com | 9881711748 |
| | | Professor | ordinator | | |

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|-------------|----------------------|-----------------|---------|----------------------------------|--|
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SoE and Syllabus B.E Honors in VLSI Design(NPTEL)

SoE No. **HON-101**

Scheme of Examinations B.E Honors in VLSI Design

| | | | | | C | onta | ct H | ours | | % | % Weightage | | ESE | | |
|--|-----|--------------|--|-----|---|------|------|-----------|----------|--|-------------|-----|-------------------|--|--|
| SN | Sem | Sub. Code | Subject | T/P | L | T | P | Hrs | Credits | MSEs* | TA** | ESE | Duration Hours | | |
| B.E Honors in VLSI Design (NPTEL Based) Any six co | | | | | | | | ny six co | urses to | be chose | n | | | | |
| 1. | V | ETHN01 | CMOS Digital VLSI Design | T | | | | | | This is SWAYAM / NPTEL based program and COURSES with 12–14-week syllabus are expected to be available on SWAYAM/NPTEL platform. If they are not available before the commencement of semester, Similar / Equivalent Subjects shall be notified by BoS of the | | | | | |
| 2. | V | ETHN02 | Digital System Design | T | | | | | | | | | | | |
| 3. | V | ETHN03 | VLSI Technology | T | | | | | | | | | | | |
| 4. | VI | ETHN11 | Analog IC Design | T | | | | | | | | | | | |
| 5. | VI | ETHN12 | Architectural Design of Digital Integrated Circuits | T | | | | | | | | | | | |
| 6. | VI | ETHN13 | VLSI Design or CMOS VLSI Circuits | T | | | | | | | | | | | |
| 7. | VII | ETHN21 | VLSI Testing or Digital VLSI Testing or VLSI design Verification | T | | | | | | Department. Chairman BoS will notify all the subjects which are 12-14 week duration before the | | | fy all the | | |
| 8. | VII | ETHN22 | VLSI Physical Design or VLSI Design | T | | | | | | | | | | | |
| 9. | VII | ETHN23 | Advanced VLSI Design | T | | | | | | | | | | | |
| | | | ТО | TAL | | | | | | | | | | | |

MSEs* = Three MSEs of 15 Marks each will conducted and marks of better 2 of these 3 MSEs will be considered for Continuous Assessment

TA ** = for Theory : 20 marks on lecture quizzes, 8 marks on assignments, 2 marks on class performance TA** = for Practical : MSPA will be 15 marks each

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|-------------|----------------------|-----------------|---------|----------------------------------|
| Chairperson | Dean (Acad. Matters) | Date of Release | Version | 7.112021 22 011114140 |