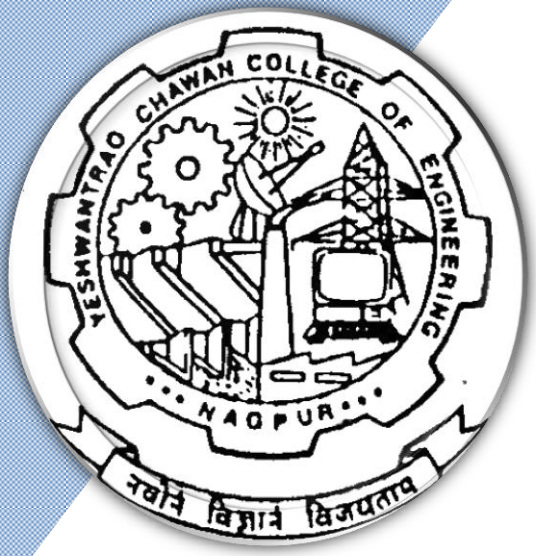
Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

(Accredited 'A' Grade by NAAC with a score of 3.25)

Hingna Road, Wanadongri, Nagpur - 441 110



SoE & Syllabus 2019

M.Tech. Electronics Engineering

28 June 2019

Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

M. Tech. SCHEME OF EXAMINATION 2019

Electronics Engineering

SN	Sem	Sub Code	Subject	T/P	Contact Hours				Credits	% Weightage			ESE Duration
					L	T	P	Hrs		MSEs*	TA	ESE	
I SEMESTER													
1	1	EE3901	Advanced Digital Signal Processing	T	3	0	0	3	3	30	10	60	3
2	1	EE3902	**Lab:** Advanced Digital Signal Processing	P	0	0	2	2	1	40		60	
3	1	EE3903	Digital IC Design	T	3	0	0	3	3	30	10	60	3
4	1	EE3904	**Lab:** Digital IC Design	P	0	0	2	2	1		40	60	
5	1	EE3905	RISC & DSP Processor Architecture	T	3	0	0	3	3	30	10	60	3
6	1	EE3906	Advanced Digital System Design	T	3	0	0	3	3	30	10	60	3
7	1	EE3907	**Lab:** Advanced Digital System Design	P	0	0	2	2	1		40	60	
8	1	EE3908	Advanced Communication Systems	T	3	0	0	3	3	30	10	60	3
9	1	**Professional Elective- I**		T	3	0	0	3	3	30	10	60	3
Total					**18**	**0**	**6**	**24**	**21**				

List of Professional Electives-I

1	EE3909	PE I: Analog IC Design
1	EE3910	PE I: Multirate signal Processing
1	EE3911	PE I: Low Power CMOS VLSI Design
1	EE3912	PE I :Biomedical Instrumentation

II SEMESTER

1	2	EE3915	RF Circuit Design	T	3	0	0	3	3	30	10	60	3
2	2	EE3916	**Lab:** RF Circuit Design	P	0	0	2	2	1		40	60	
3	2	EE3917	Artificial Intelligence	T	3	0	0	3	3	30	10	60	3
4	2	EE3918	Digital Image Processing	T	3	0	0	3	3	30	10	60	3
5	2	EE3919	**Lab :** Digital Image Processing	P	0	0	2	2	1		40	60	
6	2	**Professional Elective- II**		T	3	0	0	3	3	30	10	60	3
7	2	**Professional Elective- III**		T	3	0	0	3	3	30	10	60	3
8	2	**Professional Elective- IV**		T	3	0	0	3	3	30	10	60	3
Total					**18**	**0**	**4**	**22**	**20**				

List of Professional Electives-II

2	EE3920	PE II: Wireless Communication
2	EE3921	PE II: VLSI Signal Processing
2	EE3922	PE II: Verification & Testing of VLSI Circuit

List of Professional Electives-III

2	EE3923	PE III :Wireless Sensor
2	EE3924	PE III :Mixed signal VLSI Design
2	EE3925	PE III :Cryptography & Network Security

List of Professional Electives-IV

2	EE3926	PE IV :Adaptive Signal Processing
2	EE3927	PE IV :Embedded System & RTOS
2	EE3928	PE IV :Advanced Computer Architecture
2	EE3929	PE IV :Pattern recognition

III SEMESTER

1	3	EE3939	Project Phase - I	P	0	0	16	16	8	100			
Total					**0**	**0**	**16**	**16**	**8**				

IV SEMESTER

1	4	EE3940	Project Phase - II	P	0	0	24	24	12	40	60	
Total					**0**	**0**	**24**	**24**	**12**			
Grand Total of Credits									**62**			

MSEs* = Three MSEs of 15 Marks each will be conducted and marks of better 2 of these 3 MSEs will be considered for Continuous Assessment

		June 2019	**1.00**
Chairperson	**Dean (Acad. Matters)**	**Date of Release**	**Version**

Applicable for Sem 1 & 2 AY 2019-20 & Sem 3 & 4 AY 2020-21 Onwards

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M. Tech. Scheme of Examination & Syllabus 2019

Electronics Engineering

I Semester

EE3901	**Advanced Digital Signal Processing**	L= 3	T = 0	P = 0	Credits = 3

Evaluation Scheme	MSEs *	TA	ESE	Total	ESE Duration
	30	10	60	100	3 Hrs

MSEs* = Three MSEs of 15 Marks each will be conducted and marks of better 2 of these 3 MSEs will be considered for Continuous Assessment

Objective	Outcomes
To acquaint students with advanced methods of digital signal processing and their application in practice. Design and testing of systems for advanced signal processing, aiming at optimum and adaptive noise reduction, identification and modeling of systems, reconstruction and restoration, analysis and classification of signals and images	1. Graduates will be able classify the transfer functions based on systems. 2. Graduates will understand and able to design and realize FIR and IIR filters using different methodologies. 3. Graduates will able to implement the DSP algorithms. 4. Graduates will understand and analyse multirate signal processing concepts.
Mapped Program Outcomes: a, d	

SN	Course Outcomes	Mapped PO						
		a	b	c	d	e	f	g
1	Graduates will be able classify the transfer functions based on systems.				S			
2	Graduates will understand and able to design and realize FIR and IIR filters using different methodologies.	S			L			
3	Graduates will able to implement the DSP algorithms.	S			S			
4	Graduates will understand and analyze multirate signal processing concepts.	S			M			

Unit I: LTI Discrete Time Systems in the Transform Domain

Transfer function classification based on Magnitude characteristics, Transfer function classification based on phase characteristics, Types of linear phase transfer functions, Simple Digital Filters, Complementary Transfer Functions, Inverse Systems, System Identification, Digital Two pairs, Algebraic Stability Test.

UNIT II: Digital Filter Structures

Block Diagram representation, Equivalent Structures, Basic FIR Digital filter structures, Basic FIR Digital filter structures, All pass Filters, Tunable IIR filters, IIR Tapped Cascaded Lattice Structures , IIR Tapped Cascaded Lattice Structures, Parallel All pass Realization Of IIR Transfer Functions, Digital Sine-Cosine Generator, Computational Complexity of Digital Filter Structures.

UNIT III: IIR Digital Filter Design and FIR Digital Filter Design

Preliminary Considerations, Bilinear Transformation Method of IIR Filter Design, Design of Lowpass IIR Digital Filters, Design of High pass, Band pass, and Band stop IIR Digital Filters, Preliminary Considerations, FIR Filter Design Based on Windowed Fourier Series, Design of linear phase, minimum phase FIR filters, Design of Computationally efficient FIR Digital filters.

UNIT IV: DSP Algorithm Implementation

Computation of Discrete Fourier Transform, Fast DFT Algorithms Based on index mapping, DFT and IDFT Computation, Sliding Discrete Fourier Transform, DFT Computation over a Narrow Frequency Band, Number representation, Arithmetic Operations, Handling of Overflow, Tunable Digital Filters.

UNIT V: Analysis of Finite Word length effect

The Quantization Process and Errors, Quantization of Fixed point Numbers, Quantization of floating point Numbers, Analysis of Coefficient Quantisation Effects, A/D conversion Noise Analysis, Analysis Of Arithmetic Round off Errors, Dynamic Range Scaling, Signal To noise ratio in low order IIR Filters, Low Sensitivity Digital Filters, Reduction of product round off errors using Error Feedback, Limit Cycles in IIR Digital Filters, Round Off Errors in FFT Algorithm.

UNIT VI: Multirate DSP

Decimation by a factor D – Interpolation by a factor I – Filter Design and implementation for sampling rate conversion, Polyphase filter structure.

Resources:

1. Digital Signal Processing, A Computer – Based approach, by Sanjit K. Mitra, Tata Mc Graw-Hill, 2008,3rd edition.
2. Digital Signal Processing. Principles, algorithms, and applications by John G. Proakis and Dimitris G.Manolakis, PHI, 1997.3rd edition
3. Oppenheim and Schafer, Discrete Time signal Processing, Prentice Hall, 2nd edition.
4. Theory and applications of digital signal processing by Lawrence R. Rabiner and Bernard Gold, PHI,1st edition

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M. Tech. Scheme of Examination & Syllabus 2019

Electronics Engineering

I Semester

EE3902	Lab.: Advanced Digital Signal Processing	L= 0	T = 0	P = 2	Credits = 1

Evaluation Scheme	Continuous Evaluation	ESE	Total	ESE Duration
	40	60	100	

Objective	Outcomes
To acquaint students with advanced methods of digital signal processing and their application in practice. Design and testing of systems for advanced signal processing.	1. Graduates will able to design and realize FIR and IIR filters using different methodologies using software 2. Graduates will be able to do statically and parametric analysis of the signals using software.
Mapped Program Outcomes: a, c, e, f	

Sr. No.	Course Outcomes	Mapped PO						
		a	b	c	d	e	f	g
1	Graduates will able to design and realize FIR and IIR filters using different methodologies using software	S		M		L	L	
2	Graduates will be able to do statically and parametric analysis of the signals using software.	S		M		L	L	

S.N.	Name of the experiment
1	Write a MATLAB program and function to generate different time signals. [CO2(M)]
2	To perform a signal manipulation (sine, cosine, ramp, exponential etc.). [CO2(M)]
3	To perform convolution and correlation generating function. [CO2(M)]
4	To find z-transform and plot pole zero plot. [CO2(M)]
5	To find DFT and IDFT of sequence in MATLAB. [CO1(S),CO2(M)]
6	To determine the circular convolution using MATLAB. [CO1(S),CO2(M)]
7	Design of IIR filter using windowing technique. [CO1(S),CO2(M)]
8	Design of IIR filter using Bilinear transformation. [CO1(S),CO2(M)]
9	Design of IIR/FIR filter using FDA tool. [CO1(S),CO2(M)]
10	To study and design LPF/HPF/BPF/BRF by simulink. [CO1(S),CO2(M)]

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Electronics Engineering

I Semester

EE3903	**Digital IC Design**	L= 3	T = 0	P = 0	Credits = 3

Evaluation Scheme	MSEs *	TA	ESE	Total	ESE Duration
	30	10	60	100	3 Hrs

MSEs* = Three MSEs of 15 Marks each will be conducted and marks of better 2 of these 3 MSEs will be considered for Continuous Assessment

Objective	Outcomes
• The aim of this course is to give knowledge and skills in the area of CAD design of digital circuits, units and systems on currently usable VLSI chips.	1. Graduates will able to demonstrate issues related to the development of digital integrated circuits including fabrication, circuit design, implementation methodologies 2. Graduates will able to Solve complex circuit problems and optimization techniques 3. Graduates will able to design CMOS combinational, sequential logic design
Mapped Program Outcomes: a, d	

Sr.	Course Outcomes	Mapped PO						
		a	b	c	d	e	f	g
1	Graduates will able to demonstrate issues related to the development of digital integrated circuits including fabrication, circuit design, implementation methodologies	H						
2	Graduates will able to Solve complex circuit problems and optimization techniques				M			
3	Graduates will able to design CMOS combinational, sequential logic design				M			

Unit I: CMOS processing technology:

MOS transistors, CMOS logic, NAND gate, combinational logic, NOR gate, Compound gates, Pass transistor and transmission gates, tristates, multiplexers, latches and flip flops, inverter cross section, fabrication process, Layout design rules, CMOS processing technology, CMOS Process enhancements, stick diagram, VLSI design flow ,Euler path in a CMOS gate.

Unit II: MOS transistor theory:

MOS transistor theory, Working of nMOS enhancement transistor & PMOS enhancement transistor, Ideal Current voltage characteristics, threshold voltage , nonideal current voltage effects, velocity saturation, mobility degradation, channel length modulation, Body effect, sub-threshold conduction, Junction leakage, Tunnelling, Temperature dependence, Geometry dependence, Small signal AC characteristics, CMOS inverter DC transfer characteristics, Beta ratio effects, noise margin, Ratioed inverter transfer function, switch level RC delay models

Unit III: Circuit characterization and performance estimation:

Delay estimation, RC delay models, linear delay model, logical effort, parasitic delay, Delay in a logic gate, delay in a multistage logic networks, power dissipation, interconnect, design margin, Reliability, Scaling

Unit IV: Combinational circuit design:

Circuit families, static CMOS, Ratioed circuits, Cascode voltage switch logic, dynamic circuits, pass transistor circuits, differential circuits, sense amplifier circuits, BiCMOS circuits

Unit V: Sequential Circuit design:

Sequencing static circuits, Sequencing methods, Max-delay constraints, Min-delay constraints, Time borrowing, clock skew, circuit design of latches and Flip flops, static sequencing element methodology, Two phase timing types, characterizing sequencing element delays, sequencing dynamic circuits, Synchronizers.

Unit VI: Array subsystems:

Static Random access memory, Dynamic random access memory, serial access memories,Content addressable memory Programmable logic arrays.

Resources:

1. "CMOS VLSI design: A Circuits and Systems Perspective", Neil H. E. Weste, David F. Harris, A.Banerjee, 3rd Edition, Addison Wesley Publication, 2008
2. "CMOS Digital Integrated Circuits: Analysis and Design", Sung-Mo Kang, Yusuf Lebeleci, 3rd Edition, McGraw-Hill Publications, 2002

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I Semester

EE3904	Lab: Digital IC Design	L= 0	T = 0	P = 2	Credits = 1

Evaluation Scheme	Continuous Evaluation	ESE	Total	ESE Duration
	40	60	100	

Objective	Outcomes
To design & analyze the performance of MOS circuits	1. Graduates will able to design layout of basic gates, combinational & sequential logic circuits for the given technology using EDA tools 2. Graduates will able to optimize complex circuits 3. Graduate will be able to apply lambda/micron rules for designing layout
Mapped Program Outcomes: c, d, e, f	

Sr. No.	Course Outcomes	Mapped PO						
		a	b	c	d	e	f	g
1	Graduates will able to design layout of basic gates, combinational & sequential logic circuits for the given technology using EDA tools			H	H	H	H	
2	Graduates will able to optimize complex circuits			H	H	H	H	
3	Graduate will be able to apply lambda/micron rules for designing layout			H	H	H	H	

Sr. No	Name of Experiment	Mapping with CO
1.	a) Plot current voltage characteristics of nmos transistor using 0.5 micron technology b) Plot current voltage characteristics of PMOS transistor using 0.5 micron technology	CO1,CO3
2.	To design and simulate CMOS inverter using 0.5 micron technology	CO1,CO3
3.	Plot transfer characteristics of pseudo-nmos inverter with w/l for pmos is equal to twice w/l of nmos.	CO1,CO2,CO3
4.	Design and simulate two input CMOS NAND gate	CO1,CO2,CO3
5.	Design two input CMOS NOR gate.	CO1,CO2,CO3
6.	Design CMOS transmission gate.	CO1,CO2,CO3
7.	Design and simulate D-Latch using transmission gate	CO1,CO2,CO3
8.	Design 2:1 MUX using transmission gate	CO1,CO2,CO3
9.	Design two input CMOS XOR gate	CO1,CO2,CO3
10.	Design function f=not(A+B+C+D) using Euler path approach	CO1,CO2,CO3

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M. Tech. Scheme of Examination & Syllabus 2019

Electronics Engineering

I Semester

EE3905	**RISC & DSP Processor Architecture**	L= 3	T = 0	P = 0	Credits = 3

Evaluation Scheme	MSEs *	TA	ESE	Total	ESE Duration
	30	10	60	100	3 Hrs

MSEs* = Three MSEs of 15 Marks each will be conducted and marks of better 2 of these 3 MSEs will be considered for Continuous Assessment

Objective	Outcomes
• The aim of this course is to give knowledge and skills in the area of embedded system particularly RISC architecture & develop a system around processor core particularly ARM core. • Also this subject will provide knowledge about DSP Processors and associated hardware experimentation.	1. Graduates will understand architectural details of ARM7, DSP processor & Embedded System. 2. Graduates will be able to demonstrate the Embedded based system design 3. Graduates will be able to interface various peripheral devices with processor to solve engineering problems.
Mapped Program Outcomes: a, b, d	

S	Course Outcomes	Mapped PO						
		a	b	c	d	e	f	g
1	Graduates will understand architectural details of ARM7, DSP processor & Embedded System.	H	L		L			
2	Graduates will be able to demonstrate the Embedded based system design		H		M			
3	Graduates will be able to interface various peripheral devices with processor to solve engineering problems.		H		M			

Unit – I: Introduction to Embedded Systems, RISC architecture, CISC architecture, Introduction to VLIW architecture, Von Neuman & Harward architecture, pipelining, MEMORY organization.

Unit– II: Architectural Features of ARM: Processor modes, Register organization, ARM exceptions, ARM and THUMB instruction sets, Programming, ARM development tools.

Unit–III : Pipeline ARM organisation, ARM instruction execution, Timing diagrams for data path, Co-processor interface, Hardware and software breakpoints, Exceptions and its handling, Memory faults.

Unit–IV : ARM architectural support for high level language programming, floating point data types, functions and procedures, Thumb instruction set, The ARM memory interface, the advanced buses: AMBA, ASB, APB, ARM Debugger.

Unit–V : Peripherals: Arm ADC, Real Time Clock, UARTs, SPI, Communication Protocols: I2C Bus, Control Area Network, Bluetooth

Unit–VI : DSP Architecture: MAC, Modified bus structures and Memory access schemes, multiple access Memory, Multi-ported memory, Pipelining, Special addressing modes, 32 bit floating point DSP Processor: architecture, block diagram, functional units, on chip memory, on chip peripherals.

Resources:

1. "ARM System-on-Chip Architecture", Steve Furber ,2nd Edition, Pearson Education,2002
2. "Digital signal processors",B. Venkataramani, M Bhaskar, 1st Edition, Tata McGraw Hill , 2002
3. "Embedded System Design", Frank Vahid and Tony Givargis, 1st Edition, Wiely Publication, 2002
4. Technical reference manuals from TI
5. "ARM System Developer's Guide: Designing and Optimizing", Sloss Andrew N, Symes Dominic, Wright Chris, Morgan Kaufman Publication.2004
6. Embedded Linux, Hardware, Software and interfacing 2002. Craig Hallabaugh Addison-Wesley Professional
7. "Embedded Systems: Architecture, Programming and Design" Raj Kamal 2nd Edition Tata McGraw-Hill Edication

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M. Tech. Scheme of Examination & Syllabus 2019

Electronics Engineering

I Semester

EE3906	Advanced Digital System Design	L= 3	T = 0	P = 0	Credits = 3

Evaluation Scheme	MSEs *	TA	ESE	Total	ESE Duration
	30	10	60	100	3 Hrs

MSEs* = Three MSEs of 15 Marks each will be conducted and marks of better 2 of these 3 MSEs will be considered for Continuous Assessment

Objective	Outcomes
• To expose students to the advanced design techniques and methodology and industrial standard EDA tools in Digital Circuits and Systems design.	1. Graduates will be able to design and analyse combinational and sequential logic circuits. 2. Graduates will understand hardware description language and able to design and simulate digital systems using different abstraction levels. 3. Graduates will be able to understand and apply timing issues in multiple contexts and design the circuit. 4. Graduates will understand programmable devices and able to design digital systems using modern design tools.
Mapped Program Outcomes: a, c, d	

SN	Course Outcomes	Mapped PO						
		a	b	c	d	e	f	g
1	Graduates will be able to design and analyse combinational and sequential logic circuits.	H			H			
2	Graduates will understand hardware description language and able to design and simulate digital systems using different abstraction levels.	H			H			
3	Graduates will be able to understand and apply timing issues in multiple contexts and design the circuit.	L			M			
4	Graduates will understand programmable devices and able to design digital systems using modern design tools.	L		L				

Unit - I

Digital Design Fundamentals, Combinational & Sequential design issues, Introduction to finite state machines, Moore & Mealy Machine, Introduction to programmable devices, PLA, PAL, PROM, Structure of CPLDs, Introduction to FPGA, Architecture, CLB, IOB, Programmable Interconnect Points, Different type of programmable switches used in PLDs

Unit - II

HDL Based Design flow, Requirements of HDL, Design Methodologies, Different Modelling styles, Introduction to Verilog, Elements of Verilog, Verilog Module definition, Elements of Module

Unit – III

Basic Concepts in Verilog, Reserved Keywords, Syntax & Semantics, Comments, Identifiers, Number Representation, System Representation, Verilog Ports, Verilog Data Types, Wire & Variables, Physical & Abstract, Constants, Parameter, Verilog Data Operators, Design entry in Verilog & Testbench, Compilation and synthesis, Timing analysis

Unit – IV

Data Flow Modelling, Delay, Continuous Assignment, Delayed Continuous assignment, Structural Modelling Feature, Module Instantiation, Gate level Primitives, Gate Delays, Switch Level Primitives, User Defined Primitives

Unit - V

Behavioural Modelling, Initial, Always, Procedural Assignment, Blocking and Non- Blocking assignments, Sequential & Parallel Blocks, Race around Condition, Timing Control, Procedural Statements, Conditional Statements if case loop repeat forever etc, Zero Delay Control, Event Based Timing Control, Compiler Directives, Assign De-assign, Force Release, Latch Models, FF Models, State Machine Coding ,Moore and Mealy Machines

Unit - VI

Combinational & sequential system Design examples like Shift Registers, Counters, LFSR, Stacks and Queues, Multi bit Adders & Multiplier, Huffman Coding, Processor and Memory Model, CPU, System Tasks and Functions, Design Verification

Resources:

1. "Verilog Digital System Design" - Zainalabedin Navabi , Second Edition, Tata McGraw Hill , 2009
2. "Verilog HDL : A Guide to Digital Design and Synthesis" ,Samir Palnitkar, 2nd Edition , Prentice Hall India, 2003
3. "A Verilog HDL Primer", J. Bhaskar, 2nd Edition, Star Galaxy Press, 1997

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M. Tech. Scheme of Examination & Syllabus 2019

Electronics Engineering

I Semester

EE3907	Lab: Advanced Digital System Design	L= 0	T = 0	P = 2	Credits = 1

Evaluation Scheme	Continuous Evaluation	ESE	Total	ESE Duration
	40	60	100	

Objective	Outcomes
To learn front end Digital System design flow.	1. Graduates will be able to design, simulate and synthesize digital systems using Modern digital system design tools. 2. Graduates will be able to apply timing issues in multiple contexts.
Mapped Program Outcomes: c, d, e, f	

Sr. No.	Course Outcomes	Mapped PO						
		a	b	c	d	e	f	g
1.	Graduates will be able to design, simulate and synthesize digital systems using Modern digital system design tools.			H		H	H	
2.	Graduates will be able to apply timing issues in multiple contexts.				H	M	H	

Sr. No	Name of Experiment
1	Verilog Code using Bitwise Operator .Test it with test stimuli generated by test bench.[CO1(H),CO2(H)]
2	Using GATE level primitive write verilog code and test it with test stimuli generated by test bench. [CO1(H),CO2(H)]
3	Verilog code using DATA flow modeling style. Test it with test stimuli generated by test bench. [CO1(H),CO2(H)]
4	Write verilog code using conditional assignment statement. Test it with test stimuli generated by test bench. [CO1(H),CO2(H)]
5	Write verilog code using Structural Modeling style. Test it with test stimuli generated by test bench. [CO1(H),CO2(H)]
6	Verilog code using Behavioral modeling style. Test it with test stimuli generated by test bench. [CO1(H),CO2(H)]
7	Write UDP for A. Combinational Circuit B.Sequential circuit [CO1(H),CO2(H)]
8	Write verilog code using switch level modeling for a. NAND gate b. Full adder using transmission gate [CO1(H),CO2(H)]
9	Write verilog code using while loop. [CO1(H),CO2(H)]
10	Write Verilog code for Mealy and Moore sequence detector.(using overlapping allowed and not allowed). [CO1(H),CO2(H)]
11	Mini Project[CO1(H),CO2(H)]

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M. Tech. Scheme of Examination & Syllabus 2019

Electronics Engineering

I Semester

EE3908	Advanced Communication System	L= 3	T = 0	P = 0	Credits = 3

Evaluation Scheme	MSEs *	TA	ESE	Total	ESE Duration
	30	10	60	100	3 Hrs

MSEs* = Three MSEs of 15 Marks each will be conducted and marks of better 2 of these 3 MSEs will be considered for Continuous Assessment

Objective	Outcomes
• To acquaint students to the advanced communication systems and methodology and various Issues related with Communication.	1. Graduates will be able to understand basic theory of digital communications and the most common digital communications techniques. 2. Graduates will be able to apply and analyze mathematical modeling to the problems in digital communications. 3. Graduates will be able to demonstrate the concept of modulation technique used in digital communication 4. Graduates will be able to understand error control coding and optimum receivers in communication systems.
Mapped Program Outcomes: a, d	

SN	Course Outcomes	Mapped PO						
		a	b	c	d	e	f	g
1	Graduates will be able to understand basic theory of digital communications and the most common digital communications techniques.	M			H			
2	Graduates will be able to apply and analyze mathematical modeling to the problems in digital communications.	H			M			
3	Graduates will be able to demonstrate the concept of modulation technique used in digital communication	L			M			
4.	Graduates will be able to understand error control coding and optimum receivers in communication systems.	L			H			

Unit I

Random Process: Mathematical Definition of a Random Process, Stationary Processes, Mean, Correlation and Covariance functions ,Transmission of a Random Process Through a linear Time Invariant Filter, Power Spectral Density, Gaussian Process, Noise, Narrowband Noise, Representation of Narrowband Nose in terms of In Phase and Quadrature components, Representation of Narrowband Noise in terms of Envelope and Phase components. .[CO1-M,CO2-H]

Unit II

Characterization of Communication Signals and Systems- Signal space representation- Vector space concept, signal space concept, orthogonal expansions of signals, representation of digitally modulated signals-memory less modulation methods, [CO1-M,Co2-H]

Unit III

Pulse Modulation techniques
Minimum Shift Keying (MSK) Modulation, GMSK, Continuous Phase Modulation (CPM) Schemes Channel Characterization and Modeling, Orthogonal Frequency Division Multiplexing (OFDM), Carrier Synchronization, Timing synchronization. [CO1-L,CO2-M,CO3-H]

Unit IV

Optimum receiver for signals corrupted by AWGN, performance of the Optimum receiver for memory less modulation, Optimum receiver for CPM signals Optimum receiver for signal with random phase in AWGN channel. The optimum filter, Schwarz's inequality, transfer function of optimum filter, matched filter, properties of Matched filter, correlation receiver. [CO2-M,CO3-S]

Unit V

Channel Capacity and Convolution Coding::Channel models, Channel Capacity, Transfer convolution Codes, Optimum decoding of convolution codes-Viterbi algorithm, Fano algorithm, Punctured convolution codes. [CO1-L,CO3-H]

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Unit VI

Spread spectrum signals for digital communications: Introduction to Spread Spectrum Modulation, DSSS, FHSS, and CDMA signals, Code Acquisition and Tracking, Spread Spectrum as a Multiple Access Technique. [CO1-M,CO3-H]

Resources:

1. "Communication Systems", Simon Haykins, 4th edition,John Wiley and sons,INC
2. "Digital Communication", J.G. Proakis, 4th edition, McGraw Hill, 1995.
3. "Digital Communication", Edward. A. Lee and David. G. Messerschmitt, 2nd Edition, Allied Publishers, 2003

		June 2019	1.00	Applicable for Sem 1 & 2 AY 2019-20 & Sem 3 & 4 AY 2021-22 Onwards
Chairperson	Dean (Acad. Matters)	Date of Release	Version	

Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

M. Tech. Scheme of Examination & Syllabus 2019

Electronics Engineering

I Semester

EE3909	PE I: Analog IC Design	L= 3	T = 0	P = 0	Credits = 3

Evaluation Scheme	MSEs *	TA	ESE	Total	ESE Duration
	30	10	60	100	3 Hrs

MSEs* = Three MSEs of 15 Marks each will be conducted and marks of better 2 of these 3 MSEs will be considered for Continuous Assessment

Objective	Outcomes
To understand the functions of various digital and analog ICs and their applications in the design of electronic circuits.	1. Graduates will able to demonstrate behaviour of single, multiple transistor amplifiers. 2. Graduates will able to Solve complex circuit problems 3. Graduates will able to model integrated circuit devices 4. Graduates will be able to design nonlinear analog circuits.
Mapped Program Outcomes: a, d	

SN	Course Outcomes	Mapped PO						
		a	b	c	d	e	f	g
1	Graduates will able to demonstrate behaviour of single, multiple transistor amplifiers.	H			M			
2	Graduates will able to Solve complex circuit problems				H			
3	Graduates will able to model integrated circuit devices	H			M			
4	Graduates will be able to design nonlinear analog circuits.				L			

Unit I: Models for integrated circuit active devices:

Depletion region of a p-n junction, Small Signal & large signal behavior of MOS & BJT transistor, short channel effects in MOS transistors, weak inversion in MOS transistor, substrate current in MOS transistor

Unit II: Single transistor and multiple transistor amplifiers:

Basic Single transistor Amplifiers stages: Common Emitter, Common base, Common Collector, Common Drain, Common Gate & Common Source Amplifiers, Multiple Transistor Amplifier stages: CC-CE, CC-CC, & Darlington configuration, Cascode configuration, Active Cascode, Super source follower, Differential pairs, DC transfer characteristics.

Unit III: Current Mirrors, Active Loads & References:

Current Mirrors: Simple current mirror, Cascode current mirrors, Widlar current mirror, Wilson Current mirror, Active loads, Voltage & current references, supply and temperature independent biasing techniques

Unit IV: Operational Amplifier with single ended outputs:

Deviations from ideality in real operational amplifiers, Basic two stage op amp, two stage MOS Operational Amplifier with cascodes, MOS telescopic-cascode operational amplifiers, MOS Folded-cascode operational amplifiers, MOS active cascade operational amplifiers, Bipolar operational amplifiers

Unit V: Frequency response of integrated circuits:

Single stage amplifiers & miller effect, MOS differential amplifier differential mode gain, frequency response of the common mode gain for a differential amplifier, frequency response of voltage buffers, frequency response of current buffers, Multistage amplifier frequency response, frequency response of a current mirror loading a differential pair.

Unit VI: Nonlinear Analog Circuits:

Analysis of four quadrants, Gilbert cell as an analog multiplier, Phase Locked Loops, Integrated circuit phase locked loops, Voltage controlled oscillators, Switched Capacitor Circuits and Switched Capacitor Filters.

Resources:

1) "Analysis and Design of Analog Integrated Circuits", Paul B Gray ,hurst ,Lewis, Meyer ,fifth edition, John Wiley & sons, reprint 2010.
2) "CMOS Analog Circuit Design"P.E.Allen,D.R.Holdberg,second edition,Oxford univ. press.2010
3) "CMOS circuit design, Layout, and simulation" R.Jacob Baker, second edition, Wiley student edition, reprint 2009

		June 2019	1.00	Applicable for Sem 1 & 2 AY 2019-20 & Sem 3 & 4 AY 2021-22 Onwards
Chairperson	Dean (Acad. Matters)	Date of Release	Version	

Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

M. Tech. Scheme of Examination & Syllabus 2019

Electronics Engineering

I Semester

EEE3910	**PE I: Multirate Signal Processing**	L= 3	T = 0	P = 0	Credits = 3

Evaluation Scheme	MSEs *	TA	ESE	Total	ESE Duration
	30	10	60	100	3 Hrs

MSEs* = Three MSEs of 15 Marks each will be conducted and marks of better 2 of these 3 MSEs will be considered for Continuous Assessment

Objective	Outcomes
• To acquaint the students with Multirate systems, Multirate Filter Banks and wavelet transform and application in signal processing	1. Graduates will understand and demonstrate multirate filter bank theory in signal processing area. 2. Graduates will able to understand and identify perfect reconstruction process. 3. Graduates will able to understand and identify difference between Fourier Transform, short time Fourier Transform and wavelet Transform 4. Graduates will understand knowledge of wavelet Transform and its applications.
Mapped Program Outcomes: a, d	

SN	Course Outcomes	Mapped PO						
		a	b	c	d	e	f	g
1	Graduates will understand and demonstrate multirate filter bank theory in signal processing area.	M			H			
2	Graduates will able to understand and identify perfect reconstruction process.	L			M			
3	Graduates will able to understand and identify difference between Fourier Transform, short time Fourier Transform and wavelet Transform	M			M			
4	Graduates will understand knowledge of wavelet Transform and its applications.	H						

Unit I

Basic multi-rate operations, interconnection of building blocks, poly-phase representation, multistage implementation, applications of multi-rate systems, special filters and filter banks.

Unit II

Maximally decimated filter banks: Errors created in the QMF bank, alias free QMF system, power symmetric QMF banks, M-channel filter banks, poly-phase representation, perfect reconstruction systems, alias-free filter banks.

Unit III

Para-unitary Perfect Reconstruction Filter Banks: Lossless transfer matrices, filter bank properties induced by paraunitariness, two channel Paraunitary lattices, M-channel FIR Para-unitary QMF banks, transform coding. Short-time Fourier transform: trades of between traditional Fourier transform and STFT,STFT as a bank of filter , window selection, STFT verses Wavelet transform, STFT to wavelet conversion .

Unit IV

Continuous Time Wavelets, Definition of CWT, CWT as a correlation, Constant Q factor Filtering Interpretation and Time Frequency Resolution.CWT as an operator. Inverse CWT. Introduction to the discrete Wavelet transform and orthogonal wavelet decomposition.

Unit V

MRA, Orthogonal Wavelets, and their relationship to Filter Banks: Introduction, Formal Definition of an MRN, Construction of a General orthonormal MRN, Wavelet basis For the MRN. Digital Filtering Interpretation, Examples of orthonomal basis generating Wavelets, Interpreting orthonormal MRNs for discrete tine signals, DTWT for Image Compression, Audio Compression

Unit VI

Biomedical signal processing applications; Geophysical signal analysis applications, Efficient signal design and realization: wavelet based modulation and demodulation, Applications in mathematical approximation, Applications to the solution of some differential equations, Applications in computer graphics and computer vision.

Resources:

1. P.P. Vaidyanathan, "Multirate Systems and Filter Banks," Pearson Education.
2. Raghuveer M.Rao ,Ajit Bopardikar, Wavelet Transform; Introduction to theory and application, Pearson Education,2006
3. Digital Signal Processing, A Computer – Based approach, by Sanjit K. Mitra, Tata Mc Graw-Hill,1998,3rd edition.

		June 2019	1.00	Applicable for Sem 1 & 2 AY 2019-20 & Sem 3 & 4 AY 2021-22 Onwards
Chairperson	Dean (Acad. Matters)	Date of Release	Version	

Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

M. Tech. Scheme of Examination & Syllabus 2019

Electronics Engineering

I Semester

EE3911	**PE I: Low Power CMOS VLSI Design**	L= 3	T = 0	P = 0	Credits = 3

Evaluation Scheme	MSEs *	TA	ESE	Total	ESE Duration
	30	10	60	100	3 Hrs

MSEs* = Three MSEs of 15 Marks each will be conducted and marks of better 2 of these 3 MSEs will be considered for Continuous Assessment

Objective	Outcomes
• To acquaint students with principles of design , analysis , modelling and optimization of low power VLSI , as well as to promote an interest in VLSI design	1. Graduates will understand the concepts of sources of power dissipation and basics of CMOS Physics. 2. Graduates will understand the concepts of levels of abstraction and its power dissipation. 3. Graduates will understand the Power Optimization methods at Behavior, Logic and Circuit Level design. 4. Graduates will understand the challenges in deep submicron technology. 5. Graduates will understand the principles for low power designs, and have the capabilities to analyze power consumption and develop low power strategies for a given system.
Mapped Program Outcomes: a, b, d	

SN	Course Outcomes	Mapped PO						
		a	b	c	d	e	f	g
1	Graduates will understand the concepts of sources of power dissipation and basics of CMOS Physics.	M	L					
2	Graduates will understand the concepts of levels of abstraction and its power dissipation.	M	M					
3	Graduates will understand the Power Optimization methods at Behavior, Logic and Circuit Level design.	M	L		H			
4	Graduates will understand the challenges in deep submicron technology.	M	M		H			
5	Graduates will understand the principles for low power designs, and have the capabilities to analyze power consumption and develop low power strategies for a given system.	M	M		H			

Unit - I

Need for low power VLSI chips, Sources of power dissipation: Short circuit dissipation, dynamic dissipation, designing Techniques for low power. Physics of power dissipation in MOSFET devices, MOS Capacitance analysis, low power figure of merits, brief overview of low power VLSI design limits.

Unit - II

Probabilistic power analysis: random logic signals, probability and frequency, probabilistic power analysis techniques, signal entropy, Low power circuits: transistor and gate sizing, equivalent pin ordering, network reconstruction and reorganization, Glitching Power, special latches and flip-flops.

Unit - III

Behavioural, Logic and circuit level approaches. Algorithm level transforms. Circuit activity driven architectural transformations, voltage scaling, operation reduction and substitution, pre-computation, Logic: gate reorganization, signal gating, logic encoding, state machine encoding.

Unit - IV

Design style, Leakage current in Deep sub-micron transistors, device design issues, minimizing short channel effect. Low voltage design techniques using reverse Vgs. Steep sub threshold swing and multiple threshold voltages. Multiple threshold CMOS based on path critically, multiple supply voltages.

Unit - V

Low energy computing, Energy dissipation in transistor channel. Energy recovery circuit design, designs with reversible and partially reversible logic, energy recovery in adiabatic logic and SRAM core, Design of peripheral circuits – address decoder, level shifter and IO Buffer, supply clock generation.

Unit - VI

Introduction, sources of software power dissipation, power estimation and optimization. Co-design for low power**.**

Resources:

1. "Solid State Electronic Devices", 6th Edition, Ben Streetman, Sanjay Benerjee.
2. "Low-Power CMOS VLSI Circuit Design", Kaushik Roy, Sharat C. Prasad, 1st Edition, Wiley India, 2009
3. "Practical Low Power Digital VLSI Design", Gary K. Yeap, Kluwer Academic Publisher, 2002
4. "Low-Power CMOS Circuits-Technology, Logic Design and CAD Tools" Christian Piguet, 2006 by Taylor & Francis Group, LLC
5. "Energy Efficient Microprocessor Design", T. D. Burd and R. A. Brodersen, Boston: Springer, 2002.
6. "Low-Power Digital CMOS Design", A. Chandrakasan and R. Brodersen, Boston: Springer, 1995.
7. "Digital Integrated Circuits: A Design Perspective", 2nd ed., J. Rabaey, A. Chandrakasan, B. Nikolic.

		June 2019	1.00	Applicable for Sem 1 & 2 AY 2019-20 & Sem 3 & 4 AY 2021-22 Onwards
Chairperson	Dean (Acad. Matters)	Date of Release	Version	

Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

M. Tech. Scheme of Examination & Syllabus 2019

Electronics Engineering

I Semester

EE3912	PE I: Biomedical Instrumentation	L= 3	T = 0	P = 0	Credits = 3

Evaluation Scheme	MSEs *	TA	ESE	Total	ESE Duration
	30	10	60	100	3 Hrs

MSEs* = Three MSEs of 15 Marks each will be conducted and marks of better 2 of these 3 MSEs will be considered for Continuous Assessment

Objective	Outcome
• This course is intended for exposing the students to basics of biomedical instrumentation. • It also includes sections on microprocessors and signal acquisition systems as applied to medical instrumentation.	1. Graduate will be able to develop understanding of biology and physiology 2. Graduate will be able to make measurements on and interpret data from living systems 3. Graduate will be able apply knowledge of science and engineering to solve the problems at the interface of engineering and biology 4. Graduate will be able address the problems associated with the interaction between Instruments and living systems.
Mapped Program Outcomes: a, b, d	

SN	Outcome	a	b	c	d	e	f	g
1	Graduate will be able to develop understanding of biology and physiology				H			
2	Graduate will be able to make measurements on and interpret data from living systems		M					
3	Graduate will be able apply knowledge of science and engineering to solve the problems at the interface of engineering and biology	H	H					
4	Graduate will be able address the problems associated with the interaction between Instruments and living systems.		M		L			

UNIT I:

Introduction to Biomedical instrumentation, development of biomedical instrumentation, biometrics, Physiological system of body, problems encountered in measuring a living system.

UNIT II:

Basic transducer principle, active transducer, passive transducer, electrode theory, biopotential electrodes, biochemical transducers.

UNIT III:

The heart and cardiovascular system, characteristics of blood flow, blood pressure measurement, heart sound measurement. Principles of ultrasonic diagnosis, temperature measurement, electrocardiograph, plethysmography, pulmonary function measurement spirometry, pulmonary function analyzers, respiratory gas analyzers.

UNIT VI:

Generation of ionizing radiation, instrumentation for diagnostic X-ray, special technique, instrumentation for medical use of radioisotopes, radiation therapy, EMG.

UNIT V:

Patient care and monitoring, the elements of intensive care monitoring , diagnosis, calibration, reparability of patient monitoring equipment, instrumentation for monitoring patient, pacemakers, defibrillators.

UNIT VI:

Interfacing the computer with medical instrumentation and other equipments, electrical safety of medical equipment. Physiological effects of electrical current, shock hazards from electrical equipments, Methods of accident prevention.

Resources:

1. Biomedical Instrumentation & Measurement, By Leaslie Cromwell, Fred Weibell, Erich A Pfeiffer, 2nd Edition ,PHI
2. Handbook of Biomedical Instrumentation, R.S.Khandpur, 2nd Edition, TMH
3. Bioelectronic Measurement, Dean A Dmane, David Michaels,Jan 1983 edition, PHI
4. Medicine and Clinical Engineering, Jacobson and Webster, 2nd Edition, PHI
5. Introduction to Biomedical Equipment Design ,Carr and Brown, 4th Edition, John Wiley
6. Biomedical Digital Signal Processing, Tompkins, 1993 Edition, PHI

		June 2019	1.00	Applicable for Sem 1 & 2 AY 2019-20 & Sem 3 & 4 AY 2021-22 Onwards
Chairperson	Dean (Acad. Matters)	Date of Release	Version	

Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

M. Tech. Scheme of Examination & Syllabus 2019

Electronics Engineering

II Semester

EE3915	RF Circuit Design	L= 3	T = 0	P = 0	Credits = 3

Evaluation Scheme	MSEs *	TA	ESE	Total	ESE Duration
	30	10	60	100	3 Hrs

MSEs* = Three MSEs of 15 Marks each will be conducted and marks of better 2 of these 3 MSEs will be considered for Continuous Assessment

Objective	Outcomes
• To study RF component such as resonator, filter, transmission lines, etc • To learn design of RF amplifiers using transistors	1. Graduates will have an ability to demonstrate in- depth knowledge of general RF circuits, components and systems and an understanding of resonant circuits 2. Graduates will be able to understand and use Smith Chart for developing circuits in RF applications. 3. Graduates will be able to design impedance matching networks, passive RF filters and RF power amplifiers.
Mapped Program Outcomes: a, d	

Sr. No.	Course Outcomes	Mapped PO						
		a	b	c	d	e	f	g
1	Graduates will have an ability to demonstrate in- depth knowledge of general RF circuits, components and systems and an understanding of resonant circuits	H			L			
2	Graduates will be able to understand and use Smith Chart for developing circuits in RF applications.	M			H			
3	Graduates will be able to design impedance matching networks, passive RF filters and RF power amplifiers.				H			

Unit – I

Introduction, Importance of Radio frequency Design, RF Behaviour of Passive Components, Chip Components, Transmission Line Analysis, Equivalent Circuit Representation, Circuit Parameters for a Parallel Plate Transmission Line, Microstrip Transmission Line, Terminated Lossless Transmission Line, Special Termination Conditions, Sourced and Loaded Transmission Line.

Unit – II

The Smith Chart, From Reflection Coefficient to Load Impedance, Impedance Transformation, Admittance, Transformation, Parallel and Series Connections, Single- and Multiport Networks, Interconnecting Networks, Network Properties and Applications, Scattering Parameters.

Unit – III

An Overview of RF Filter Design, Basic Resonator and Filter Configurations, Special Filter Realizations, Filter Implementation, Coupled Filter.

Unit – IV

Matching and Biasing Networks: Impedance Matching Using Discrete Components, Microstrip Line Matching Networks, Amplifier Classes of Operation and Biasing Networks.

Unit – V

RF Transistor Amplifier Designs: Characteristics of Amplifiers, Amplifier Power Relations, Stability Considerations, Constant Gain, Noise Figure Circles, Constant VSWR Circles, Broadband, High-Power, and Multistage Amplifiers

Unit – VI

Oscillators, Basic Oscillator Model, High-Frequency Oscillator Configuration, Oscillators describing functions, Colpitt's oscillators Resonators, Tuned Oscillators, Negative resistance oscillators, Phase noise Basic Characteristics of Mixers. Non-linear based mixers, Quadratic mixers, Multiplier based mixers, Single balanced and doubles balanced mixers, sub sampling mixers.

Resources:

1. "RF Circuit Design – Theory and Applications", Reinhold Luduig and Pavel Bretchko, 2nd Edition, Pearson Education, 2000.
2. T.Lee, "Design of CMOS RF Integrated Circuits", Cambridge, 2004.
3. B.Razavi, "RF Microelectronics", Pearson Education, 1997.
4. B.Razavi, "Design of Analog CMOS Integrated Circuits", McGraw Hill, 2001

		June 2019	1.00	Applicable for Sem 1 & 2 AY 2019-20 & Sem 3 & 4 AY 2021-22 Onwards
Chairperson	Dean (Acad. Matters)	Date of Release	Version	

Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

M. Tech. Scheme of Examination & Syllabus 2019

Electronics Engineering

II Semester

EE3916	Lab : RF Circuit Design	L= 0	T = 0	P = 2	Credits = 1

Evaluation Scheme	Continuous Evaluation	ESE	Total	ESE Duration
	40	60	100	

Objective	Outcomes
• To study RF component such as resonator, filter, transmission lines, etc • To learn design of RF amplifiers using transistors	1. Graduates will able to Understand and use smith chart for developing circuits in RF applications 2. Graduates will be able to design impedance matching networks, passive RF filters and RF filters and RF power amplifiers 3. Graduate will be able to use CAD tools for RF circuit design
Mapped Program Outcomes: c, d, e, f	

SN	Course Outcomes	Mapped PO						
		a	b	c	d	e	f	g
1	Graduates will able to Understand and use smith chart for developing circuits in RF applications				H	H	H	
2	Graduates will be able to design impedance matching networks, passive RF filters and RF filters and RF power amplifiers				H	H	H	
3	Graduate will be able to use CAD tools for RF circuit design			M		H	H	

Sr. No	Name of Experiment		
1	To find impedances of different resonant circuits.	CO1[M], CO2[M]	CO3[S]
2	To find input impedance of a short circuited transmission line.	CO1[M], CO2[M]	CO3[S]
3	To determine input impedance of transmission line using smith chart.	CO1[M], CO2[M]	CO3[S]
4	Design of T- matched network.	CO3[S]	CO3[S]
5	Design of π- matched network.	CO3[S]	CO3[S]
6	Design of low pass filter and high pass filter.	CO3[S]	CO3[S]
7	Design of band pass filter and band reject filter.	CO3[S]	CO3[S]
8	Design of tapped capacitor and tapped inductor network.	CO3[S]	CO3[S]
9	Design of double tapped resonator network.	CO3[S]	CO3[S]
10	Design of high power amplifier as per the specifications.	CO3[S]	CO3[S]
11	Design of Low noise amplifier as per the specifications.	CO3[S]	CO3[S]
12	Design of Dual stage transistor amplifier.	CO3[S]	CO3[S]

		June 2019	1.00	Applicable for Sem 1 & 2 AY 2019-20 & Sem 3 & 4 AY 2021-22 Onwards
Chairperson	Dean (Acad. Matters)	Date of Release	Version	

Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

M. Tech. Scheme of Examination & Syllabus 2019

Electronics Engineering

II Semester

EE3917	Artificial Intelligence	L= 3	T = 0	P = 0	Credits = 3

Evaluation Scheme	MSEs *	TA	ESE	Total	ESE Duration
	30	10	60	100	3 Hrs

MSEs* = Three MSEs of 15 Marks each will be conducted and marks of better 2 of these 3 MSEs will be considered for Continuous Assessment

Objective	Outcomes
1. To study the fundamental concepts in Artificial Intelligence, its applications, techniques, related fields and different types of AI agents. 2. To learn various AI search algorithms (uninformed, informed, heuristic, constraint satisfaction) 3. To understand the fundamentals of different knowledge representation approaches. 4. To comprehend various nonmonotonic reasoning techniques and its applications and To know the learning methods and expert system fundamentals.	1. Relate and apply AI fundamentals or AI agents for a given AI and Non-AI problems. 2. Explain and solve different real time problem using informed and/or uninformed searching techniques. 3. Choose and apply appropriate knowledge representation approach for a given Problem Domain. 4. Demonstrate the working knowledge of reasoning in the presence of incomplete and/or uncertain information and analyze and compare learning approaches and recall AI basics for expert system

Unit – I

Introduction to AI: Definition of AI, early work in AI, the importance of AI, AI and related fields, distributed AI, task domain of AI, Problems, problem spaces and searches: defining the problem on a state space search, Introduction to intelligent agents, generic architecture of intelligent agents.

Unit – II

Production systems and control strategies: depth first and breadth first search, back tracking, problem characteristics, issues in the design of search programs. Heuristic search techniques: generate and test hill climbing, best first search, problem reduction, constraint satisfaction, means-ends analysis.

Unit – III

Knowledge representation: issues, representation and mapping approaches, procedural Vsdeclarative knowledge, introduction to proposition logic, knowledge representation using predicate logic, unification and resolution algorithms.

Unit – IV

Representation of knowledge using rules, logic programming, forward backward reasoning, matching, control knowledge. Knowledge representation using semantics" nets, Prolog: Representation of Predicates, rules, and facts, recursion unification.

Unit – V

Introduction to non-monotonic reasoning, logics for non-montonic reasoning Statistical reasoning: probability and Bay's theorem, certainty factors and rule based system.

Unit – V

Learning: general learning model, overview of different forms of learning, learning decision trees, Artificial Neural Networks (Introduction). Expert Systems: Design & Development of Expert System, knowledge-based Systems, Rule Based Expert System, Expert System Shell, Application Areas of Expert System

TEXT BOOKS:

1. Artificial Intelligence by E. Richand K. Knight and Nair.

REFERENCE BOOKS:

1. Introduction to Artificial Intelligence and Expert System by D. W . Patterson, PHI.
2. Principles of Artificial Intelligence by N. J. Nilsson, Narosa.
3. Artificial Intelligence by George F. Lugar, 4 Edition , Pearson Education.
4. Expert Systems: Design and Development by John Durkin, Macmillan, USA

		June 2019	1.00	Applicable for Sem 1 & 2 AY 2019-20 & Sem 3 & 4 AY 2021-22 Onwards
Chairperson	Dean (Acad. Matters)	Date of Release	Version	

II Semester

EE3918	Digital Image Processing	L= 3	T = 0	P = 0	Credits = 3

Evaluation Scheme	MSEs *	TA	ESE	Total	ESE Duration
	30	10	60	100	3 Hrs

MSEs* = Three MSEs of 15 Marks each will be conducted and marks of better 2 of these 3 MSEs will be considered for Continuous Assessment

Objective	Outcomes
• Provide deeper knowledge of theoretically demanding methods of image data processing and of their applications.	Upon successfully completing the course, the student should: 1. Demonstrate the understanding of fundamentals of Digital image processing wrt to enhancement, filtering, segmentation, restoration & representation 2. Able to understand the mathematical implementation & interpretation of image transforms 3. be able to formulate solutions to general image processing problems 4. develop skill base necessary to further explore advanced topics of Digital Image Processing for research
Mapped Program Outcomes: a, c, d	

Sr. No.	Course Outcomes	Mapped PO						
		a	b	c	d	e	f	g
1	Demonstrate the understanding of fundamentals of Digital image processing wrt to enhancement, filtering, segmentation, restoration & representation	H		M	M			
2	Able to understand the mathematical implementation & interpretation of image transforms	H		M	M			
3	be able to formulate solutions to general image processing problems	H		M	M			
4	develop skill base necessary to further explore advanced topics of Digital Image Processing for research	M		M	M			

Unit I

An image model – sampling & quantization – basic relation between pixels: imaging geometry, Properties of 2-D Fourier transforms, FFT algorithm and other separable image transforms, Walsh transforms, Hadamard, Cosine, Haar, Slant Transforms, KL Transforms and their properties, Wavelets.

Unit II

Spatial domain methods, Frequency domain methods, Histogram Modification technique, Neighbourhood averaging, Median filtering, Low pass filtering, Averaging of Multiple Images, Image sharpening by differentiation, High pass Filtering,

Unit III

Degradation model for Continuous functions, Discrete Formulation, Diagonalization of Circulant and Block –Circulant Matrices, Effects of Diagonalization, Constrained and unconstrained Restorations Inverse filtering, Wiener Filter, Constrained least Square Restoration.

Unit IV

Fundamentals, Image compression models, error free compression, lossy compression, image compression standards Objective an subjective Fidelity Criteria, the encoding process, the Mapping, the Quantizer and the Coder, Contour Encoding, Run length Encoding, Image Encoding relative to a Fidelity Criterion, Differential Pulse Code Modulation, Transform Encoding.

Unit V

The detection of Discontinuities, Point Line and Edge Detections, Gradient Operators, Combined Detection, Image segmentation Thresholding. Region oriented segmentation Representation Schemes, Chain Codes, Polygon Approximation, Boundary Descriptors, Simple Descriptors, Shape Numbers, Fourier Descriptors Dilation and erosion, opening and closing hit-or-miss transformation, morphological algorithms, extension to gray scale images.

Unit VI

Color Image Processing: Color Fundamentals, color models, Pseudocolor image processing, Basics of full color image processing, Color transformations, Smoothing and sharpening, Color segmentation, Noise in color images,

Resources:

1. "Digital Image Processing", Gonzalez RC & Woods RE, 2nd Edition ,Addison Wesley Publishing Company,2002
2. "Fundamentals of Digital Image Processing" ,3rd Edition, Jain AK, Printice Hall of India, 1989
3. "Digital Image Processing", Pratt William K., 4th Edition,John Wiley & Sons 2000.

		June 2019	1.00	Applicable for Sem 1 & 2 AY 2019-20 & Sem 3 & 4 AY 2021-22 Onwards
Chairperson	Dean (Acad. Matters)	Date of Release	Version	

Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

M. Tech. Scheme of Examination & Syllabus 2019

Electronics Engineering

II Semester

EE3919	Lab: Digital Image Processing	L= 0	T = 0	P = 2	Credits = 1

Evaluation Scheme	Continuous Evaluation	ESE	Total	ESE Duration
	40	60	100	

Objective	Outcomes
Provide deeper knowledge of theoretically demanding methods of image data processing and of their applications.	1. Graduates will Understand digital image processing fundamentals: digitization, enhancement and restoration, encoding, segmentation 2. Graduates will be able to apply image processing techniques in both the spatial and frequency (Fourier) domain.
Mapped Program Outcomes: a, c, d, e, f	

SN.	Course Outcomes	Mapped PO						
		a	b	c	d	e	f	g
1	Graduates will Understand digital image processing fundamentals: digitization, enhancement and restoration, encoding, segmentation			M	M	H	H	
2	Graduates will be able to apply image processing techniques in both the spatial and frequency (Fourier) domain.	H			H	H	H	

Expt. No.	Name of Experiments
1.	Write a Matlab Code for Bit Plane Slicing of a given image.[CO-1(S)]
2.	To perform point processing of the given image.[CO-1(S),CO-2(M)]
3.	To perform histogram equalization on a gray scale image.[CO-1(S)]
4.	Perform spatial filtering using Median filter.[CO-1(S),CO-2(M)]
5.	To perform Fourier transform on an image.[CO-2,(S)]
6.	To perform edge detection using sobel and prewitt operation on an image.[CO-1(S),CO-2(W)]
7.	To perform morphological operations such as dilation and erosion.[CO-1(S),CO-2(W)]
8.	To perform Wavelet transform on a gray scale image.[CO-1(M)]
9.	To perform low pass and high pass filtering in frequency domain on a gray scale image.[CO-1(W),CO-2(S)]
10.	To perform gray level morphological operations on an image.[CO-1(S),CO-2(M)]

		June 2019	1.00	Applicable for Sem 1 & 2 AY 2019-20 & Sem 3 & 4 AY 2021-22 Onwards
Chairperson	Dean (Acad. Matters)	Date of Release	Version	

Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

M. Tech. Scheme of Examination & Syllabus 2019

Electronics Engineering

II Semester

EE3920	PE II: Wireless Communication	L= 3	T = 0	P = 0	Credits = 3

Evaluation Scheme	MSEs *	TA	ESE	Total	ESE Duration
	30	10	60	100	3 Hrs

MSEs* = Three MSEs of 15 Marks each will be conducted and marks of better 2 of these 3 MSEs will be considered for Continuous Assessment

Objective	Outcomes
• The course aims to give basic knowledge of different mobile / wireless communication systems	1. Will be able to study different standard & generation in mobile communication system 2. Will be able to understand the need and different methods for enhancing the quality of communication. 3. Will be able to gain technical knowledge of current practice in wireless systems. 4. Will be able to analyse & solve the problem to improve quality of communication.
Mapped Program Outcomes: a, d	

SN	Course Outcomes	Mapped PO						
		a	b	c	d	e	f	g
1	Will be able to study different standard & generation in mobile communication system	M						
2	Will be able to understand the need and different methods for enhancing the quality of communication.	M			M			
3	Will be able to gain technical knowledge of current practice in wireless systems.	H						
4	Will be able to analyze & solve the problem to improve quality of communication.				M			

Unit - I

Mobile Radio Propagation: Large& Small Scale Path Loss & Fading: Introduction to Radio Wave Propagation, Reflection, Diffraction, Scattering Practical Link Budget Design Using Path Loss Models, Signal Penetration into Buildings, Ray Tracing & Site Specific Modeling. Small Scale Multipath Propagation, Small Scale Multipath Measurements, Parameters of Mobile Multipath Channels, Types of Small Scale Fading, Rayleigh & Rician Distribution

Unit - II

Equalization&Diversity: Fundamentals of equalization, classification of equalizer: linear & non-linear equalizer, Diversity Technique: Derivation of selection diversity improvement, Derivation of maximal ratio combining improvement, Space diversity, Polarization Diversity, time diversity & frequency diversity RAKE receivers

Unit - III

Multiplexing & multiple access techniques for wireless communication: FDMA, TDMA, FHMA, CDMA, SDMA, Orthogonal Frequency Division Multiplexing (OFDM)**,** Packet radio protocol: Pure & Slotted ALOHA, CSMA, PRMA, capacity of cellular system

Unit - IV

Wireless Systems and Standards: GSM-GSM services and features, Architecture, Radio Subsystem, GSM channel types, Frame structure and signal processing in GSM, CDMA-Forward CDMA channel, Reverse CDMA channel

Unit – V

Modern Wireless Communication System: 2G, 3G wireless network, Wireless local loop, & LMDS, Wireless Local Area networks (WLANs), Bluetooth & Personal Area Networks (PANs)

Unit – VI

Advanced wireless communication: 4G features and challenges,QoS-enabled MAC Protocol, Class-based QoS over Air Interface in 4G,Wi-Fi,Wi-Max,wirelessRouter,features of wireless routers, Difference between wireless & Wi-Fi,Zigbee

Resources:

1. "Advanced Wireless Communication"-- Savo G. GlisicJohn Wiley & Sons, 13-Dec-2005
2. "Wireless Communication- Principle and Practices" – Rapaport, 2nd Edition,Pearson Education , 2001
3. "Mobile Communications – Design fundamentals" ,William C. Y. Lee,2nd Edition, John Wiley Publication, 1993
4. "Mobile Cellular Communication", W .C .Y. Lee ,2nd Edition, McGraw Hill, 2006
5. "The Mobile Radio Propagation channel", J.D. Parson ,2nd edition, John Willey,2010

		June 2019	1.00	Applicable for Sem 1 & 2 AY 2019-20 & Sem 3 & 4 AY 2021-22 Onwards
Chairperson	Dean (Acad. Matters)	Date of Release	Version	

II Semester

EE3921	PE II: VLSI Signal Processing	L= 3	T = 0	P = 0	Credits = 3

Evaluation Scheme	MSEs *	TA	ESE	Total	ESE Duration
	30	10	60	100	3 Hrs

MSEs* = Three MSEs of 15 Marks each will be conducted and marks of better 2 of these 3 MSEs will be considered for Continuous Assessment

Objective	Outcomes
• The students shall gain proficiency in subjects like the basic design of theory involved in VLSI for signal processing and communication systems , various software tools related to VLSI, Signal Processing and Communication Systems.	1. Graduates will understand and able to design architectures for DSP algorithms. 2. Graduates will understand and able to apply the optimisation concept in terms of area, speed and power on DSP systems. 3. Graduates will understand and able to optimize DSP arithmetic.
Mapped Program Outcomes: a, d	

SN	Course Outcomes	Mapped PO						
		a	b	c	d	e	f	g
1	Graduates will understand and able to design architectures for DSP algorithms.	H			M			
2	Graduates will understand and able to apply the optimisation concept in terms of area, speed and power on DSP systems.	M			M			
3	Graduates will understand and able to optimize DSP arithmetic.	M			H			

UNIT I:

Introduction to DSP systems, Data flow and Dependence graphs - critical path, Loop bound, iteration bound, longest path matrix algorithm, Pipelining and Parallel processing of FIR filters, parallel processing, Pipelining and parallel processing for low power.

UNIT II:

Retiming – definitions and properties, solving systems of inequalities, Retiming techniques, Unfolding – an algorithm for unfolding, properties of unfolding, sample period reduction and parallel processing application

UNIT III:

Folding: folding transformation, Register Minimization Techniques, Register minimization in folded architectures folding of multirate systems. Systolic Architecture Design: Introduction, Systolic Array Design Methodology, FIR systolic Arrays, Selection of scheduling vector, Matrix Multiplication and 2D systolic array Design, Systolic design for space representations containing Delays.

UNIT IV:

Fast convolution – Cook-Toom algorithm, modified Cook-Toom algorithm, Winograd algorithm, iterated and cyclic convolution, Algorithmic strength reduction in filters and transforms – 2-parallel FIR filter, 2-parallel fast FIR filter, rank-order filters, Odd-Even merge-sort architecture, parallel rank order filters.

UNIT V:

Bit-level arithmetic architectures – parallel multipliers with sign extension, parallel carry-ripple and carry-save multipliers, Design of Lyon's bit-serial multipliers using Horner's rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner's rule for precision improvement, Distributed Arithmetic.

Unit VI:

Redundant number representation, carry free radix-2 addition and subtraction, hybrid radix 4 addition,radix2 hybrid redundant multiplication architectures, data format conversion, redundant to non redundant converter, Numerical strength reduction – sub-expression elimination, multiple constant multiplication, iterative matching.

Resources:

1. Keshab K. Parhi, "VLSI Digital Signal Processing Systems, Design and implementation ", Wiley, Interscience, 2007.
2. U. Meyer – Baese, " Digital Signal Processing with Field Programmable Gate Arrays", Springer, Second Edition, 2004

Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

M. Tech. Scheme of Examination & Syllabus 2019

Electronics Engineering

II Semester

EE3922	PE II: Verification & Testing of VLSI Circuits	L= 3	T = 0	P = 0	Credits = 3

Evaluation Scheme	MSEs *	TA	ESE	Total	ESE Duration
	30	10	60	100	3 Hrs

MSEs* = Three MSEs of 15 Marks each will be conducted and marks of better 2 of these 3 MSEs will be considered for Continuous Assessment

Objective	Outcomes
• To gain a knowledge from the area of applying diagnostic principles in the design of modern Electronic systems.	1. Students develop an understanding of VLSI design verification and testing issues. 2. Students learn how to generate test patterns for faults in a system and how to design a system for testability. 3. Ability to model different faults and carry out fault simulation in digital circuits. 4. Ability to know about importance of testing and its types in VLSI circuits.
Mapped Program Outcomes: a, d	

SN	Course Outcomes	Mapped PO						
		a	b	c	d	e	f	g
1	Students develop an understanding of VLSI design verification and testing issues.	M						
2	Students learn how to generate test patterns for faults in a system and how to design a system for testability.	M			H			
3	Ability to model different faults and carry out fault simulation in digital circuits.				H			
4	Ability to know about importance of testing and its types in VLSI circuits.				M			

Unit I : Overview Of Testing**:** Design Process, Verification, Faults & Their Detection, Test Pattern Generation, Fault Coverage, Types Of Tests, Test Application, Testing Economics. Defects, Failures, and Faults: Physical Defects, Failures Modes, Faults, Fault Equivalence and Dominance, Fault Collapsing

Unit II : Design Representation: Graphical representation, Graphs, Binary Decision diagrams, Netlists, VLSI Design Flow: CAD tools, Design Methodologies, Semicustom Design

Unit III : Simulation: Logic Simulation, Approaches to Simulation, Fault Simulation & Their Results. Automatic Test Pattern Generation: D-Algorithm, Critical Path Extensions to D-Algorithm PODEM, FAN

Unit IV : Ad Hoc Techniques, Scan–Path Design, Test pattern generation, Test Pattern Application, Scan architectures, multiple scan chains, Partial Scan Testing

Unit V : Boundary-Scan Testing: Boundary Scans Architecture, Test Access Port, Registers, Tap Controller, Modes of Operation. Built In Self Test: Pseudorandom Test Pattern Generation, Response Compaction, BIST Architectures

Unit VI : Memory Testing: Types of Memory Testing, Functional Testing Schemes, Testing FPGAs and Microprocessors: Testability Of FPGAs, Testing RAM- Based FPGAs, Testing Microprocessors, Synthesis For Testability.

Resources:

1. "Principles of Testing Electronic Systems", 2nd edition Samiha Mourad, Yervant Zorian
2. "Essentials of Electronic Testing for Digital, Memory, and Mixed-Signal VLSI Circuits",Michael L. Bushnell and Vishwani D. Agrawal, B.S.Publications, 2000
3. "Digital Systems Testing and Testable Design" ,Miron Abramovici, Melvin Breuer and Arthur Friedman, IEEE press,
4. "A Guide to VHDL" by Stanley Mazor,2nd Edition, Kluwer Academic Press, 2007
5. "HDL Chip Design" by Douglas Smith, 3rd Edition, Doone Publications, 2008
6. "Rapid Prototyping of Digital Systems", by J. O. Hamblen and M. Furman, Kluwer Academic Publishers.2001

		June 2019	1.00	Applicable for Sem 1 & 2 AY 2019-20 & Sem 3 & 4 AY 2021-22 Onwards
Chairperson	Dean (Acad. Matters)	Date of Release	Version	

Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

M. Tech. Scheme of Examination & Syllabus 2019

Electronics Engineering

II Semester

EE3923	PE III: Wireless Sensor	L= 3	T = 0	P = 0	Credits = 3

Evaluation Scheme	MSEs *	TA	ESE	Total	ESE Duration
	30	10	60	100	3 Hrs

MSEs* = Three MSEs of 15 Marks each will be conducted and marks of better 2 of these 3 MSEs will be considered for Continuous Assessment

Objective	Outcomes
• The objective of the course is to give the student good understanding of programming embedded wireless systems where the requirements on low energy dissipation is hard and the real time requirements and the limited resources of memory and processing capability makes it necessary for optimised the implementation of the software functions.	1. Graduates will able to study basic wireless sensor technology and different types of sensor protocol. 2. Graduates will able to understand different routing challenges and design issue in wireless sensor 3. Graduates will able to understand wireless sensor network management and traffic management issues
Mapped Program Outcomes: a, d	

SN	Outcome	a	b	c	d	e	f	g
1	Graduates will able to study basic wireless sensor technology and different types of sensor protocol	M						
2	Graduates will able to understand different routing challenges and design issue in wireless sensor				H			
3	Graduates will able to understand wireless sensor network management and traffic management issues				H			

Unit I

Introduction and Overview of Wireless Sensor Networks, Commercial and Scientific Applications of Wireless Sensor Networks, Basic Wireless Sensor Technology, Sensor Taxonomy, wireless network environment, wireless network trends.

Unit II

Radio technology primer, Available wireless technologies, Wireless Sensors Networks Protocols, Physical Layer, Fundamentals of Medium Access Control Protocols for Wireless Sensor Networks, MAC protocols for WSN, Case Study, IEEE 802.15 4LR WPAN, Standard case study.

Unit III

Sensors Network Protocols, Data dissemination and gathering, Routing Challenges and design issues in wireless sensor network, Routing strategies in WSN.

Unit IV

Protocols, Transport Control Protocols for Wireless Sensors Networks, Traditional transport control protocol, and transport protocol design issues, examples of existing transport control protocol, performance of TCP.

Unit V

Middleware for Sensor Networks, WSN middleware principles, Middleware architecture, existing middleware.

Unit VI

Network Management for Wireless Sensor Networks, Requirements, Design issues, Examples of management Architecture, Performance and Traffic Management Issues.

Resources:

1. "Wireless Sensor Networks: Technology, Protocols, and Applications", Kazem Sohraby, Daniel Minoli, Taieb Znati, WIey Interscience Publication, 2007
2. "Computer Networks" ,Andrew Tanenbaum, 4th ed, Pearson Education,2007

		June 2019	1.00	Applicable for Sem 1 & 2 AY 2019-20 & Sem 3 & 4 AY 2021-22 Onwards
Chairperson	Dean (Acad. Matters)	Date of Release	Version	

Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

M. Tech. Scheme of Examination & Syllabus 2019

Electronics Engineering

II Semester

EE3924	PE III: Mixed Signal VLSI Design	L= 3	T = 0	P = 0	Credits = 3

Evaluation Scheme	MSEs *	TA	ESE	Total	ESE Duration
	30	10	60	100	3 Hrs

MSEs* = Three MSEs of 15 Marks each will be conducted and marks of better 2 of these 3 MSEs will be considered for Continuous Assessment

Objective	Outcomes
• To study different types of mixed signal VLSI design and their procedures with methods applied in different stages of design.	1. Graduates will understand the challenges in modern VLSI Design and learn the skills of overcoming these problems when two opposing signal domains are integrated onto a single chip. 2. Graduates will understand the basic building blocks of Data converter systems. 3. Graduates will understand the review of fundamentals of semiconductor components. 4. Graduates will understand the basics of different data converters that are used in different mixed signal systems. 5. Graduates will understand the physical layout representation and the alternative layout solutions of data converter systems. 6. Graduates will understand the design of various CMOS Op-Amps used in mixed signal system. 7. Graduates will understand the design of various analog filers used in data converter systems.
Mapped Program Outcomes: a, b, d	

SN	Course Outcomes	Mapped PO						
		a	b	c	d	e	f	g
1	Graduates will understand the challenges in modern VLSI Design and learn the skills of overcoming these problems when two opposing signal domains are integrated onto a single chip.	M	M		H			
2	Graduates will understand the basic building blocks of Data converter systems.	M	M		H			
3	Graduates will understand the review of fundamentals of semiconductor components.	H	M		M			
4	Graduates will understand the basics of different data converters that are used in different Mixed signal systems.	M	M		H			
5	Graduates will understand the physical layout representation and the alternative layout solutions of data converter systems.	L	M		M			
6	Graduates will understand the design of various CMOS Op-Amps used in Mixed signal system.	M	L		M			
7	Graduates will understand the design of various analog filers used in data converter systems.	M	M		H			

Unit - I

Introduction to Mixed Signal VLSI System, Signal and Filters, digital comb filter, the z-plane, simple digital filters, Sampling and Aliasing: Impulse Sampling, Sample and Hold. Quantization noise. Spectral density of quantization noise.

Unit - II

Data Converter SNR: Effective number of bits Clock jitter, Using averaging to improve SNR, Decimating filters for ADCs, Interpolating filters for DACs, Band pass and High pass Sync filters, Using feedback to improve SNR.

Unit - III

Sub-Micron CMOS circuit design : Process flow, capacitors and resistors, MOSFET Switch, Delay and Adder elements, Analog circuits – MOSFET Biasing, Op-Amp design, Circuit noise.

Unit - IV

Implementing Data converters: Current mode and voltage mode R-2R DAC, Using Op-Amps in data converters, Implementing ADCs, Cyclic ADC, Introduction to Sigma Delta ADC and Line Drivers.

Unit - V

Integrator Based CMOS Filters: Integrator Building Blocks, Low pass and Active R-C filters, MOSFET-C integrators,gm-C Integrators, Discrete time integrators

Unit - VI

Bilinear and Bi-quadratic transfer functions – Active R-C Transconductor-C and Switched Capacitor implementations both transfer functions, Canonic form of a digital filter.

Resources:

1. "CMOS – Mixed signal circuit design, layout and simulation",R.Jacob Baker, "2nd Edition
   a. IEEE Press and Wiley Interscience, 2002.
2. "CMOS Circuit Design, Layout, and Simulation", Third Edition, R. Jacob Baker
3. "Design of Analog CMOS Integrated circuits", B. Razavi, 1st Edition, McGraw Hill, 2001.
4. "CMOS Analog Circuit Design", P.E. Allen and D.R. Holberg, 2nd Edition, Oxford University Press, 2002.

		June 2019	1.00	Applicable for Sem 1 & 2 AY 2019-20 & Sem 3 & 4 AY 2021-22 Onwards
Chairperson	Dean (Acad. Matters)	Date of Release	Version	

Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

M. Tech. Scheme of Examination & Syllabus 2019

Electronics Engineering

II Semester

EE3925	PE III: Cryptography & Network Security	L= 3	T = 0	P = 0	Credits = 3

Evaluation Scheme	MSEs *	TA	ESE	Total	ESE Duration
	30	10	60	100	3 Hrs

MSEs* = Three MSEs of 15 Marks each will be conducted and marks of better 2 of these 3 MSEs will be considered for Continuous Assessment

Objective	Outcome
• This course will introduce cryptography theories, algorithms, and systems. It will also consider necessary approaches and techniques to build protection mechanisms in order to secure computer networks.	The students who succeeded in this course; 1. Learn threats to computer networks and protection mechanisms and methods need to thwart these threats. 2. Understand the theory of fundamental cryptography, encryption, and decryption algorithms, 3. Build simple cryptosystems by applying encryption algorithms, 4. Comprehend secure identity management (authentication), message authentication, and digital signature techniques.
Mapped Program Outcomes: a, b, c, d, e, f	

SN	Course Outcomes	Mapped PO						
		a	b	c	d	e	f	g
1	Learn threats to computer networks and protection mechanisms and methods need to thwart these threats.	M	M	M	S	M		
2	Understand the theory of fundamental cryptography, encryption, and decryption algorithms,		M		M	H		
3	Build simple cryptosystems by applying encryption algorithms,			M	M	M	S	
4	Comprehend secure identity management (authentication), message authentication, and digital signature techniques.					M		

UNIT I:

Security Goals, Cryptographic Attacks, Services & Mechanisms, Techniques, Mathematics of Cryptography, Traditional Symmetric Key Ciphers.

Unit II:

Mathematics of Symmetric Key Cryptography , Algebraic Structures, GF(2n) Fields, Introduction to Modern Key Ciphers , Modern Block Ciphers, Modern Stream Ciphers.

Unit III:

Data Encryption Standard (DES) , DES Structure, DES Analysis, Security of DES, Multiple DES, Examples of Block Cipers Influenced by DES, Advanced Encryption Standard, Transformation , Key Expansion , AES Ciphers, Analysis of AES.

UNIT IV:

Mathematics of Asymmetric-Key Cryptography , Primes , Primality Testing, Factorization, Chinese's Remainder Theorem, Quadratic Congruence, Exponentiation & Logarithmic.

UNIT V:

Asymmetric – Key Cryptography , RSA Cryptography , Rabin Cryptosystem, ElGamal Cryptosystem, Elliptic Curve Cryptosystem

Unit VI:

Message Authentication and Hash Functions, Digital Signatures and Key Management. IP Security: Architecture, Authentication header, Encapsulating security payloads, Web Security: Secure socket layer and transport layer security, secure electronic transaction (SET). System Security: Intruders, Viruses and related threads, firewall design principals, trusted systems.

Resources:

1. Cryptography and Network Security, William Stallings. (Second Edition) Pearson Education Asia .
2. Cryptography and Network Security, Behrouz A. Forouzan (Second Edition) Mcgraw-Hill .

		June 2019	1.00	Applicable for Sem 1 & 2 AY 2019-20 & Sem 3 & 4 AY 2021-22 Onwards
Chairperson	Dean (Acad. Matters)	Date of Release	Version	

Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

M. Tech. Scheme of Examination & Syllabus 2019

Electronics Engineering

II Semester

EE3926	PE IV: Adaptive Signal Processing	L= 3	T = 0	P = 0	Credits = 3

Evaluation Scheme	MSEs *	TA	ESE	Total	ESE Duration
	30	10	60	100	3 Hrs

MSEs* = Three MSEs of 15 Marks each will be conducted and marks of better 2 of these 3 MSEs will be considered for Continuous Assessment

Objective	Outcomes
• The primary objective of this course is to develop the ideas of optimality and adaptation in signal processing, design, analysis, and implementation of digital signal processing systems	1. Graduates will understand and analyze knowledge of adaptive filters 2. Graduates will able to identify and analyze statistical analysis. 3. Graduates will understand parametric signal analysis
Mapped Program Outcomes: a, d	

SN	Course Outcomes	Mapped PO						
		a	b	c	d	e	f	g
1	Graduates will understand and analyze knowledge of adaptive filters	M			H			
2	Graduates will able to identify and analyze statistical analysis.	M			H			
3	Graduates will understand parametric signal analysis	M						

Unit – I

The Filtering Problem, Adaptive Filters, Linear Filter Structures, Approaches to the Development of Linear Adaptive Filtering Algorithms, Real and Complex Forms of Adaptive Filters, Nonlinear Adaptive Filters, Some Historical Notes, Partial Characterization of a Discrete-Time Stochastic Process, Mean Ergodic Theorem, Correlation Matrix, Correlation Matrix of Sine Wave Plus Noise, Stochastic Models, Wold Decomposition, Asymptotic Stationarity of an Autoregressive Process, Yule-Walker Equations, Computer Experiment: Autoregressive Process of Order2, Selecting the Model Order, Complex Gaussian Processes

Unit – II

Power Spectral Density, Properties of Power Spectral Density, Transmission of a Stationary Process Through a Linear Filter, Cramer Spectral Representation for a Stationary Process, Power Spectrum Estimation,Other Statistical Characteristics of a Stochastic Process, Polyspectra,Spectral-Correlation Density, The Eigenvalue Problem, Properties of Eigenvalues and Eigenvectors, Low-Rank Modeling, Eigenfilters, Eigenvalue Computations

Unit – II

Linear Optimum Filtering: Problem Statement, Principle of Orthogonality,Minimum Mean Squared Error, Wiener-Hopf Equations, Error-Performance Surface, Numerical Example, Channel Equalization, Linearly Constrained Minimum Variance Filter, Generalized Sidelobe Cancelers, Forward Linear Predication, Backward Linear Predication, Levinson-Durbin Algorithm, Properties of Prediction-Error Filters, Schur-Cohn Test, Autoregressive Modeling of a Stationary Stochastic Process, Cholesky Factorization, Lattice Predictors, Joint-Process Estimation, Block Estimation, Recursive Minimum Mean-Square Estimation For Scalar Random Variables, The Innovation of the State using the Innovations Process, Filtering, Initial Conditions, Summary of the Kalman Filter, The Extended Kalman Filter

Unit – IV

Overview of the structure and operation of the Least-Mean-Square Algorithm,Stability and Performance Analysis of the LMS Algorithm, Computer Experiment of Adaptive Prediction, Computer Experiment of Adaptive Equalization, Computer Experiment on Minimum-Variance Distortionless Response Beamformer, Directionality of Convergence of the LMS Algorithm for Non-White Inputs, Robustness of the LMS Algorithm, Normalized LMS Algorithm

Unit – V

Block Adaptive Filters, Fast LMS Algorithm, Unconstrained Frequency- Domain Adaptive Filtering, Self-Orthogonalizing Adaptive Filters,Computer Experiment on Adaptive Equalization, Classification of Adaptive Filtering Algorithms,

Unit – VI

Statement of the Linear Least-Squares Estimation Problem, Data Windowing, Principle of Orthogonality , Minimum Sum of Error Squares,Normal Equations and Linear Least Squares Filters, Time-Averaged Correlation Matrix, Reformulation of the Normal Equations in Terms of Data Matrices, Properties of Least- Squares Estimates, Parametric Spectrum estimation, Singular Value Decomposition, Pseudoinverse, Interpretation of Singular Values and Singular Vectors, Minimum Norm Solution to the Linear Least-Squares Problem, Normalized LMS Algorithm Viewed as the Minimum-Norm Solution to an Underdetermined Least Squares Estimation Problem,

Resources:

1. "Adaptive Filter Theory ", Simon Haykin, 4th Edition, Prentice Hall of India, 2001
2. "Theory and Design of Adaptive Filters", Michael G Larimore, C Richard Johnson,John R Treichler, Prentice Hall of India, 1987.

		June 2019	1.00	Applicable for Sem 1 & 2 AY 2019-20 & Sem 3 & 4 AY 2021-22 Onwards
Chairperson	Dean (Acad. Matters)	Date of Release	Version	

Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

M. Tech. Scheme of Examination & Syllabus 2019

Electronics Engineering

II Semester

EE3927	PE IV: Embedded System & RTOS	L= 3	T = 0	P = 0	Credits = 3

Evaluation Scheme	MSEs *	TA	ESE	Total	ESE Duration
	30	10	60	100	3 Hrs

MSEs* = Three MSEs of 15 Marks each will be conducted and marks of better 2 of these 3 MSEs will be considered for Continuous Assessment

Objective	Outcomes
• To introduce students to the embedded systems, its hardware and software, real time operating systems, inter-task communication and an exemplary case of RTOS.	1. Students will be able to understand and learn the concepts, architecture, programming, addressing modes for various embedded systems 2. Students will be acquainted with the new concepts related to design of embedded systems, introspect themselves for applying their previous knowledge for various parameters, especially, selection of operating systems, processors, controllers, memory, IO devices, etc 3. Students will be able to establish link for hardware-software interaction for embedded systems, develop build process for signal / data processing through related software and hardware set up 4. Students will be acquainted with task scheduling, interrupt mechanisms and various managements related to embedded real time operating systems, and will be able to discuss / deliver presentation on contemporary issues related to system on chip and system on slice
Mapped Program Outcomes: a, c, d	

SN	Course Outcomes	Mapped PO						
		a	b	c	d	e	f	g
1	Students will be able to understand and learn the concepts, architecture, programming, addressing modes for various embedded systems	H						
2	Students will be acquainted with the new concepts related to design of embedded systems, introspect themselves for applying their previous knowledge for various parameters, especially, selection of operating systems, processors, controllers, memory, IO devices, etc	H			H			
3	Students will be able to establish link for hardware-software interaction for embedded systems, develop build process for signal / data processing through related software and hardware set up	M		H	H			
4	Students will be acquainted with task scheduling, interrupt mechanisms and various managements related to embedded real time operating systems, and will be able to discuss / deliver presentation on contemporary issues related to system on chip and system on slice				M			

Unit I: Introduction to embedded systems, basic concepts, application areas and categories of embedded systems: Stand alone Embedded systems, Real Time systems, Requirements, challenges Recent trends and applications of Embedded systems.

Unit II: New trends in hardware platforms for Embedded system design, Processor selection criteria in Embedded system design, Embedded system design with microprocessors, microcontrollers, and DSP processor.

Unit III: Issues involved in choosing appropriate development platforms and tools for design of Embedded systems, development environments, operating systems, task scheduling, non real and real time operating systems

Unit IV: Need for communication Interfaces, RS 232 communication parameters, connector configurations, UART, serial communications, Ethernet, IEEE 802.11, Bluetooth system specifications

Unit V: Embedded Real Time Operating systems, concepts, architecture of Kernel, tasks, task scheduler, interrupt service routines, semaphores, Mutex, Mailboxes, Message queue management function calls, event register management function calls, signals and timer management function calls, memory management, priority inversion problems in design of Embedded Real Time Operating systems.

Unit VI: Commonalities of Embedded Real Time Operating systems, Embedded operating systems –LINUX, Real Time Operating systems – RTLINUX, Concept of system on chip and system on Slice.

Resources:

1. 'Embedded / Real Time Systems – Concepts, design and programming' Dr.K.V.K.K.Prasad, (DreamTech Press), Reprint Edition, 2006
2. 'Designing Embedded Hardware', John Catsoulis, 2nd Edition, O'reilly Publication, 2005
3. 'Programming for Embedded systems – Cracking the code' DreamTech Software Team, WileyPublishing Inc, 2006
4. "An Embedded Software Primer", David E. Simon, 1st Edition, Pearson Education,1999
5. "Embedded System Design", Frank Vahid, Tony Givargis, John Wiley & Sons, Inc,2002
6. "Building Embedded Linux Systems", Karim Yaghmour,2nd Edition, O'reilly,2008
7. "Programming Embedded Systems", Michael Barr, 2nd Edition, O'reilly,2006
8. "Real-time systems & software", Alan C. Shaw,3rd Edition, John Wiley & sons, Inc.2001
9. "Computers as Components", Wayne Wolf, 1st Edition, Harcourt India Pvt. Ltd., 2002

		June 2019	1.00	Applicable for Sem 1 & 2 AY 2019-20 & Sem 3 & 4 AY 2021-22 Onwards
Chairperson	Dean (Acad. Matters)	Date of Release	Version	

Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

M. Tech. Scheme of Examination & Syllabus 2019

Electronics Engineering

II Semester

EE3928	PE IV: Advanced Computer Architecture	L= 3	T = 0	P = 0	Credits = 3

Evaluation Scheme	MSEs *	TA	ESE	Total	ESE Duration
	30	10	60	100	3 Hrs

MSEs* = Three MSEs of 15 Marks each will be conducted and marks of better 2 of these 3 MSEs will be considered for Continuous Assessment

Objective	Outcome
• The objective of this course is to introduce the fundamental techniques on which high-performance computing is based, to develop the foundations for analyzing the benefits of design options in computer architecture, and to give some experience of the application of these techniques.	1. Understand and evaluate the hardware components of advanced architectures Understand and analyze architectures performance and select among different ones for particular use scenarios 2. Understand and analyze the most important parallel architectures in order to distinguish their main difference. 3. Understand the levels of software and hardware comprising the Instruction Set Architecture (ISA) of a computer 4. Make design decisions based on performance data
Mapped Program Outcomes: a, c, d	

SN	Course Outcomes	Mapped PO						
		a	b	c	d	e	f	g
1	Understand and evaluate the hardware components of advanced architectures Understand and analyze architectures performance and select among different ones for particular use scenarios	M						
2	Understand and analyze the most important parallel architectures in order to distinguish their main difference.	M			M			
3	Understand the levels of software and hardware comprising the Instruction Set Architecture (ISA) of a computer	M		M	M			
4	Make design decisions based on performance data				M			

Unit – I

The state of computing, Classification of parallel computers, Multiprocessors and multicomputer, Multivector and SIMD computers. Conditions of parallelism, Data and resource Dependences, Hardware and software parallelism, Program partitioning and scheduling, Grain Size and latency, Program flow mechanisms, Control flow versus data flow, Data flow Architecture, Demand driven mechanisms, Comparisons of flow mechanisms

Unit – II

Network properties and routing, Static interconnection Networks, Dynamic interconnection Networks, Multiprocessor system Interconnects, Hierarchical bus systems, Crossbar switch and multiport memory, Multistage and combining network.

Unit – III

Advanced processor technology, Instruction-set Architectures, CISC Scalar Processors,RISC Scalar Processors, Superscalar Processors, VLIW Architectures, Vector and Symbolic processors

Unit - IV

Linear pipeline processor, nonlinear pipeline processor, Instruction pipeline Design, Mechanisms for instruction pipelining, Dynamic instruction scheduling, Branch Handling techniques, branch prediction, Arithmetic Pipeline Design, Computer arithmetic principles, Static Arithmetic pipeline, Multifunctional arithmetic pipelines

Unit – V

Cache basics & cache performance, reducing miss rate and miss penalty, multilevel cache hierarchies, main memory organizations, design of memory hierarchies.

Unit – VI

Symmetric shared memory architectures, distributed shared memory architectures, models of memory consistency, cache coherence protocols (MSI, MESI, MOESI), scalable cache coherence, overview of directory based approaches, design challenges of directory protocols, memory based directory protocols, cache based directory protocols, protocol design tradeoffs, synchronization.

Resources:

1. "Advanced computer architecture", Kai Hwang, Tata McGraw Hill,1993
2. "Computer organization and design" ,D. A. Patterson and J. L. Hennessey, 2nd Edition, Morgan Kaufmann,
3. "Computer Architecture and organization", J.P.Hayes, 3rd Edition, McGraw Hill,1998
4. "Memory System and Pipelined processors" Harvey G.Cragon , NarosaPublication,1998
5. "Parallel computer";V.Rajaranam & C.S.R.Murthy, Printice Hall of India,2002
6. "Foundation of Parallel Processing", K.Ghose, Rajan Moona & Phalguni Gupta, Narosa Publications,2002

		June 2019	1.00	Applicable for Sem 1 & 2 AY 2019-20 & Sem 3 & 4 AY 2021-22 Onwards
Chairperson	Dean (Acad. Matters)	Date of Release	Version	

Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

M. Tech. Scheme of Examination & Syllabus 2019

Electronics Engineering

II Semester

EE3929	PE IV: Pattern Recognition	L= 3	T = 0	P = 0	Credits = 3

Evaluation Scheme	MSEs *	TA	ESE	Total	ESE Duration
	30	10	60	100	3 Hrs

MSEs* = Three MSEs of 15 Marks each will be conducted and marks of better 2 of these 3 MSEs will be considered for Continuous Assessment

Objective	Outcomes
• Provide deeper knowledge of demanding methods of pattern recognition and of their applications.	Upon successfully completing the course, the student should: 1. Demonstrate the understanding of fundamentals of Bays Decision Theory 2. Able to understand parameter estimation and supervised learning, non-parametric techniques 3. be able to use linear discriminate functions, unsupervised learning and clustering 4. develop skill base necessary to further explore advanced topics of Pattern Recognition and their applications for research
Mapped Program Outcomes: a, b, d	

SN	Course Outcomes	Mapped PO						
		a	b	c	d	e	f	g
1	Upon successfully completing the course, the student should: Demonstrate the understanding of fundamentals of Bays Decision Theory	**H**			**M**			
2	Able to understand parameter estimation and supervised learning, non-parametric techniques		**H**		M			
3	be able to use linear discriminate functions, unsupervised learning and clustering	H						
4	develop skill base necessary to further explore advanced topics of Pattern Recognition and their applications for research		**M**		H			

Unit I

PATTERN RECOGNITION OVERVIEW: Engineering approach to PATTERN RECOGNITION, relationship of PATTERN RECOGNITION to other areas, Pattern recognition applications, pattern techniques, pattern recognition approaches (StatPR, SyntPR, NeurPR)
FEATURES AND FEATURE EXTRACTIONS TECHNIQUES: Introduction, zoned features, Graph representation techniques, sequentially detected features, feature extraction, feature vector and feature space.

Unit II

BAYS DECISION THEORY: Introduction, bays decision theory continuous case, two category classification, minimum error rate classification, classifier, discriminate functions and decision surfaces (multicategory and two category case). The normal density function (Univariate and multivariate normal density function)

Unit III

PARAMETER ESTIMATION AND SUPERVISED LEARNING: maximum likelihood estimation, Bayes classifier, general Bayesian learning, problem of dimensionally,

Unit IV

NON-PARAMATRIC TECHNIQUES, Density estimation, Parzen windows, k nearest estimation, nearest neighbor rule, k- nearest neighbor rule, approximation by Series expansion, approximation for binary case, Fisher's linear discriminant, Multiple discriminant analysis

Unit V

LINEAR DISCRIMINATE FUNCTIONS: Linear discriminate functions and decision surface, two category and multicategory case generalized linear discriminate functions, minimizing the perception criteria functions, relaxation procedure, minimum squared error procedures

Unit VI

UNSUPERVISED LEARNING AND CLUSTERING: Mixture densities and identifiability Maximum likelihood estimates, Unsupervised Bayesian learning, Data description and clustering, similarity measures, criterion functions for clustering, iterative optimization, hierarchical clustering

References:

1. Pattern classification and scene analysis, R. O. Duda and P. E. Hart, Wiley Interscience publications.
2. Pattern Recognition and Image Analysis, Earl Gose, Richard Johnsonbaugh, and Steve Jost; PHI Pvte. Ltd.,NewDelhi-1, 1999
3. Pattern Recognition, Sergios Theodoridis and Konstantinos Koutroumbas, Elsevier Academic Press, Second Edition, 2003,

		June 2019	1.00	Applicable for Sem 1 & 2 AY 2019-20 & Sem 3 & 4 AY 2021-22 Onwards
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III Semester

EE3938	**Seminar**	L= 0	T = 0	P = 2	Credits = 1

Evaluation Scheme	Continuous Evaluation	ESE	Total	ESE Duration
	100		100	

III Semester

EE3939	**Project Phase – I**	L= 0	T = 0	P = 16	Credits = 8
Evaluation Scheme	Continuous Evaluation	ESE		Total	ESE Duration
	100			100	

Objective	**Outcome**
	1. Students will be able to identify and formulate problem effectively through literature survey and analysis. 2. Students will be able present the idea effectively with good presentation and communication skill 3. Students will be able to use related EDA tools and related software. 4. Students will be able to understand project management and the importance of social and research ethics.
Mapped PO: a, b, c, d, e, f, g	

IV Semester

EE3940	**Project Phase – II**	L= 0	T = 0	P = 24	Credits = 12

Evaluation Scheme	Continuous Evaluation	ESE	Total	ESE Duration
	40	60	100	

Objective	Outcome
	1. Students will be able to identify and formulate problem effectively through literature survey and analysis. 2. Students will be able present the idea effectively with good presentation and communication skill 3. Students will be able to use related EDA tools and related software. 4. Students will be able to understand project management and the importance of social and research ethics.
Mapped PO: a ,b, c, d, e, f, g	