YESHWANTRAO CHAVAN COLLEGE OF ENGINEERING
(An Autonomous Institution affiliated to R T M Nagpur University Nagpur)
Accredited by NAAC (1st Cycle) with 'A' Grade (Score 3.25 on 4 Point Scale)
Wanadongri, Hingna Road, Nagpur-441110

Department of Electronics Engineering
(Honors in VLSI Design)

B.E. Honors in VLSI Design
SoE & Syllabus 2021-22

B.E Honors in VLSI Design

Information Brochure of Honor Program

1. **Title of the Program: B.E Honors in VLSI Design**
2. **Type of Program: Honor**
3. **Department offering the program: Electronics Engineering**
4. **Industry / Association / Collaboration: Intel Corporation, Bangalore Cadence, Bangalore**
5. **Department/s eligible to opt for the program:**

   The students of Department of Electronics Engineering are only permitted to opt for this program.
6. **General information about courses in program:**

   This course will provide students with the ability to design state-of-the-art digital CMOS circuits. The course introduces students to what is becoming a fundamental design technique. The ability to design integrated circuits or to at least be able to analyze other designs is becoming a necessity for many computer engineering students entering the work force or pursuing an advanced degree. In addition, this course allows students to see how physically to implement some of the designs or design techniques they have learned in other classes. Very-large-scale integration (VLSI) is commonly known as chip-design. VLSI is a method that generates integrated circuits by integrating thousands of transistor-based circuits into a single chip. It can quickly search an application in Communications, DSP, MEMS, Microwave and RF, Consumer Electronics, Cryptography, Automobiles, Robotics, Space Applications and Health industry. Today, VLSI gadgets can be found all around us. We can find progressed VLSI contributions to our vehicles, mobile phones, electronic appliances, cameras, medicinal machines, and many different places. This rapidly growing sector is opening its doors in verification based employment opportunities for those with solid basics in electronic circuit structure and hardware description languages, VLSI designing and verification.

7. Advance knowledge or research orientation of Program:

This course introduces to the concepts and techniques of modern integrated circuit design. It also provides specialization in offering Verification of design, ASIC Design flow and concepts on advanced ASIC verification methodologies and technologies. VLSI Design Methodologies course is a front end VLSI course which imparts the VLSI Design Flow, Digital Design and RTL programming using Verilog HDL. This course starts with an overview of VLSI and explains VLSI technology, ASIC design, Moore's law and the difference between ASIC and FPGA. With this overview, it walks you through all the steps of complete VLSI Design flow and explains every step in detail. Then it covers the complete digital design, combinational, sequential designs. And finally it trains you extensively on Verilog HDL programming and makes you a hands-on RTL designer.

8. Employability potential of program:

With the development in electronic gadgets, higher technology like utilities, procedure geometries, and product innovation consistently, there is a constant requirement to design, build and re-make integrated circuits (ICs). Since devices like cell phones are being made with new features in a very short time. There is a high demand for skilled VLSI (Very Large Scale Integration) designers to take a shot at these products. Thus, there is a huge demand for qualified VLSI professionals in semiconductor industry. Use of computer aided design (CAD) tools for circuit design and simulation enables the students to grab the opportunity in VLSI designed based Industries like Intel Semiconductors, Tessolve Semiconductors, Texas Instruments, Wipro, IBM, NXP, Cypress, Broadcom, Qualcomm, ST Micro, AMD, Avago Tech etc.

9. Departmental Steering committee: For proper publicity / conduct of program

SN	Name of the Faculty Member	Post	Designation	e-mail ID	Contact Number
1	Dr. P. T. Karule	Chairman	Prof. & Head	ptkarule@gmail.com	9764996490
2	Dr. S. V. Rathkanthiwar	Member	Professor	svr_1967@yahoo.com	9764996797
3	Dr. A. S. Khobragade	Member	Professor	atish_khobragade@rediffmail.com	9765005110
4	Dr. R. D. Thakre	Member	Professor	rdt2909@gmail.com	9423603236

10. Program Coordinator:

SN	Name of the Faculty Member	Post	Designation	e-mail ID	Contact Number
1	Vilas Alagdive	Coordinator	Asst.Professor	vilas_a23@rediffmail.com	7768842506

Scheme of Examinations
B.E Honors in Honors in VLSI Design

SN	Sem	Sub. Code	Subject	T/P	Contact Hours				Credits	% Weightage			ESE Duration Hours
					L	T	P	Hrs		MSEs*	TA**	ESE	
1	5	EEH131	Synthesis & Optimization of VLSI Circuits	T	3	0	0	3	3	30	30	40	3 Hours
2	5	EEH132	Advanced Digital System Design	T	3	0	0	3	3	30	30	40	3 Hours
3	5	EEH133	Lab: Advanced Digital System Design	P	0	0	2	2	1		60	40	
4	6	EEH141	VLSI Testing	T	3	0	0	3	3	30	30	40	3 Hours
5	6	EEH142	Digital IC Design	T	3	0	0	3	3	30	30	40	3 Hours
6	6	EEH143	Lab: Digital IC Design	P	0	0	2	2	1		60	40	
7	7	EEH151	Low Power CMOS VLSI Design	T	3	0	0	3	3	30	30	40	3 Hours
8	7	EEH152	Lab: Low Power CMOS VLSI Design	P	0	0	2	2	1		60	40	
			TOTAL		**15**	**0**	**6**	**21**	**18**				

MSEs* = Three MSEs of 15 Marks each will conducted and marks of better 2 of these 3 MSEs will be considered for Continuous Assessment

TA ** = for Theory : 20 marks on lecture quizzes, 8 marks on assignments, 2 marks on class performance
TA = for Practical : MSPA will be 15 marks each**

5th Semester

EEH131	Synthesis & Optimization of VLSI Circuits			L= 3	T = 0	P = 0	Credits = 3
Evaluation Scheme ***Best Two out of three MSE's would be considered**	MSE-I*	MSE-II*	MSE-III*	TA	ESE	Total	ESE Duration
	15	15	15	30	40	100	3 Hrs
Prerequisites							

Course Objective

Students should be able to

1. Acquaint concept of Optimization of Very Large Scale Integration (VLSI) circuit and systems design.

Course Outcome

Students will be able to

1. Understand basic Boolean functions, their representations and different CAD based synthesis and optimization issues.
2. Understand, able to analyze and solve the algorithms which underpin behavioral synthesis including scheduling, allocation and binding.
3. Understand and able to analyze high level synthesis issues, two level logic optimization, multilevel logic optimization, and sequential logic optimization.
4. Understand and able to apply the Satisfiability (SAT) concept.

UNIT I :

Microelectronics, semiconductor technologies and circuit taxonomy, microelectronic design styles, computer aided synthesis and optimization. Graphs Notation, undirected graphs, directed graphs, combinatorial optimization, Algorithms, tractable and intractable problems, algorithms for linear and integer programs, graph optimization problems and algorithms, Boolean algebra and Applications

UNIT II :

Hardware Modeling Languages, distinctive features, structural hardware language, Behavioral hardware language, HDLs used in synthesis, abstract models, structures logic networks, state diagrams, data flow and sequencing graphs, compilation and optimization techniques.

UNIT III :

Logic optimization, principles, operation on two level logic covers, algorithms for logic minimization, symbolic minimization and encoding property, minimization of Boolean relations. Multiple level combinational optimizations: Models and transformations

UNIT IV :

Combinational networks, algebraic model, Synthesis of testable network, algorithm for delay evaluation and optimization, rule based system for logic optimization. Sequential circuit optimization, Sequential circuit optimization using state based models, sequential circuit optimization using network models.

UNIT V:
A model for scheduling problems, Scheduling with resource and without resource constraints, Scheduling algorithms for extended sequencing models, Scheduling Pipe lined circuits. Cell library binding, Problem formulation and analysis, algorithms for library binding, specific problems and algorithms for library binding (lookup table F.P.G.As and Antifuse based F.P.G.As), rule based library binding.

UNIT VI:
Simulation, Types of simulators, basic components of a simulator, fault simulation Techniques, Automatic test pattern generation methods (ATPG), design for Testability (DFT) Techniques.

Text Books:

	Title	Edition	Author	Publisher
1	Synthesis and Optimization of Digital Circuits	1 st Edition	Giovanni De Micheli	Tata McGraw-Hill, 2003

Reference Book:

	Title	Edition	Author	Publisher
1	Logic Synthesis	1st Edition,	Srinivas Devadas Abhijit Ghosh, and Kurt Keutzer	McGraw-Hill, USA, 1994**.**

5th Semester

EEH132	Advanced Digital System Design			L= 3	T = 0	P = 0	Credits = 3
Evaluation Scheme	MSE-I*	MSE-II*	MSE-III*	TA	ESE	Total	ESE Duration
***Best Two out of three MSE's would be considered**	15	15	15	30	40	100	3 Hrs
Prerequisites							

Course Objective

Students should be able to

1. Expose students to the advanced design techniques and methodology and industrial standard EDA tools in Digital Circuits and Systems design

Course Outcome

Students will be able to

1. Design and analyse combinational and sequential logic circuits.
2. Understand hardware description language and able to design and simulate digital systems using different abstraction levels
3. Understand and apply timing issues in multiple contexts and design the circuit.
4. Understand programmable devices and able to design digital systems using modern design tools

UNIT I :

Digital Design Fundamentals, Combinational & Sequential design issues, Introduction to finite state machines, Moore & Mealy Machine, Introduction to programmable devices, PLA, PAL, PROM, Structure of CPLDs, Introduction to FPGA, Architecture, CLB, IOB, Programmable Interconnect Points, Different type of programmable switches used in PLDs.

UNIT II :

HDL Based Design flow, Requirements of HDL, Design Methodologies, Different Modelling styles, Introduction to Verilog, Elements of Verilog, Verilog Module definition, Elements of Module.

UNIT III :

Basic Concepts in Verilog, Reserved Keywords, Syntax & Semantics, Comments, Identifiers, Number Representation, System Representation, Verilog Ports, Verilog Data Types, Wire & Variables, Physical & Abstract, Constants, Parameter, Verilog Data Operators, Design entry in Verilog & Testbench, Compilation and synthesis, Timing analysis

UNIT IV :

Data Flow Modelling, Delay, Continuous Assignment, Delayed Continuous assignment, Structural Modelling Feature, Module Instantiation, Gate level Primitives, Gate Delays, Switch Level Primitives, User Defined Primitives.

UNIT V:

Behavioral Modelling, Initial, Always, Procedural Assignment, Blocking and Non- Blocking assignments,Sequential & Parallel Blocks, Race around Condition, Timing Control, Procedural Statements, Conditional Statements if case loop repeat forever etc, Zero Delay Control, Event Based Timing Control, Compiler Directives, Assign Deassign, Force Release, Latch Models, FF Models, State Machine Coding ,Moore and Mealy Machines.

UNIT VI:

Combinational & sequential system Design examples like Shift Registers, Counters, LFSR, Stacks and Queues, Multi bit Adders & Multiplier, Huffman Coding, Processor and Memory Model , CPU, System Tasks and Functions, Design Verification.

Text Books:

	Title	Edition	Author	Publisher
1	Verilog HDL : A Guide to Digital Design and Synthesis	, 2nd Edition	Samir Palnitkar	2003

Reference Book:

	Title	Edition	Author	Publisher
1	Verilog Digital System Design	Second Edition	Zainalabedin Navabi	Tata McGraw Hill , 2009

5th Semester

EEH133	Lab: Advanced Digital System Design			L= 0	T = 0	P = 1	Credits = 1
Evaluation Scheme	MSE-I*	MSE-II*	MSE-III*	TA	ESE	Total	ESE Duration
***Best Two out of three MSE's would be considered**	--	--	--	60	40	100	3 Hrs
Prerequisites							

Course Objective

Students should be able to

1. Expose students to the advanced design techniques and methodology and industrial standard EDA tools in Digital Circuits and Systems design

Course Outcome

Students will be able to

1. Design and analyse combinational and sequential logic circuits.
2. Understand hardware description language and able to design and simulate digital systems using different abstraction levels
3. Understand and apply timing issues in multiple contexts and design the circuit.
4. Understand programmable devices and able to design digital systems using modern design tools

SN	Experiment Name
1.	Verilog Code using Bitwise Operator .Test it with test stimuli generated by test bench
2.	Using GATE level primitive write verilog code and test it with test stimuli generated by test bench
3.	Verilog code using DATA flow modelling style. Test it with test stimuli generated by test bench
4.	Write verilog code using conditional assignment statement. Test it with test stimuli generated by test bench
5.	Write verilog code using Structural Modeling style. Test it with test stimuli generated by test bench
6.	Verilog code using Behavioural modeling style. Test it with test stimuli generated by test bench
7.	Write UDP for A. Combinational Circuit B.Sequential circuit
8.	Write Verilog code using switch level modeling for a. NAND gate b. Full adder using transmission gate
9.	Write verilog code using while loop
10.	Write Verilog code for Mealy and Moore sequence detector.(using overlapping allowed and not allowed)

Text Books:				
	Title	**Edition**	**Author**	**Publisher**
1	Verilog HDL : A Guide to Digital Design and Synthesis	, 2nd Edition	Samir Palnitkar	2003
Reference Book:				
	Title	**Edition**	**Author**	**Publisher**
1	Verilog Digital System Design	Second Edition	Zainalabedin Navabi	Tata McGraw Hill , 2009

6th Semester

EEH141	VLSI Testing			L= 3	T = 0	P = 0	Credits = 3
Evaluation Scheme	MSE-I*	MSE-II*	MSE-III*	TA	ESE	Total	ESE Duration
***Best Two out of three MSE's would be considered**	15	15	15	30	40	100	3 Hrs
Prerequisites							

Course Objective

Students should be able to

1. Gain a knowledge from the area of applying diagnostic principles in the design of modern Electronic systems

Course Outcome

Students will be able to

1. Develop an understanding of VLSI design verification and testing issues.
2. Learn how to generate test patterns for faults in a system and how to design a system for testability.
3. Model different faults and carry out fault simulation in digital circuits.
4. Know about importance of testing and its types in VLSI circuits.

UNIT I :

Overview Of Testing: Design Process, Verification, Faults & Their Detection, Test Pattern Generation,Fault Coverage, Types Of Tests, Test Application, Testing Economics. Defects, Failures, and Faults: Physical
Defects, Failures Modes, Faults, Fault Equivalence and Dominance, Fault Collapsing

UNIT II :

Design Representation: Graphical representation, Graphs, Binary Decision diagrams, Netlists, VLSI Design Flow: CAD tools, Design Methodologies, Semicustom Design

UNIT III :

Simulation: Logic Simulation, Approaches to Simulation, Fault Simulation & Their Results. Automatic Test Pattern Generation: D-Algorithm, Critical Path Extensions to D-Algorithm PODEM

UNIT IV :

Ad Hoc Techniques, Scan–Path Design, Test pattern generation, Test Pattern Application, Scan architectures, multiple scan chains, Partial Scan Testing

UNIT V:

Boundary-Scan Testing: Boundary Scans Architecture, Test Access Port, Registers, Tap Controller,Modes of Operation. Built In Self Test: Pseudorandom Test Pattern Generation, Response Compaction, BIST Architectures

UNIT VI:
Memory Testing: Types of Memory Testing, Functional Testing Schemes, Testing FPGAs and Microprocessors: Testability Of FPGAs, Testing RAM- Based FPGAs, Testing Microprocessors, Synthesis For Testability

Text Books:

	Title	Edition	Author	Publisher
1	Essentials of Electronic Testing for Digital, Memory, and Mixed-Signal VLSI Circuits	2nd Edition 2003	MichaelL.Bushnell and Vishwani D. Agrawal,	B.S.Publications
2	HDL Chip Design	3rd Edition2008	Douglas Smith	Doone Publications

Reference Book:

	Title	Edition	Author	Publisher
1	A Guide to VHDL	2nd Edition2007	Stanley Mazor	Kluwer Academic Pres

6th Semester

EEH142	**Digital IC Design**			L= 3	T = 0	P = 0	Credits = 3
Evaluation Scheme	MSE-I*	MSE-II*	MSE-III*	TA	ESE	Total	ESE Duration
***Best Two out of three MSE's would be considered**	15	15	15	30	40	100	3 Hrs
Prerequisites							

Course Objective

Students should be able to

1. Understand knowledge and skills in the area of CAD design of digital circuits, units and systems on currently usable VLSI chips.

Course Outcome

Students will be able to

1. Demonstrate issues related to the development of digital integrated circuits including fabrication, circuit design, implementation methodologies
2. Solve complex circuit problems and optimization techniques
3. Design CMOS combinational, sequential logic design
4. Design programmable logic arrays

UNIT I :

MOS transistors, CMOS logic, NAND gate, combinational logic, NOR gate, Compound gates, Pass transistor and transmission gates, tristates, multiplexers, latches and flip flops, inverter cross section, fabrication process, Layout design rules, CMOS processing technology, CMOS Process enhancements, stick diagram, VLSI design flow ,Euler path in a CMOS gate.

UNIT II :

MOS transistor theory, Working of NMOS enhancement transistor & PMOS enhancement transistor, Ideal Current voltage characteristics, threshold voltage , non-ideal current voltage effects, velocity saturation, mobility degradation, channel length modulation, Body effect, sub-threshold conduction, Junction leakage, Tunneling, Temperature dependence, Geometry dependence, Small signal AC characteristics, CMOS inverter DC transfer characteristics, Beta ratio effects, noise margin, Ratioed inverter transfer function, switch level RC delay models

UNIT III :

Delay estimation, RC delay models, linear delay model, logical effort, parasitic delay, Delay in a logic gate, delay in a multi stage logic networks, power dissipation, interconnect, design margin, Reliability, Scaling

UNIT IV :

Circuit families, static CMOS, Ratioed circuits, Cascode voltage switch logic, dynamic circuits, pass transistor circuits, differential circuits, sense amplifier circuits, Bi-CMOS circuits

UNIT V:
Sequencing static circuits, Sequencing methods, Max-delay constraints, Min-delay constraints, Time borrowing, clock skew, circuit design of latches and Flip flops, static sequencing element methodology, Two phase timing types, characterizing sequencing element delays, sequencing dynamic circuits, Synchronizers

UNIT VI:
Static Random access memory, Dynamic random access memory, serial access memories, Content addressable memory Programmable logic arrays.

Text Books:

	Title	Edition	Author	Publisher
1	CMOS VLSI design: A Circuits and Systems Perspective	3rd Edition	Neil H. E. Weste, David F. Harris, A.Banerjee,	Addison Wesley Publication, 2008

Reference Book:

	Title	Edition	Author	Publisher
1	CMOS Digital Integrated Circuits: Analysis and Design	3rd Edition	Sung-Mo Kang, Yusuf Lebeleci	McGraw-Hill Publications, 2002

6th Semester

EEH143	Lab: Digital IC Design			L= 0	T = 0	P = 1	Credits = 1
Evaluation Scheme	MSE-I*	MSE-II*	MSE-III*	TA	ESE	Total	ESE Duration
***Best Two out of three MSE's would be considered**	--	--	--	60	40	100	3 Hrs
Prerequisites							

Course Objective

Students should be able to

1. Understand knowledge and skills in the area of CAD design of digital circuits, units and systems on currently usable VLSI chips.

Course Outcome

Students will be able to

1. Demonstrate issues related to the development of digital integrated circuits including fabrication, circuit design, implementation methodologies
2. Solve complex circuit problems and optimization techniques
3. Design CMOS combinational, sequential logic design
4. Design programmable logic arrays

SN	Experiment Name
1.	a) Plot current voltage characteristics of NMOS transistor using 0.5 micron technology b) Plot current voltage characteristics of PMOS transistor using 0.5 micron technology
2.	To design and simulate CMOS inverter using 0.5 micron technology
3.	A plot transfer characteristic of Pseudo-NMOS inverter with w/l for PMOS is equal to twice w/l of NMOS.
4.	Design and simulate two input CMOS NAND gate
5.	Design two input CMOS NOR gate.
6.	Design CMOS transmission gate.
7.	Design and simulate D-Latch using transmission gate
8.	Design 2:1 MUX using transmission gate.
9.	Design two input CMOS XOR gate
10.	Design function f=not(A+B+C+D) using Euler path approach

Text Books:				
	Title	**Edition**	**Author**	**Publisher**
1	CMOS VLSI design: A Circuits and Systems Perspective	3rd Edition	Neil H. E. Weste, David F. Harris, A.Banerjee,	Addison Wesley Publication, 2008

Reference Book:				
	Title	**Edition**	**Author**	**Publisher**
1	CMOS Digital Integrated Circuits: Analysis and Design	3rd Edition	Sung-Mo Kang, Yusuf Lebeleci	McGraw-Hill Publications, 2002

7th Semester

EEH151	**Low Power CMOS VLSI Design**			L= 3	T = 0	P = 0	Credits = 3
Evaluation Scheme	MSE-I*	MSE-II*	MSE-III*	TA	ESE	Total	ESE Duration
***Best Two out of three MSE's would be considered**	15	15	15	30	40	100	3 Hrs
Prerequisites							

Course Objective

Students should be able to

1. expose students to the advanced design techniques and methodology and industrial standard EDA tools in Digital Circuits and Systems design

Course Outcome

Students will be able to

1. Graduates will understand the concepts of sources of power dissipation and basics of CMOS Physics.
2. Understand the concepts of levels of abstraction and its power dissipation.
3. Understand the Power Optimization methods at Behaviour, Logic and Circuit Level design.
4. Understand the principles for low power designs, and have the capabilities to analyze power consumption and develop low power strategies for a given system.

UNIT I :

Need for low power VLSI chips, Sources of power dissipation: Short circuit dissipation, dynamic dissipation, designing Techniques for low power. Physics of power dissipation in MOSFET devices, MOS Capacitance analysis, low power figure of merits, brief overview of low power VLSI design limits.

UNIT II :

Probabilistic power analysis: random logic signals, probability and frequency, probabilistic power analysis techniques, signal entropy, Low power circuits: transistor and gate sizing, equivalent pin ordering, network
reconstruction and reorganization, Glitching Power, special latches and flip-flops.

UNIT III :

Behavioural, Logic and circuit level approaches. Algorithm level transforms. Circuit activity driven architectural transformations, voltage scaling, operation reduction and substitution, pre-computation, Logic:gate reorganization, signal gating, logic encoding

UNIT IV :

Design style, Leakage current in Deep sub-micron transistors, device design issues, minimizing shortchannel effect. Low voltage design techniques using reverse Vgs. Steep sub threshold swing and multiple threshold voltages. Multiple threshold CMOS based on path critically, multiple supply voltages.

UNIT V:
Low energy computing, Energy dissipation in transistor channel. Energy recovery circuit design,designs with reversible and partially reversible logic, energy recovery in adiabatic logic and SRAM core, Design of peripheral circuits – address decoder, level shifter and IO Buffer, supply clock generation

UNIT VI:
Introduction, sources of software power dissipation, power estimation and optimization. Co-design for low power

Text Books:

	Title	Edition	Author	Publisher
1	Solid State Electronic Devices	6th Edition	Ben Streetman, Sanjay Benerjee	Prentice Hall India
2	Low-Power CMOS VLSI Circuit Design	1st Edition	Kaushik Roy, Sharat C. Prasad	Wiley India,2009
3	CMOS VLSI design: A Circuits and Systems Perspective	3rd Edition	Neil H. E. Weste, David F. Harris, A.Banerjee,	Addison Wesley Publication, 2008

Reference Book:

	Title	Edition	Author	Publisher
1	Low-Power Digital CMOS Design	2nd Edition	A. Chandrakasan and R. Brodersen	Boston: Springer, 1995.
2	CMOS Digital Integrated Circuits: Analysis and Design	3rd Edition	Sung-Mo Kang, Yusuf Lebeleci	McGraw-Hill Publications, 2002

7th Semester

EEH152	**Lab: Low Power CMOS VLSI Design**			L= 0	T = 0	P = 1	Credits = 1
Evaluation Scheme ***Best Two out of three MSE's would be considered**	MSE-I*	MSE-II*	MSE-III*	TA	ESE	Total	ESE Duration
	--	--	--	60	40	100	3 Hrs
Prerequisites							

Course Objective

Students should be able to

1. expose students to the advanced design techniques and methodology and industrial standard EDA tools in Digital Circuits and Systems design

Course Outcome

Students will be able to

1. Graduates will understand the concepts of sources of power dissipation and basics of CMOS Physics.
2. Understand the concepts of levels of abstraction and its power dissipation.
3. Understand the Power Optimization methods at Behaviour, Logic and Circuit Level design.
4. Understand the principles for low power designs, and have the capabilities to analyze power consumption and develop low power strategies for a given system.

SN	Experiment Name
1.	Plot current voltage characteristics of NMOS transistor using CMOS technology
2.	Design function $F=\overline{(A*B*C)+(D*E)}$ with complementary CMOS Logic and pseudo NMOS Logic.
3.	Design function $F=\overline{(A+B)*(C+D)}$ with complementary CMOS Logic and pseudo NMOS Logic.
4.	Design two input CMOS XOR gate
5.	Design two input CMOS XNOR gate
6.	Design adiabatic Half Adder
7.	Design adiabatic Half Subtractor
8.	Design adiabatic Full Adder
9.	Design adiabatic 2:1 Multiplexer
10.	Design adiabatic 4:1 Multiplexer

Text Books:				
	Title	**Edition**	**Author**	**Publisher**
1	Solid State Electronic Devices	6th Edition	Ben Streetman, Sanjay Benerjee	Prentice Hall India
2	Low-Power CMOS VLSI Circuit Design	1st Edition	Kaushik Roy, Sharat C. Prasad	Wiley India,2009
3	CMOS VLSI design: A Circuits and Systems Perspective	3rd Edition	Neil H. E. Weste, David F. Harris, A.Banerjee,	Addison Wesley Publication, 2008

Reference Book:				
	Title	**Edition**	**Author**	**Publisher**
1	Low-Power Digital CMOS Design	2nd Edition	A. Chandrakasan and R. Brodersen	Boston: Springer, 1995.
2	CMOS Digital Integrated Circuits: Analysis and Design	3rd Edition	Sung-Mo Kang, Yusuf Lebeleci	McGraw-Hill Publications, 2002