Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

Hingna Road, Wanadongri, Nagpur - 441 110

Post Graduation (M. Tech.)

SoE & Syllabus 2014

1 to 4 Semester

VLSI DESIGN

Update on May 2017

Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

M. Tech. SCHEME OF EXAMINATION 2014

Department of Electronics Engineering

VLSI DESIGN

Sl. No.	Course Code	Course Title	Contact Hours L	Contact Hours T	Contact Hours P	Total Contact Hrs.	Credits	% Weightage MSE - I	% Weightage MSE - II	% Weightage TA	% Weightage ESE	ESE Duration Hrs.
		I SEMESTER										
1	EE1951	VLSI Signal Processing	3	0	0	3	3	15	15	10	60	3
2	EE1952	Digital IC Design	3	0	0	3	3	15	15	10	60	3
3	EE1953	VLSI Technology	3	0	0	3	3	15	15	10	60	3
4	EE1954	Embedded System & RTOS	3	0	0	3	3	15	15	10	60	3
5	EE1955	Advanced Digital System Design	3	0	0	3	3	15	15	10	60	3
6	EE1956	Lab: Embedded System & RTOS	0	0	2	2	1			40	60	
7	EE1957	Lab: Digital IC Design	0	0	2	2	1			40	60	
8	EE1958	Lab: Advanced Digital System Design	0	0	2	2	1			40	60	
			15	**0**	**6**	**21**	**18**					
		II SEMESTER										
1	EE1961	RF Circuit design	3	0	0	3	3	15	15	10	60	3
2	EE1962	Analog IC Design	3	0	0	3	3	15	15	10	60	3
3	EE1963	Sythesis & Optimisation of VLSI Circuits	3	0	0	3	3	15	15	10	60	3
4	**Professional Elective - I**		3	0	0	3	3	15	15	10	60	3
	EE1966	Low Power CMOS VLSI Design										
	EE1967	Hardware Software Codesign										
	EE1968	Nano Scale MOS Transistors										
5	**Professional Elective - II**		3	0	0	3	3	15	15	10	60	3
	EE1969	Verification & Testing of VLSI Circuit										
	EE1970	Digital Image Processing										
	EE1971	Solid State Devices & Modelling										
6	EE1964	Lab: RF Circuit design	0	0	2	2	1			40	60	
7	EE1965	Lab: Analog IC Design	0	0	2	2	1			40	60	
8	EE1972	Seminar	0	0	2	2	1			100		
			15	**0**	**6**	**21**	**18**					
		III SEMESTER										
1	**Professional Elective - III**		3	0	0	3	3	15	15	10	60	3
	EE1982	Mixed Signal VLSI Design										
	EE1983	Micro Electro Mechanical Systems										
	EE1984	VLSI for wireless communication										
2	**Professional Elective - IV**		3	0	0	3	3	15	15	10	60	3
	EE1985	ASIC Design										
	EE1986	Semiconductor Memory Design										
	EE1987	Advanced Computer Architecture										
3	EE1981	Project Phase - I	0	0	16	16	8			100		
			6	**0**	**16**	**22**	**14**					
		IV SEMESTER										
1	EE1991	Project Phase - II	0	0	24	24	12			40	60	
			0	**0**	**24**	**24**	**12**					
		Grand Total of Credits					**62**					

Chairperson	**Date of Release**	May 2014	**Applicable for**
Dean (Acad. Matt.)	**Version**	**1**	**AY 2014-15 Onwards**

I Semester

EE1951 / EE1920	VLSI Signal Processing	L= 3	T = 0	P = 0	Credits = 3

Evaluation Scheme	MSE-I	MSE-II	TA	ESE	Total	ESE Duration
	15	15	10	60	100	3 Hrs

Objective	Outcomes
• The students shall gain proficiency in subjects like the basic design of theory involved in VLSI for signal processing and communication systems , various software tools related to VLSI, Signal Processing and Communication Systems.	1. Graduates will understand and able to design architectures for DSP algorithms. 2. Graduates will understand and able to apply the optimisation concept in terms of area, speed and power on DSP systems. 3. Graduates will understand and able to optimize DSP arithmetic.
Mapped Program Outcomes: a, d	

SN	Course Outcomes	Mapped PO						
		a	b	c	d	e	f	g
1	Graduates will understand and able to design architectures for DSP algorithms.	H			M			
2	Graduates will understand and able to apply the optimisation concept in terms of area, speed and power on DSP systems.	M			M			
3	Graduates will understand and able to optimize DSP arithmetic.	M			H			

UNIT I:

Introduction to DSP systems, Data flow and Dependence graphs - critical path, Loop bound, iteration bound, longest path matrix algorithm, Pipelining and Parallel processing of FIR filters, parallel processing, Pipelining and parallel processing for low power.

UNIT II:

Retiming – definitions and properties, solving systems of inequalities, Retiming techniques, Unfolding – an algorithm for unfolding, properties of unfolding, sample period reduction and parallel processing application

UNIT III:

Folding: folding transformation, Register Minimization Techniques, Register minimization in folded architectures folding of multirate systems. Systolic Architecture Design: Introduction, Systolic Array Design Methodology, FIR systolic Arrays, Selection of scheduling vector, Matrix Multiplication and 2D systolic array Design, Systolic design for space representations containing Delays.

UNIT IV:

Fast convolution – Cook-Toom algorithm, modified Cook-Toom algorithm, Winograd algorithm, iterated and cyclic convolution, Algorithmic strength reduction in filters and transforms – 2-parallel FIR filter, 2-parallel fast FIR filter, rank-order filters, Odd-Even merge-sort architecture, parallel rank order filters.

UNIT V:

Bit-level arithmetic architectures – parallel multipliers with sign extension, parallel carry-ripple and carry-save multipliers, Design of Lyon's bit-serial multipliers using Horner's rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner's rule for precision improvement, Distributed Arithmetic.

I Semester

EE1951 / EE1920	**VLSI Signal Processing**	L= 3	T = 0	P = 0	Credits = 3

Evaluation Scheme	MSE-I	MSE-II	TA	ESE	Total	ESE Duration
	15	15	10	60	100	3 Hrs

Unit VI:

Redundant number representation, carry free radix-2 addition and subtraction, hybrid radix 4 addition,radix2 hybrid redundant multiplication architectures, data format conversion, redundant to non redundant converter, Numerical strength reduction – sub-expression elimination, multiple constant multiplication, iterative matching.

Resources:

1. Keshab K. Parhi, "VLSI Digital Signal Processing Systems, Design and implementation ", Wiley, Interscience, 2007.
2. U. Meyer – Baese, " Digital Signal Processing with Field Programmable Gate Arrays", Springer, Second Edition, 2004

I Semester

EE1952 / EE1902	Digital IC Design	L=3	T = 0	P = 0	Credits = 3

Evaluation Scheme	MSE-I	MSE-II	TA	ESE	Total	ESE Duration
	15	15	10	60	100	3 Hrs

Objective	Outcomes
• The aim of this course is to give knowledge and skills in the area of CAD design of digital circuits, units and systems on currently usable VLSI chips.	1. Graduates will able to demonstrate issues related to the development of digital integrated circuits including fabrication, circuit design, implementation methodologies 2. Graduates will able to Solve complex circuit problems and optimization techniques 3. Graduates will able to design CMOS combinational, sequential logic design
Mapped Programme outcomes: a, d	

SN	Course Outcomes	Mapped PO						
		a	b	c	d	e	f	g
1	Graduates will able to demonstrate issues related to the development of digital integrated circuits including fabrication, circuit design, implementation methodologies	H						
2	Graduates will able to Solve complex circuit problems and optimization techniques				M			
3	Graduates will able to design CMOS combinational, sequential logic design				M			

Unit I: CMOS processing technology:

MOS transistors, CMOS logic, NAND gate, combinational logic, NOR gate, Compound gates, Pass transistor and transmission gates, tristates, multiplexers, latches and flip flops, inverter cross section, fabrication process, Layout design rules, CMOS processing technology, CMOS Process enhancements, stick diagram, VLSI design flow ,Euler path in a CMOS gate.

Unit II: MOS transistor theory:

MOS transistor theory, Working of nMOS enhancement transistor & PMOS enhancement transistor, Ideal Current voltage characteristics, threshold voltage , nonideal current voltage effects, velocity saturation, mobility degradation, channel length modulation, Body effect, subthreshold conduction, Junction leakage, Tunneling, Temperature dependence, Geometry dependence, Small signal AC characteristics, CMOS inverter DC transfer characteristics, Beta ratio effects, noise margin, Ratioed inverter transfer function, switch level RC delay models

Unit III: Circuit characterization and performance estimation:

Delay estimation, RC delay models, linear delay model, logical effort, parasitic delay, Delay in a logic gate, delay in a multistage logic networks, power dissipation, interconnect, design margin, Reliability, Scaling

Unit IV: Combinational circuit design:

Circuit families, static CMOS, Ratioed circuits, Cascode voltage switch logic, dynamic circuits, pass transistor circuits, differential circuits, sense amplifier circuits, BiCMOS circuits

Unit V: Sequential Circuit design:

Sequencing static circuits, Sequencing methods, Max-delay constraints, Min-delay constraints, Time borrowing, clock skew, circuit design of latches and Flip flops, static sequencing element methodology, Two phase timing types, characterizing sequencing element delays, sequencing dynamic circuits, Synchronizers.

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Dean (Acad. Matters)		Version	1.01	

I Semester

EE1952 / EE1902	Digital IC Design	L=3	T = 0	P = 0	Credits = 3

Evaluation Scheme	MSE-I	MSE-II	TA	ESE	Total	ESE Duration
	15	15	10	60	100	3 Hrs

Unit VI: Array subsystems:

Static Random access memory, Dynamic random access memory, serial access memories, Content addressable memory Programmable logic arrays.

Resources:

1. "CMOS VLSI design: A Circuits and Systems Perspective", Neil H. E. Weste, David F. Harris, A.Banerjee, 3rd Edition, Addison Wesley Publication, 2008
2. "CMOS Digital Integrated Circuits: Analysis and Design", Sung-Mo Kang, Yusuf Lebeleci, 3rd Edition, McGraw-Hill Publications, 2002

Chairperson		Date of Release	May 2017	Applicable for AY 2017-18 Onwards
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I Semester

EE1953	VLSI Technology	L= 3	T = 0	P = 0	Credits = 3

Evaluation Scheme	MSE-I	MSE-II	TA	ESE	Total	ESE Duration
	15	15	10	60	100	3 Hrs

Objective	Outcomes
• The objective of the VLSI Technology is to identify new/hot areas of interest to the Electron Devices and Solid-State Circuits communities.	1. Graduates will be able to understand the Fabrication of ICs and purification of Silicon in different technologies. 2. Graduates will be able to understand impart in-depth knowledge about Etching and deposition of different layers. 3. Graduates will be able to understand the different packaging techniques of VLSI devices.
Mapped Programme outcomes: a, b, c	

SN	Course Outcomes	Mapped PO						
		a	b	c	d	e	f	g
1	Graduates will be able to understand the Fabrication of ICs and purification of Silicon in different technologies.	H	H	M				
2	Graduates will be able to understand impart in-depth knowledge about Etching and deposition of different layers.	H	M	M				
3	Graduates will be able to understand the different packaging techniques of VLSI devices.	H	M	M				

Unit I

Crystal growth & wafer preparation, Processing considerations: Chemical cleaning, gettering the thermal Stress factors.Epitaxy: Vapors phase Epitaxy, Basic Transport processes & reaction kinetics, doping & auto doping, equipments, safety considerations, buried layers, epitaxial defects, molecular beam epitaxy, equipment used, film characteristics, SOI structure.

Unit II

Oxidation: Growth mechanism & kinetics, Silicon oxidation model, interface considerations, orientation dependence of oxidation rates, thin oxides, Oxides, Oxidation technique & systems dry & wet oxidation. Masking properties of SiO2.Diffusion: Diffusion from a chemical source in vapour form at high temperature, diffusion from doped oxide source, diffusion from an ion implanted layer.

Unit III

Lithography: Optical Lithography: optical resists, contact & proximity printing, projection printing,
electron lithography: resists, mask generation, Electron optics, roster scans & vector scans, variable beam shape.X-ray lithography: resists & printing, X ray sources & masks. Ion lithography.
Etching: Reactive plasma etching, AC & DC plasma excitation, plasma properties, chemistry & surface interactions, feature size control & anisotropic etching, ion enhanced & induced etching, properties of etch processing. Reactive Ion Beam etching, Specific etches processes: poly/polycide. Trench etching,

Unit IV

Dielectric &polysilicon film deposition: Deposition processes, Polysilicon, Silicon dioxide, silicon nitride. Diffusion: Models of diffusion in solids, Ficks one dimensional diffusion equations, atomic diffusion mechanisms, Diffusivities of B,P,As &Sb, Diffusion enhancement & retardations,

Unit V

Ion implantation, range theory, equipment, annealing, Metallization, Metallization Applications, Metallization Choices, Physical vapor Deposition, Patterning, Metallization problems.

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I Semester

EE1953	**VLSI Technology**	L= 3	T = 0	P = 0	Credits = 3

Evaluation Scheme	MSE-I	MSE-II	TA	ESE	Total	ESE Duration
	15	15	10	60	100	3 Hrs

Unit VI

VLSI Process integration, Fundamental considerations for IC processing, nMOS IC technology, CMOS IC technology, MOS memory IC technology, Bipolar IC technology, Yield & reliability, mechanism of yield loss in VLSI, modelling of yield loss mechanisms, reliability requirements for VLSI.

Resources:

1. S.M. Sze, " Modern Semiconductor Device Physics", John Wiley & Sons, 2000.
2. . B.G. Streetman, "Solid State Electronics Devices", Prentice Hall, 2002.
3. Chen,"VLSI Technology" Wiley, March 2003

I Semester

EE1954 / EE1937	Embedded System & RTOS	L= 3	T = 0	P = 0	Credits = 3

Evaluation Scheme	MSE-I	MSE-II	TA	ESE	Total	ESE Duration
	15	15	10	60	100	3 Hrs

Objective	Outcomes
• To introduce students to the embedded systems, its hardware and software, real time operating systems, inter-task communication and an exemplary case of RTOS.	1. Students will be able to understand and learn the concepts, architecture, programming, addressing modes for various embedded system. 2. Students will be acquainted with the new concepts related to design of embedded systems, introspect themselves for applying their previous knowledge for various parameters, especially, selection of operating systems, processors, controllers, memory, IO devices, etc 3. Students will be able to establish link for hardware-software interaction for embedded systems, develop build process for signal / data processing through related software and hardware set up 4. Students will be acquainted with task scheduling, interrupt mechanisms and various managements related to embedded real time operating systems, and will be able to discuss deliver presentation on contemporary issues related to system on chip and system on slice
Mapped Program Outcomes: a, c, d	

SN	Course Outcomes	Mapped PO						
		a	b	c	d	e	f	g
1	Students will be able to understand and learn the concepts, architecture, programming, addressing modes for various embedded systems	H						
2	Students will be acquainted with the new concepts related to design of embedded systems, introspect themselves for applying their previous knowledge for various parameters, especially, selection of operating systems, processors, controllers, memory, IO devices, etc	H			H			
3	Students will be able to establish link for hardware-software interaction for embedded systems, develop build process for signal / data processing through related software and hardware set up	M		H	H			
4	Students will be acquainted with task scheduling, interrupt mechanisms and various managements related to embedded real time operating systems, and will be able to discuss / deliver presentation on contemporary issues related to system on chip and system on slice				M			

Unit I:

Introduction to embedded systems, basic concepts, application areas and categories of embedded systems: Stand aloneEmbedded systems, Real Time systems, Requirements, challenges Recent trends and applications of Embedded systems.

Unit II:

New trends in hardware platforms for Embedded system design, Processor selection criteria in Embedded system design, Embedded system design with microprocessors, microcontrollers, and DSP processor.

I Semester

EE1954 / EE1937	Embedded System & RTOS	L= 3	T = 0	P = 0	Credits = 3

Evaluation Scheme	MSE-I	MSE-II	TA	ESE	Total	ESE Duration
	15	15	10	60	100	3 Hrs

Unit III:

Issues involved in choosing appropriate development platforms and tools for design of Embedded systems, development environments, operating systems, task scheduling, non real and real time operating systems

Unit IV:

Need for communication Interfaces, RS 232 communication parameters, connector configurations, UART, serial communications, Ethernet, IEEE 802.11, Bluetooth system specifications

Unit V:

Embedded Real Time Operating systems, concepts, architecture of Kernel, tasks, task scheduler, interrupt service routines, semaphores, Mutex, Mailboxes, Message queue management function calls, event register management function calls, signals and timer management function calls, memory management, priority inversion problems in design of Embedded Real Time Operating systems.

Unit VI:

Commonalities of Embedded Real Time Operating systems, Embedded operating systems –LINUX, Real Time Operating systems –RTLINUX, Concept of system on chip and system on Slice.

Resources:

1. 'Embedded / Real Time Systems – Concepts, design and programming' Dr.K.V.K.K.Prasad, (DreamTech Press), Reprint Edition, 2006
2. 'Designing Embedded Hardware', John Catsoulis, 2nd Edition, O'reilly Publication, 2005
3. 'Programming for Embedded systems – Cracking the code' DreamTech Software Team, WileyPublishingInc, 2006
4. "An Embedded Software Primer", David E. Simon, 1st Edition, Pearson Education,1999
5. "Embedded System Design", Frank Vahid, Tony Givargis, John Wiley & Sons, Inc,2002
6. "Building Embedded Linux Systems", Karim Yaghmour,2nd Edition, O'reilly,2008
7. "Programming Embedded Systems", Michael Barr, 2nd Edition, O'reilly,2006
8. "Real-time systems & software", Alan C. Shaw,3rd Edition, John Wiley & sons, Inc.2001
9. "Computers as Components", Wayne Wolf, 1st Edition, Harcourt India Pvt. Ltd., 2002

I Semester

EE1955 / EE1904	Advanced Digital System Design	L= 3	T = 0	P = 0	Credits = 3

Evaluation Scheme	MSE-I	MSE-II	TA	ESE	Total	ESE Duration
	15	15	10	60	100	3 Hrs

Objective	Outcomes
• To expose students to the advanced design techniques and methodology and industrial standard EDA tools in Digital Circuits and Systems design.	1. Graduates will be able to design and analyse combinational and sequential logic circuits. 2. Graduates will understand hardware description language and able to design and simulate digital systems using different abstraction levels. 3. Graduates will be able to understand and apply timing issues in multiple contexts and design the circuit. 4. Graduates will understand programmable devices and able to design digital systems using modern design tools.
Mapped Program Outcomes: a, c, d	

SN	Course Outcomes	Mapped PO						
		a	b	c	d	e	f	g
1	Graduates will be able to design and analyse combinational and sequential logic circuits.	H			H			
2	Graduates will understand hardware description language and able to design and simulate digital systems using different abstraction levels.	H			H			
3	Graduates will be able to understand and apply timing issues in multiple contexts and design the circuit.	L			M			
4	Graduates will understand programmable devices and able to design digital systems using modern design tools.	L		L				

Unit I

Digital Design Fundamentals, Combinational & Sequential design issues, Introduction to finite state machines, Moore & Mealy Machine, Introduction to programmable devices, PLA, PAL, PROM, Structure of CPLDs, Introduction to FPGA, Architecture, CLB, IOB, Programmable Interconnect Points, Different type of programmable switches used in PLDs.

Unit II

HDL Based Design flow, Requirements of HDL, Design Methodologies, Different Modeling styles, Introduction to Verilog, Elements of Verilog, Verilog Module definition, Elements of Module.

Unit III

Basic Concepts in Verilog, Reserved Keywords, Syntax & Semantics, Comments, Identifiers, Number Representation, System Representation, Verilog Ports, Verilog Data Types, Wire & Variables, Physical & Abstract, Constants, Parameter, Verilog Data Operators, Design entry in Verilog &Testbench, Compilation and synthesis, Timing analysis.

Unit IV

Data Flow Modeling, Delay, Continuous Assignment, Delayed Continuous assignment, Structural Modeling Feature, Module Instantiation, Gate level Primitives, Gate Delays, Switch Level Primitives, User Defined Primitives.

I Semester

EE1955 / EE1904	**Advanced Digital System Design**	L= 3	T = 0	P = 0	Credits = 3

Evaluation Scheme	MSE-I	MSE-II	TA	ESE	Total	ESE Duration
	15	15	10	60	100	3 Hrs

Unit V

Behavioral Modeling, Initial, Always, Procedural Assignment, Blocking and Non- Blocking assignments, Sequential & Parallel Blocks, Race around Condition, Timing Control, Procedural Statements, Conditional Statements if case loop repeat forever etc, Zero Delay Control, Event Based Timing Control, Compiler Directives, Assign Deassign, Force Release, Latch Models, FF Models, State Machine Coding ,Moore and Mealy Machines.

Unit VI

Combinational & sequential system Design examples like Shift Registers, Counters, LFSR, Stacks and Queues, Multi bit Adders & Multiplier, Huffman Coding, Processor and Memory Model , CPU, System Tasks and Functions, Design Verification.

Resources:

1. "Verilog Digital System Design" - ZainalabedinNavabi, Second Edition, Tata McGraw Hill, 2009
2. "Verilog HDL: A Guide to Digital Design and Synthesis", Samir Palnitkar, 2nd Edition, Prentice Hall India, 2003
3. "A Verilog HDL Primer", J. Bhaskar, 2nd Edition, Star Galaxy Press, 1997

I Semester

EE1956	Lab: Embedded System & RTOS	L= 0	T = 0	P = 2	Credits = 1

Evaluation Scheme	Continuous Evaluation	ESE	Total	ESE Duration
	40	60	100	

Objective	Outcomes
1. To introduce the difference between embedded systems and general purpose systems 2. To introduce different peripheral interfaces to embedded systems. 3. To become familiar with programming environment used to develop embedded system 4. To apply knowledge gained in software-hardware integration in team-based projects.	1. Students will be able to learn different embedded system designing tools 2. Students will be able to design, test and critically evaluate embedded solutions to real world situations using digital components (sequential and combinatorial).
Mapped Program Outcomes: a, c	

SN	Course Outcomes	Mapped PO						
		a	b	c	d	e	f	g
1	Students will be able to learn different embedded system designing tools	M		H				
2	Students will be able to design, test and critically evaluate embedded solutions to real world situations using digital components (sequential and combinatorial).	H		H				

Practical based on Syllabus of **Embedded System & RTOS**

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I Semester

EE1957/ EE1907	Lab : Digital IC Design	L= 0	T = 0	P = 2	Credits = 1
Evaluation Scheme	Continuous Evaluation	ESE	Total	ESE Duration	
	40	60	100		

Objective	Outcomes
To design & analyze the performance of MOS circuits	1. Graduates will able to design layout of basic gates, combinational & sequential logic circuits for the given technology using EDA tools 2. Graduates will able to optimize complex circuits 3. Graduate will be able to apply lambda/micron rules for designing layout
Mapped Program Outcomes: c, d, e, f	

SN	Course Outcomes	Mapped PO						
		a	b	c	d	e	f	g
1	Graduates will able to design layout of basic gates, combinational & sequential logic circuits for the given technology using EDA tools			H	H	H	H	
2	Graduates will able to optimize complex circuits			H	H	H	H	
	Graduate will be able to apply lambda/micron rules for designing layout			H	H	H	H	

SN	Name of Experiment	Mapping with CO
1.	a) Plot current voltage characteristics of nmos transistor using 0.5 micron technology b) Plot current voltage characteristics of PMOS transistor using 0.5 micron technology	CO1,CO3
2.	To design and simulate CMOS inverter using 0.5 micron technology	CO1,CO3
3.	Plot transfer characteristics of pseudo-nmos inverter with w/l for pmos is equal to twice w/l of nmos.	CO1,CO2,CO3
4.	Design and simulate two input CMOS NAND gate	CO1,CO2,CO3
5.	Design two input CMOS NOR gate.	CO1,CO2,CO3
6.	Design CMOS transmission gate.	CO1,CO2,CO3
7.	Design and simulate D-Latch using transmission gate	CO1,CO2,CO3
8.	Design 2:1 MUX using transmission gate	CO1,CO2,CO3
9.	Design two input CMOS XOR gate	CO1,CO2,CO3
10.	Design function f=not(A+B+C+D) using Euler path approach	CO1,CO2,CO3

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I Semester

EE1958/ EE1908	**Lab: Advanced Digital System Design**	L= 0	T = 0	P = 2	Credits = 1

Evaluation Scheme	Continuous Evaluation	ESE	Total	ESE Duration
	40	60	100	

Objective	Outcomes
To learn front end Digital System design flow.	1. Graduates will be able to design, simulate and synthesize digital systems using Modern digital system design tools. 2. Graduates will be able to apply timing issues in multiple contexts.
Mapped Program Outcomes: c, d, e, f	

SN	Course Outcomes	Mapped PO						
		a	b	c	d	e	f	**g**
1.	Graduates will be able to design, simulate and synthesize digital systems using Modern digital system design tools.			H		H	H	
2.	Graduates will be able to apply timing issues in multiple contexts.				H	M	H	

Sr. No	**Name of Experiment**
1	Verilog Code using Bitwise Operator .Test it with test stimuli generated by test bench.[CO1(H),CO2(H)]
2	Using GATE level primitive write verilog code and test it with test stimuli generated by test bench. [CO1(H),CO2(H)]
3	Verilog code using DATA flow modeling style. Test it with test stimuli generated by test bench. [CO1(H),CO2(H)]
4	Write verilog code using conditional assignment statement. Test it with test stimuli generated by test bench. [CO1(H),CO2(H)]
5	Write verilog code using Structural Modeling style. Test it with test stimuli generated by test bench. [CO1(H),CO2(H)]
6	Verilog code using Behavioral modeling style. Test it with test stimuli generated by test bench. [CO1(H),CO2(H)]
7	Write UDP for A. Combinational Circuit B.Sequential circuit [CO1(H),CO2(H)]
8	Write verilog code using switch level modeling for a. NAND gate b. Full adder using transmission gate [CO1(H),CO2(H)]
9	Write verilog code using while loop. [CO1(H),CO2(H)]
10	Write verilog code for Mealy and Moore sequence detector.(using overlapping allowed and not allowed). [CO1(H),CO2(H)]
11	Mini Project[CO1(H),CO2(H)]

II Semester

EE 1961 / EE1911	RF Circuit Design	L= 3	T = 0	P = 0	Credits = 3

Evaluation Scheme	MSE-I	MSE-II	TA	ESE	Total	ESE Duration
	15	15	10	60	100	3 Hrs

Objective	Outcomes
• To study RF component such as resonator, filter, transmission lines, etc • To learn design of RF amplifiers using transistors	1. Graduates will have an ability to demonstrate in- depth knowledge of general RF circuits, components and systems and an understanding of resonant circuits 2. Graduates will be able to understand and use Smith Chart for developing circuits in RF applications. 3. Graduates will be able to design impedance matching networks, passive RF filters and RF power amplifiers.
Mapped Program Outcomes: a, d	

SN	Course Outcomes	Mapped PO						
		a	b	c	d	e	f	g
1	Graduates will have an ability to demonstrate in- depth knowledge of general RF circuits, components and systems and an understanding of resonant circuits	H			L			
2	Graduates will be able to understand and use Smith Chart for developing circuits in RF applications.	M			H			
3	Graduates will be able to design impedance matching networks, passive RF filters and RF power amplifiers.				H			

Unit I

Introduction, Importance of Radio frequency Design, RF Behaviour of Passive Components, Chip Components, Transmission Line Analysis, Equivalent Circuit Representation, Circuit Parameters for a Parallel Plate Transmission Line, Microstrip Transmission Line, Terminated Lossless Transmission Line, Special Termination Conditions, Sourced and Loaded Transmission Line.

Unit II

The Smith Chart, From Reflection Coefficient to Load Impedance, Impedance Transformation, Admittance, Transformation, Parallel and Series Connections, Single- and Multiport Networks, Interconnecting Networks, Network Properties and Applications, Scattering Parameters.

Unit III

An Overview of RF Filter Design, Basic Resonator and Filter Configurations, Special Filter Realizations, Filter Implementation, Coupled Filter.

Unit IV

Matching and Biasing Networks: Impedance Matching Using Discrete Components, Microstrip Line Matching Networks, Amplifier Classes of Operation and Biasing Networks.

Unit V

RF Transistor Amplifier Designs: Characteristics of Amplifiers, Amplifier Power Relations, Stability Considerations, Constant Gain, Noise Figure Circles, Constant VSWR Circles, Broadband, High-Power, and Multistage Amplifiers

Unit VI

Oscillators, Basic Oscillator Model, High-Frequency Oscillator Configuration, Oscillators describing functions, Colpitt's oscillators Resonators, Tuned Oscillators, Negative resistance oscillators, Phase noise Basic Characteristics of Mixers. Non-linear based mixers, Quadratic mixers, Multiplier based mixers,Single balanced and double balanced mixers, sub sampling mixers.

Resources:

1. "RF Circuit Design – Theory and Applications", Reinhold Luduig and PavelBretchko, 2nd Edition, Pearson Education, 2000.
2. T.Lee, "Design of CMOS RF Integrated Circuits", Cambridge, 2004.
3. B.Razavi, "RF Microelectronics", Pearson Education, 1997.
4. B.Razavi, "Design of Analog CMOS Integrated Circuits", McGraw Hill, 2001

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II Semester

EE1962/EE1916	Analog IC Design	L= 3	T = 0	P = 0	Credits = 3

Evaluation Scheme	MSE-I	MSE-II	TA	ESE	Total	ESE Duration
	15	15	10	60	100	3 Hrs

Objective	Outcomes
To understand the functions of various digital and analog ICs and their applications in the design of electronic circuits.	1. Graduates will able to demonstrate behaviour of single, multiple transistor amplifiers. 2. Graduates will able to Solve complex circuit problems 3. Graduates will able to model integrated circuit devices 4. Graduates will be able to design nonlinear analog circuits.
Mapped Program Outcomes: a,d	

SN	Course Outcomes	Mapped PO						
		a	b	c	d	e	f	g
1	Graduates will able to demonstrate behaviour of single, multiple transistor amplifiers.	H			M			
2	Graduates will able to Solve complex circuit problems				H			
3	Graduates will able to model integrated circuit devices	H			M			
4	Graduates will be able to design nonlinear analog circuits.				L			

Unit I: Models for integrated circuit active devices:

Depletion region of a p-n junction, Small Signal & large signal behavior of MOS & BJT transistor, short channel effects in MOS transistors, weak inversion in MOS transistor, substrate current in MOS transistor

Unit II: Single transistor and multiple transistor amplifiers:

Basic Single transistor Amplifiers stages: Common Emitter, Common base, Common Collector, Common Drain, Common Gate & Common Source Amplifiers, Multiple Transistor Amplifier stages: CC-CE, CC-CC, & Darlington configuration, Cascode configuration, Active Cascode, Super source follower, Differential pairs, DC transfer characteristics.

Unit III: Current Mirrors, Active Loads & References:

Current Mirrors: Simple current mirror, Cascode current mirrors, Widlar current mirror, Wilson Current mirror, Active loads, Voltage & current references, supply and temperature independent biasing techniques

Unit IV: Operational Amplifier with single ended outputs:

Deviations from ideality in real operational amplifiers, Basic two stage op amp, two stage MOS Operational Amplifier with cascodes, MOS telescopic-cascode operational amplifiers, MOS Folded-cascode operational amplifiers, MOS active cascade operational amplifiers, Bipolar operational amplifiers

Unit V: Frequency response of integrated circuits:

Single stage amplifiers & miller effect, MOS differential amplifier differential mode gain, frequency response of the common mode gain for a differential amplifier, frequency response of voltage buffers, frequency response of current buffers, Multistage amplifier frequency response, frequency response of a current mirror loading a differential pair.

Unit VI: Nonlinear Analog Circuits:

Analysis of four quadrants, Gilbert cell as an analog multiplier, Phase Locked Loops, Integrated circuit phase locked loops, Voltage controlled oscillators, Switched Capacitor Circuits and Switched Capacitor Filters.

Resources:

1. "Analysis and Design of Analog Integrated Circuits", Paul B Gray ,hurst ,Lewis, Meyer ,fifth edition, John Wiley & sons, reprint 2010.
2. "CMOS Analog Circuit Design"P.E.Allen,D.R.Holdberg,secondedition,Oxforduniv. press.2010
3. "CMOS circuit design, Layout, and simulation" R.Jacob Baker, second edition, Wiley student edition, reprint 2009

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Nagar Yuwak Shikshan Sanstha's

Yeshwantrao Chavan College of Engineering

(An Autonomous Institution affiliated to Rashtrasant Tukadoji Maharaj Nagpur University)

M. Tech. SoE and Syllabus 2014

VLSI DESIGN

II Semester

EE1963	**Synthesis & Optimization of VLSI Circuits**	L= 3	T = 0	P = 0	Credits = 3

Evaluation Scheme	MSE-I	MSE-II	TA	ESE	Total	ESE Duration
	15	15	10	60	100	3 Hrs

Objective	**Outcomes**
• The objective of this course is to acquaint concept of Optimization of Very Large Scale Integration (VLSI) circuit and. systems design	At the end of this course, students will 1. Understand basic Boolean functions, their representations and different CAD based synthesis and optimization issues. 2. Understand, able to analyze and solve the algorithms which underpin behavioral synthesis including scheduling, allocation and binding. 3. Understand and able to analyze high level synthesis issues, two level logic optimization, multilevel logic optimization, and sequential logic optimization. 4. Understand and able to apply the Satisfiability (SAT) concept.
Mapped Program Outcomes: a,b,d	

SN	Course Outcomes	Mapped PO						
		a	b	c	d	e	f	g
1	Understand basic Boolean functions, their representations and different CAD based synthesis and optimization issues.	H	M		M			
2	Understand, able to analyze and solve the algorithms which underpin behavioral synthesis including scheduling, allocation and binding.	H						
3	Understand and able to analyze high level synthesis issues, two level logic optimization, multilevel logic optimization, and sequential logic optimization.	H	M		M			
4	Understand and able to apply the Satisfiability (SAT) concept.	H						

Unit I

Microelectronics, Semiconductor technologies and circuit taxonomy, Microelectronic design styles, Computer aided synthesis and optimization. Graphs Notation, Undirected graphs, Directed graphs, Combinatorial optimization, Algorithms, Tractable and intractable problems Graph optimization problems and algorithms, Boolean algebra and Applications.

Unit II

Hardware Modeling Languages, Distinctive features, Structural hardware language, Behavioral hardware language, HDLs used in synthesis, Abstract models, Structures logic networks, State diagrams, Data flow and sequencing graphs, Compilation and optimization techniques.

Unit III

Logic optimization, principles, Operation on two level logic covers, Algorithms for logic minimization, Symbolic minimization and encoding property, Minimization of Boolean relations. Multiple level combinational optimizations, Models and transformations

Unit IV

Combinational networks, Algebraic model, Synthesis of testable network, Algorithm for delay evaluation and optimization, Rule based system for logic optimization. Sequential circuit optimization, Sequential circuit optimization using state based models, Sequential circuit optimization using network models.

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II Semester

EE1963	**Synthesis & Optimization of VLSI Circuits**	L= 3	T = 0	P = 0	Credits = 3

Evaluation Scheme	MSE-I	MSE-II	TA	ESE	Total	ESE Duration
	15	15	10	60	100	3 Hrs

Unit V

A model for scheduling problems, Scheduling with resource and without resource constraints, Scheduling algorithms for extended sequencing models, Scheduling Pipe lined circuits. Cell library binding, Problem formulation and analysis, Algorithms for library binding, Specific problems and algorithms for library binding (lookup table F.P.G.As and Antifuse based F.P.G.As), Rule based library binding.

Unit VI

Ongoing work in logic Synthesis, Speedup Algorithms Design Reuse, Domain Specific Synthesis, Testability, Future role of Logic Synthesis

Resources:

1 "Synthesis and Optimization of Digital Circuits" ,Giovanni De Micheli, 1st Edition, Tata McGraw-Hill, 2003.
2. "Logic Synthesis" SrinivasDevadas, AbhijitGhosh, and Kurt Keutzer,1st Edition, McGraw-Hill, USA, 1994.
3. "Principles of CMOS VLSI Design: A System Perspective",NeilWeste and K. Eshragian, 2nd edition,Pearson Education,2000.
4. "VHDL for Programmable Logic," Kevin Skahill, 1st Edition, Pearson Education, 2000.

II Semester

EE1966 / EE1918	Low Power CMOS VLSI Design	L= 3	T = 0	P = 0	Credits = 3

Evaluation Scheme	MSE-I	MSE-II	TA	ESE	Total	ESE Duration
	15	15	10	60	100	3 Hrs

Objective	Outcomes
• To acquaint students with principles of design , analysis , modelling and optimization of low power VLSI , as well as to promote an interest in VLSI design	1. Graduates will understand the concepts of sources of power dissipation and basics of CMOS Physics. 2. Graduates will understand the concepts of levels of abstraction and its power dissipation. 3. Graduates will understand the Power Optimization methods at Behaviour, Logic and Circuit Level design. 4. Graduates will understand the challenges in deep submicron technology. 5. Graduates will understand the principles for low power designs, and have the capabilities to analyze power consumption and develop low power strategies for a given system.
Mapped Program Outcomes: a,b,d	

SN	Course Outcomes	Mapped PO						
		a	b	c	d	e	f	g
1	Graduates will understand the concepts of sources of power dissipation and basics of CMOS Physics.	M	L					
2	Graduates will understand the concepts of levels of abstraction and its power dissipation.	M	M					
3	Graduates will understand the Power Optimization methods at Behavior, Logic and Circuit Level design.	M	L		H			
4	Graduates will understand the challenges in deep submicron technology.	M	M		H			
5	Graduates will understand the principles for low power designs, and have the capabilities to analyze power consumption and develop low power strategies for a given system.	M	M		H			

Unit I

Need for low power VLSI chips, Sources of power dissipation: Short circuit dissipation, dynamic dissipation, designing Techniques for low power. Physics of power dissipation in MOSFET devices, MOS Capacitance analysis, low power figure of merits, brief overview of low power VLSI design limits.

Unit II

Probabilistic power analysis: random logic signals, probability and frequency, probabilistic power analysis techniques, signal entropy, Low power circuits: transistor and gate sizing, equivalent pin ordering, network reconstruction and reorganization, Glitching Power, special latches and flip-flops.

Unit III

Behavioural, Logic and circuit level approaches. Algorithm level transforms. Circuit activity driven architectural transformations, voltage scaling, operation reduction and substitution, pre-computation, Logic: gate reorganization, signal gating, logic encoding, state machine encoding.

Unit IV

Design style, Leakage current in Deep sub-micron transistors, device design issues, minimizing short channel effect. Low voltage design techniques using reverse Vgs. Steep sub threshold swing and multiple threshold voltages. Multiple threshold CMOS based on path critically, multiple supply voltages.

II Semester

EE1966 / EE1918	**Low Power CMOS VLSI Design**	L= 3	T = 0	P = 0	Credits = 3

Evaluation Scheme	MSE-I	MSE-II	TA	ESE	Total	ESE Duration
	15	15	10	60	100	3 Hrs

Unit V

Low energy computing, Energy dissipation in transistor channel. Energy recovery circuit design, designs with reversible and partially reversible logic, energy recovery in adiabatic logic and SRAM core, Design of peripheral circuits – address decoder, level shifter and IO Buffer, supply clock generation.

Unit VI

Introduction, sources of software power dissipation, power estimation and optimization. Co-design for low power**.**

Resources:

1. "Solid State Electronic Devices", 6th Edition, Ben Streetman, Sanjay Benerjee.
2. "Low-Power CMOS VLSI Circuit Design", Kaushik Roy, Sharat C. Prasad, 1st Edition, Wiley India,2009
3. "Practical Low Power Digital VLSI Design", Gary K. Yeap, Kluwer Academic Publisher, 2002
4. "Low-Power CMOS Circuits-Technology, Logic Design and CAD Tools" Christian Piguet, 2006 by Taylor & Francis Group, LLC
5. "Energy Efficient Microprocessor Design", T. D. Burd and R. A. Brodersen, Boston: Springer, 2002.
6. "Low-Power Digital CMOS Design", A. Chandrakasan and R. Brodersen, Boston: Springer, 1995.
7. "Digital Integrated Circuits: A Design Perspective", 2nd ed., J. Rabaey, A. Chandrakasan, B. Nikolic.

II Semester

EE1967	Hardware Software Codesign	L= 3	T = 0	P = 0	Credits = 3

Evaluation Scheme	MSE-I	MSE-II	TA	ESE	Total	ESE Duration
	15	15	10	60	100	3 Hrs

Objective	Outcomes
To educate the hardware, software, and system designer on the fundamentals of hardware/software codesign in a manner that will assist him/her in understanding and employing cooperative hardware/software design techniques for the construction of complex systems, particularly embedded systems.	1. Graduates will understand the Models for describing hardware and software components (specification) 2. Graduates will understand the System design (hardware-software partitioning and design space exploration) 3. Graduates will understand Performance analysis and estimation techniques
Mapped Program Outcomes: a	

SN	Course Outcomes	Mapped PO						
		a	b	c	d	e	f	g
1	Graduates will understand the Models for describing hardware and software components (specification)	H						
2	Graduates will understand the System design (hardware-software partitioning and design space exploration)	H						
3	Graduates will understand Performance analysis and estimation techniques	H						

Unit I

Introducing Hardware/Software Codesign, The Quest for Energy Efficiency, The Driving Factors in Hardware/Software Codesign, The Hardware-Software Codesign Space, The Dualism of Hardware Design and Software Design, Modeling Abstraction Level, Concurrency and Parallelism, Introducing Data Flow Graphs, Analyzing Synchronous Data Flow Graphs, Control Flow Modeling and the Limitations of Data Flow Models, Adding Time and Resources, Transformations

Unit II

Software and Hardware Implementation of Data Flow, Hardware/Software Implementation of Data Flow, Data and Control Edges of a C Program, Implementing Data and Control Edges, Construction of the Control Flow Graph, Construction of the Data Flow Graph, Application: Translating C to Hardware, Single-Assignment Programs

Unit III

Finite State Machine with Datapath, Hardware Modules, Finite State Machines, Finite State Machines with Datapath, FSMD Design Example: A Median Processor, Proper FSMD,Language Mapping for FSMD by Example, Limitations of Finite State Machines, Microprogrammed Control, Micro-instruction Encoding, The Micro-programmed Datapath, Implementing a Micro-programmed Machine, Micro-program Interpreters, Micro-program Pipelining

Unit IV

General-Purpose Embedded Cores: Processors, The RISC Pipeline, Program Organization, Compiler Tools, Low-Level Program Analysis, Processor Simulation, The System-on-Chip Concept, Four Design Principles in SoC Architecture, Example: Portable Multimedia System, SoC Modeling in GEZEL

Unit V

Connecting Hardware and Software, Synchronization Schemes, Communication-Constrained Versus Computation-Constrained, Tight and Loose Coupling, On-Chip Bus Systems, Bus Transfers, Multi-master Bus Systems, Bus Topologies

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II Semester

EE1967	**Hardware Software Codesign**	L= 3	T = 0	P = 0	Credits = 3

Evaluation Scheme	MSE-I	MSE-II	TA	ESE	Total	ESE Duration
	15	15	10	60	100	3 Hrs

Unit VI

Microprocessor Interfaces: Memory-Mapped Interfaces, Coprocessor Interfaces, Custom-Instruction Interfaces, Hardware Interfaces: The Coprocessor Hardware Interface, Data Design, Control Design, Programmer's Model = Control Design + Data Design

Resources:

1. "A Practical Introduction to Hardware/Software Codesign" By Patrick R. Schaumont , Second Edition, Springer New York Heidelberg Dordrecht London,2013
2. "Readings in Hardware/software Co-design"**By Giovanni De Micheli,**Morgan Kaufmann, 2002
3. "The Co-design of Embedded Systems: A Unified Hardware Software Representation", Sanjaya Kumar, James H. Ayler , Kluwer Academic Publisher, 2002
4. "Co-synthesis of Hardware and Software for Embedded Systems",R.Gupta, Kluwer Publications, 1995.

II Semester

EE1968	Nano Scale MOS Transistors	L= 3	T = 0	P = 0	Credits = 3

Evaluation Scheme	MSE-I	MSE-II	TA	ESE	Total	ESE Duration
	15	15	10	60	100	3 Hrs

Objective	Outcomes
• To understand the necessary of scaling of MOS transistor. • To introduce the concepts of nano scale MOS transistor concepts and their performance characteristics. • To study the various nano scaled MOS transistors.	1. Graduates will be able to apply knowledge from undergraduate engineering and other disciplines to identify, formulate and present solutions to technical problems in various engineering fields related to VLSI design and technology. 2. Graduates will be able to learn advanced technologies in the fields of VLSI design along with the fundamental concepts. 3. Graduates will be to understand multigate CMOS in detail 4. Graduate will be able to understand scaling effects and multigate circuit design.
Mapped Program Outcomes: a,c,d	

SN	Course Outcomes	Mapped PO						
		a	b	c	d	e	f	g
1	Graduates will be able to apply knowledge from undergraduate engineering and other disciplines to identify, formulate and present solutions to technical problems in various engineering fields related to VLSI design and technology.	H		H	H			
2	Graduates will be able to learn advanced technologies in the fields of VLSI design along with the fundamental concepts.	H		M	M			
3	Graduates will be to understand multigate CMOS in detail	H		L	L			
4	Graduate will be able to understand scaling effects and multigate circuit design	H		M	L			

UNIT I: Basics of MOSFETs:
MOSFET scaling, Short channel effects, Channel engineering , Source/Drain Engineering, High k dielectric, Copper interconnects, Strain engineering ,SOI MOSFET Physics, Classical Physics, Quantum Effects

UNIT II: Multigate Technology:
Active Area, Gate Stack, Source/ Drain Resistance and Capacitance, Mobility and Strain Engineering, Contacts to Fins

UNIT III: Compact Models for Multi-Gate Transistors:
Framework for multigate FET Modelling, Multigate Models: BSIM-CMG and BSIM-IMG, Core Models, Modelling Physical Effects of Real Devices

UNIT-IV: Physics of Multigate MOS System:
Device electrostatics, Double Gate MOS System, Double Gate MOSFETs and FinFETs, Silicon Multiple Gate Nanowires

UNIT V: Radiation Effects in MOSFETs:
Brief history of radiation effects in SOI, Total Ionizing Dose Effects, Single Event Effects, Scaling Effects

UNIT-VI: Multigate MOSFET Circuit Design:
Impact of Device Performance on Digital Circuit Design, Analog Circuit Design, Device Figure of Merit, Mixed Signal Aspects, RF Circuit Design Aspects.

Resources:
1. J P Colinge, FINFETs and other multi-gate transistors, Springer – Series on integrated circuits and systems, 2008
2. Mark Lundstrom Jing Guo, Nanoscale Transistors: Device Physics, Modeling and Simulation, Springer, 2006.
3. M S Lundstorm, Fundamentals of Carrier Transport, 2nd Ed., Cambridge University Press, Cambridge UK, 2000

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II Semester

EE1969/ EE1921	Verification & Testing of VLSI Circuits	L= 3	T = 0	P = 0	Credits = 3

Evaluation Scheme	MSE-I	MSE-II	TA	ESE	Total	ESE Duration
	15	15	10	60	100	3 Hrs

Objective	Outcomes
• To gain a knowledge from the area of applying diagnostic principles in the design of modern Electronic systems.	1. Students develop an understanding of VLSI design verification and testing issues. 2. Students learn how to generate test patterns for faults in a system and how to design a system for testability. 3. Ability to model different faults and carry out fault simulation in digital circuits. 4. Ability to know about importance of testing and its types in VLSI circuits.
Mapped Program Outcomes: a,d	

SN	Course Outcomes	Mapped PO						
		a	b	c	d	e	f	g
1	Students develop an understanding of VLSI design verification and testing issues.	M						
2	Students learn how to generate test patterns for faults in a system and how to design a system for testability.	M			H			
3	Ability to model different faults and carry out fault simulation in digital circuits.				H			
4	Ability to know about importance of testing and its types in VLSI circuits.				M			

Unit – I

Overview Of Testing**:** Design Process, Verification, Faults & Their Detection, Test Pattern Generation, Fault Coverage, Types Of Tests, Test Application, Testing Economics. Defects, Failures, and Faults: Physical Defects, Failures Modes, Faults, Fault Equivalence and Dominance, Fault Collapsing

Unit – II

Design Representation: Graphical representation, Graphs, Binary Decision diagrams, Netlists, VLSI Design Flow: CAD tools, Design Methodologies, Semicustom Design

Unit - III

Simulation: Logic Simulation, Approaches to Simulation, Fault Simulation & Their Results. Automatic Test Pattern Generation: D-Algorithm, Critical Path Extensions to D-Algorithm PODEM, FAN

Unit - IV

Ad Hoc Techniques, Scan–Path Design, Test pattern generation, Test Pattern Application, Scan architectures, multiple scan chains, Partial Scan Testing

Unit - V

Boundary-Scan Testing: Boundary Scans Architecture, Test Access Port, Registers, Tap Controller, Modes of Operation. Built In Self Test: Pseudorandom Test Pattern Generation, Response Compaction, BIST Architectures

Unit - VI

Memory Testing: Types of Memory Testing, Functional Testing Schemes, Testing FPGAs and Microprocessors: Testability Of FPGAs, Testing RAM- Based FPGAs, Testing Microprocessors, Synthesis For Testability.

Resources:

1. "Principles of Testing Electronic Systems", 2nd edition SamihaMourad, YervantZorian
2. "Essentials of Electronic Testing for Digital, Memory, and Mixed-Signal VLSI Circuits",Michael L. Bushnell and Vishwani D. Agrawal, B.S.Publications, 2000
3. "Digital Systems Testing and Testable Design" ,MironAbramovici, Melvin Breuer and Arthur Friedman, IEEE press,
4. "A Guide to VHDL" by Stanley Mazor,2nd Edition, Kluwer Academic Press, 2007
5. "HDL Chip Design" by Douglas Smith, 3rd Edition, Doone Publications, 2008
6. "Rapid Prototyping of Digital Systems", by J. O. Hamblen and M. Furman, Kluwer Academic Publishers.2001

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II Semester

EE1970/EE1913	Digital Image Processing	L= 3	T = 0	P = 0	Credits = 3

Evaluation Scheme	MSE-I	MSE-II	TA	ESE	Total	ESE Duration
	15	15	10	60	100	3 Hrs

Objective	Outcomes
• Provide deeper knowledge of theoretically demanding methods of image data processing and of their applications.	1. Graduates will be able to demonstrate the understanding of fundamentals of Digital image processing wrt to enhancement, filtering, segmentation, restoration & representation 2. Graduates will able to understand the mathematical implementation & interpretation of image transforms 3. Graduates will be able to formulate solutions to general image processing problems 4. Graduates will be able to develop skill base necessary to further explore advanced topics of Digital Image Processing for research
Mapped Program Outcomes: a,c,d	

SN	Course Outcomes	Mapped PO						
		a	b	c	d	e	f	g
1	Demonstrate the understanding of fundamentals of Digital image processing wrt to enhancement, filtering, segmentation, restoration & representation	H		M	M			
2	Able to understand the mathematical implementation & interpretation of image transforms	H		M	M			
3	be able to formulate solutions to general image processing problems	H		M	M			
4	develop skill base necessary to further explore advanced topics of Digital Image Processing for research	M		M	M			

Unit I

An image model – sampling & quantization – basic relation between pixels: imaging geometry, Properties of 2-D Fourier transforms, FFT algorithm and other separable image transforms, Walsh transforms, Hadamard, Cosine, Haar, Slant Transforms, KL Transforms and their properties, Wavelets.

Unit II

Spatial domain methods, Frequency domain methods, Histogram Modification technique, Neighbourhood averaging, Median filtering, Low pass filtering, Averaging of Multiple Images, Image sharpening by differentiation, High pass Filtering,

Unit III

Degradation model for Continuous functions, Discrete Formulation, Diagonalization of Circulant and Block – Circulant Matrices, Effects of Diagonalization, Constrained and unconstrained Restorations Inverse filtering, Wiener Filter, Constrained least Square Restoration.

Unit IV

Fundamentals, Image compression models, error free compression, lossy compression, image compression standards Objective an subjective Fidelity Criteria, the encoding process, the Mapping, the Quantizer and the Coder, Contour Encoding, Run length Encoding, Image Encoding relative to a Fidelity Criterion, Differential Pulse Code Modulation, Transform Encoding.

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II Semester

EE1970/EE1913	**Digital Image Processing**	L= 3	T = 0	P = 0	Credits = 3

Evaluation Scheme	MSE-I	MSE-II	TA	ESE	Total	ESE Duration
	15	15	10	60	100	3 Hrs

Unit V

The detection of Discontinuities, Point Line and Edge Detections, Gradient Operators, Combined Detection, Image segmentation Thresholding. Region oriented segmentation Representation Schemes, Chain Codes, Polygon Approximation, Boundary Descriptors, Simple Descriptors, Shape Numbers, Fourier Descriptors Dilation and erosion, opening and closing hit-or-miss transformation, morphological algorithms, extension to gray scale images.

Unit VI

Color Image Processing: Color Fundamentals, color models, Pseudocolor image processing, Basics of full color image processing, Color transformations, Smoothing and sharpening, Color segmentation, Noise in color images,

Resources:

1. "Digital Image Processing", Gonzalez RC & Woods RE, 2nd Edition ,Addison Wesley Publishing Company,2002
2. "Fundamentals of Digital Image Processing" ,3rd Edition, Jain AK, Printice Hall of India, 1989
3. "Digital Image Processing", Pratt William K., 4thEdition,John Wiley & Sons 2000.

II Semester

EE1971	**Solid State Devices & Modeling**	L= 3	T = 0	P = 0	Credits = 3

Evaluation Scheme	MSE-I	MSE-II	TA	ESE	Total	ESE Duration
	15	15	10	60	100	3 Hrs

Objective	**Outcomes**
• To have fundamental knowledge about structure of devices, VI characteristics of devices like PN Junction diode, Zener diode, MOSFET, BJT and Opto electronic.	1. Graduates will be able to learn advanced technologies in the fields of VLSI design along with the fundamental concepts. 2. Graduates will be able to understand and design advanced VLSI based system 3. Graduates will be able to understand the use of diodes and FET in VLSI field 4. Graduates will be able to understand the use of Lasers in VLSI field
Mapped Program Outcomes: a,c,d	

SN	**Course Outcomes**	**Mapped PO**						
		a	**b**	**c**	**d**	**e**	**f**	**g**
1	Graduates will be able to learn advanced technologies in the fields of VLSI design along with the fundamental concepts.	H		H	H			
2	Graduates will be able to understand and design advanced VLSI based system	H		H	H			
3	Graduates will be able to understand the use of diodes and FET in VLSI field	H		H	H			
4	Graduates will be able to understand the use of Lasers in VLSI field			M				

Unit I:

Semi-conductor materials- Crystal lattices, bulk crystal growth, epitaxial growth, Physical models-bohr model, quantum mechanics, atomic structure, energy bands & charge carriers in semiconductors, carrier concentration, drift of carriers in electric and magnetic fields, diffusion of carriers.

Unit II:

Fabrication of P-N junctions, equilibrium conditions, forward and reverse biased junctions, steady state conditions, reverse bias breakdown, transient and a.c. condition, deviation from simple theory, metal semi-conductor junction, heterojunction

Unit III:

P-N junction diodes, tunnel diode, photo diode, light emitting diodes and lasers. BJTs: amplification & switching: Fundamental of BJT operation, BJT fabrication, minority carrier distribution & terminal currents, generalized biasing, switching, frequency limitation of transistors, heterojuction bipolar transistor. Modeling of Diode and BJT and study their parameters.

Unit IV:

FETs: Junction FET-metal semi-conductor FET-Metal insulator semiconductor FET, Integrated circuits: fabrication of monolithic circuits, monolithic device elements. MOS Devices Modeling and study the MOS devices parameters. Study of various MOSFET model levels from level 1 to BSIM and other advance technologies.

Unit V:

Charge transfers devices, very large scale integration, testing, bonding and packaging.

Unit VI:

Lasers: stimulated emission: ruby lasers, semi-conductor lasers, other lasers, p-n-p-n switching devices, switching mechanism: semiconductor controller rectifier, negative conductance, Microwave devices: Transit time devices: Gunn effect and related devices.

Resources:

1. "Solid State Electronic Devices", Ben G Steetman , 6th Edition, Prentice Hall of India, 2008
2. "Physics of semiconductor Devices",S M Sze, 2nd Edition, Willey Publications,2007
3. "Introduction to Solid State Physics", Kittel C, 8th Edition,Willey Publications, 2008
4. "YannisTisividi s (Oxford), The MOS Transistor (2nd edition)
5. "MOSFET MODELING FOR VLSI SIMULATION: Theory and Practice, World Scientific, 01-Jan-2007

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II Semester

EE1964	Lab: RF Circuit design	L= 0	T = 0	P = 2	Credits = 1

Evaluation Scheme	Continuous Evaluation	ESE	Total	ESE Duration
	40	60	100	

Objective	Outcomes
• To study RF component such as resonator, filter, transmission lines, etc • To learn design of RF amplifiers using transistors	1. Graduates will able to Understand and use smith chart for developing circuits in RF applications 2. Graduates will be able to design impedance matching networks, passive RF filters and RF filters and RF power amplifiers 3. Graduate will be able to use CAD tools for RF circuit design.
Mapped Program Outcomes: c,d,e,f	

SN	Course Outcomes	Mapped PO						
		a	b	c	d	e	f	g
1	Graduates will able to Understand and use smith chart for developing circuits in RF applications				H	H	H	
2	Graduates will be able to design impedance matching networks, passive RF filters and RF filters and RF power amplifiers				H	H	H	
3	Graduate will be able to use CAD tools for RF circuit design			M		H	H	

Sr. No	Name of Experiment	Mapping with CO	
1	To find impedances of different resonant circuits.	CO1[M], CO2[M]	CO3[S]
2	To find input impedance of a short circuited transmission line.	CO1[M], CO2[M]	CO3[S]
3	To determine input impedance of transmission line using smith chart.	CO1[M], CO2[M]	CO3[S]
4	Design of T- matched network.	CO3[S]	CO3[S]
5	Design of π- matched network.	CO3[S]	CO3[S]
6	Design of low p ss filter and high pass filter.	CO3[S]	CO3[S]
7	Design of band pass filter and band reject filter.	CO3[S]	CO3[S]
8	Design of tapped capacitor and tapped inductor network.	CO3[S]	CO3[S]
9	Design of double tapped resonator network.	CO3[S]	CO3[S]
10	Design of high power amplifier as per the specifications.	CO3[S]	CO3[S]
11	Design of Low noise amplifier as per the specifications.	CO3[S]	CO3[S]
12	Design of Dual stage transistor amplifier.	CO3[S]	CO3[S]

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II Semester

EE1965	Lab: Analog IC Design	L= 0	T = 0	P = 2	Credits = 1

Evaluation Scheme	Continuous Evaluation	ESE	Total	ESE Duration
	40	60	100	

Objective	Outcomes
To understand the concept of various analog circuits and its design using SPICE	1. Graduate will be able to write SPICE programme for the given technology 2. Graduate will be able to understand technology parameters depending on level of transistor 3. Graduate will be able to use CAD tools

SN	Course Outcomes	Mapped PO						
		a	b	c	d	e	f	g
1	Graduate will be able to write SPICE programme for the given technology	H						
2	Graduate will be able to understand technology parameters depending on level of transistor			M				
3	G Graduate will be able to use CAD tools				H			

SN	Name of Experiment	Mapping with CO
1.	Design the complete small signal model for an NMOS transistor with NA=5×10^{15} atoms/cm^3. Device parameters are Φf=0.3 volt,W=10um, L=1 um, k' =194uA/V^2, λ =0.024 V^{-1}, tox=80 angstroms, Vt0= 0.6 volt Ignore velocity saturation effects.(a) Draw the ID-VDS characteristics for VDS from 0 to 3 volt and VGS =0.5v,1.5 V,3 V Assume VSB=0 (b)Draw the ID-VGS characteristics for VDS =2 V as VGS varies from 0 to 2 V with VSB =0,0.5V,1 V	CO1,CO2,CO3
2.	Design the complete small signal model for an pMOS transistor with ND=4×10^{16} atoms/cm^3. Device parameters are Φf=0.3 volt,W=10um, L=1 um,μp= 150 cm^2/V-s, λ =0.024 V^{-1}, tox=80 angstroms, Vt0=-0.8 volt. Ignore velocity saturation effects.(a) Draw the ID-VDS characteristics for VDS from 0 to -2 volt and VGS =-0.9,-1.2,-1.5,-1.8V Assume VSB=0 (b)Draw the ID-VGS characteristics for VDS =-2 V as VGS varies from 0 to -2 V	CO1,CO2,CO3
3.	Design common source amplifier , calculate the small signal voltage gain and the bias values of Vi and V0 at the edge of the triode region. Also calculate the bias values of Vi and Vo where the small signal voltage gain is unity with the transistor operating in the active region. What is the maximum voltage gain of this stage? Assume VDD= 3 V,RD=5kohm, k' =200uA/V^2, w=10 um ,L=1 um Vt=0.6 V and λ = 0. Check answer with SPICE.	CO1,CO2,CO3
4.	Design a widlar current source using npn transistor that produces a 10 uA output current .Use identical transistor with Vcc=30 Volt,R1=30k ohm . find output current .	CO1,CO2,CO3
5.	Design the MOS Peaking current source so that Iout=0.1 uA. a)Let I in = 1 uA and find the required value of R. b)Let R= 10 kohm and find the required Iin. In both cases assume that both the transistors are identical and operate in weak inversion with It=0.1 uA and n=1.5 , also find the minimum W/L, in both cases assuming that Vgs-Vt<0 is required to operate a transistor in weak inversion	CO1,CO2,CO3

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II Semester

EE1965	**Lab: Analog IC Design**	L= 0	T = 0	P = 2	Credits = 1

Evaluation Scheme	Continuous Evaluation	ESE	Total	ESE Duration
	40	60	100	

SN	Name of Experiment	Mapping with CO
6.	Determine the differential mode gain ,common mode gain, differential mode input resistance and common mode input resistance for differential amplifier with Itail=20uA,Rtail =10 Mohm, Rc =100kohm and VEE=Vcc=5 volt.neglect rb,ro,ru. Calculate CMRR. Also investigate the effects of adding nonzero rb and finite VA.	CO1,CO2,CO3
7.	For MOS two stage op amp ,Calculate the gain of the op amp assuming that it uses the 0.8 um process technology , assume that Leff=0.8 um and Vov=0.2 volt for all devices.	CO1,CO2,CO3
8.	Using Miller approximation, calculate the -3 db frequency of a common emitter transistor stage using the following parameters: Rs=1 kohm, rb=200 ohm, Ic=1 mA,β0=100,fT=400MHz,(at Ic=1 mA) Cμ=0.5 pF,RL=5kohm	CO1,CO2,CO3
9.	Design Current buffer circuit	CO1,CO2,CO3
10.	Design voltage buffer circuit	CO1,CO2,CO3
11	In switched capacitor amplifier assume that the source of M4 is connected to Vs instead of to ground. Calculate the output voltage that appears during Φ2 for a given Vs. Assume the op amp is ideal except that it has a finit gain a and a nonzero input capacitance Cp. Assume ideal MOS switches with zero on resistance and infinite off resistance	CO1,CO2,CO3

II Semester

EE1972	**Seminar**	L= 0	T = 0	P = 2	Credits = 1

Evaluation Scheme	Continuous Evaluation	ESE	Total	ESE Duration
	100		100	

III Semester

EE1982/EE1934	Mixed Signal VLSI Design	L= 3	T = 0	P = 0	Credits = 3

Evaluation Scheme	MSE-I	MSE-II	TA	ESE	Total	ESE Duration
	15	15	10	60	100	3 Hrs

Objective	Outcomes
• To study different types of mixed signal VLSI design and their procedures with methods applied in different stages of design.	1. Graduates will understand the challenges in modern VLSI Design and learn the skills of overcoming these problems when two opposing signal domains are integrated onto a single chip. 2. Graduates will understand the basic building blocks of Data converter systems. 3. Graduates will understand the review of fundamentals of semiconductor components. 4. Graduates will understand the basics of different data converters that are used in different mixed signal systems. 5. Graduates will understand the physical layout representation and the alternative layout solutions of data converter systems. 6. Graduates will understand the design of various CMOS Op-Amps used in mixed signal system. 7. Graduates will understand the design of various analog filers used in data converter systems.
Mapped Program Outcomes: a,b,d	

SN	Course Outcomes	Mapped PO						
		a	b	c	d	e	f	g
1	Graduates will understand the challenges in modern VLSI Design and learn the skills of overcoming these problems when two opposing signal domains are integrated onto a single chip.	M	M		H			
2	Graduates will understand the basic building blocks of Data converter systems.	M	M		H			
3	Graduates will understand the review of fundamentals of semiconductor components.	H	M		M			
4	Graduates will understand the basics of different data converters that are used in different Mixed signal systems.	M	M		H			
5	Graduates will understand the physical layout representation and the alternative layout solutions of data converter systems.	L	M		M			
6	Graduates will understand the design of various CMOS Op-Amps used in Mixed signal system.	M	L		M			
7	Graduates will understand the design of various analog filers used in data converter systems.	M	M		H			

Unit - I

Introduction to Mixed Signal VLSI System, Signal and Filters, digital comb filter, the z-plane, simple digital filters, Sampling and Aliasing: Impulse Sampling, Sample and Hold. Quantization noise.Spectral density of quantization noise.

Unit - II

Data Converter SNR: Effective number of bits Clock jitter, Using averaging to improve SNR, Decimating filters for ADCs, Interpolating filters for DACs, Band pass and High pass Sync filters, Using feedback to improve SNR.

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III Semester

EE1982/EE1934	**Mixed Signal VLSI Design**	L= 3	T = 0	P = 0	Credits = 3

Evaluation Scheme	MSE-I	MSE-II	TA	ESE	Total	ESE Duration
	15	15	10	60	100	3 Hrs

Unit - III

Sub-Micron CMOS circuit design : Process flow, capacitors and resistors, MOSFET Switch, Delay and Adder elements, Analog circuits – MOSFET Biasing, Op-Amp design, Circuit noise.

Unit - IV

Implementing Data converters: Current mode and voltage mode R-2R DAC, Using Op-Amps in data converters, Implementing ADCs, Cyclic ADC, Introduction to Sigma Delta ADC and Line Drivers.

Unit - V

Integrator Based CMOS Filters: Integrator Building Blocks, Low pass and Active R-C filters, MOSFET-C integrators,gm-C Integrators, Discrete time integrators

Unit - VI

Bilinear and Bi-quadratic transfer functions – Active R-C Transconductor-C and Switched Capacitor implementations both transfer functions, Canonic form of a digital filter.

Resources:

1. "CMOS – Mixed signal circuit design, layout and simulation",R.Jacob Baker, "2nd Edition
   a. IEEE Press and Wiley Interscience, 2002.
2. "CMOS Circuit Design, Layout, and Simulation", Third Edition, R. Jacob Baker

3. "Design of Analog CMOS Integrated circuits", B. Razavi, 1st Edition, McGraw Hill, 2001.
4. "CMOS Analog Circuit Design", P.E. Allen and D.R. Holberg, 2nd Edition, Oxford University Press, 2002.

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III Semester

EE1983	Micro-Electro-Mechanical Systems	L= 3	T = 0	P = 0	Credits = 3

Evaluation Scheme	MSE-I	MSE-II	TA	ESE	Total	ESE Duration
	15	15	10	60	100	3 Hrs

Objective	Outcomes
• The goals of this course are to go beyond the introduction stage in Micro-Electro-Mechanical Systems (MEMS) and Nano-Electro-Mechanical Systems (NEMS) to provide students with a strong background in design and characterization of micro and nano scale sensors and actuators with a broad range of applications in CNT-based sensors, actuators and devices, biomedical systems, micro- and nanoscale manipulation, adaptive optics, and microfluidics.	1. Graduates will be able to gain the knowledge of basic approaches for micro/nanosystems design 2. Graduates will be able to Understand state-of-the-art micromachining and packaging technologies 3. Graduates will be able to Learn new materials for micro/nanosystems applications 4. Graduates will be able to Develop experience on micro/nanosystems applications
Mapped Program Outcomes: a,b	

SN	Course Outcomes	Mapped PO						
		a	b	c	d	e	f	g
1	Graduates will be able to gain the knowledge of basic approaches for micro/nanosystems design	H	L					
2	Graduates will be able to Understand state-of-the-art micromachining and packaging technologies		M					
3	Graduates will be able to Learn new materials for micro/nanosystems applications		L					
4	Graduates will be able to Develop experience on micro/nanosystems applications	L						

Unit –I Smart Materials, Smart Structures, Integrated Microsystems, Micro Sensors, Actuators, Systems and Smart Materials

Unit –II Silicon Micromachining Technologies, Thin Film Deposition, Lithography, Etching, Specialized Materials for micromachining, advanced processes for Micromachining.

Unit –III Deformable Elements, Energy Methods for Elastic Bodies, Residual Stresses, Poisson Effects, Electrostatics, Coupled Electromechanics

Unit –IV Semiconductor Devices, Electronic Amplifiers, Practical Signal Conditioning, Circuits for Conditioning sensed signals, Control theory, Implementation of Controllers.

Unit –V Integration of Microsystems, Microsyststem Packaging, Case studies of Integrated Microsystems, Smart Structures in Vibration Control.

Unit – VI Scaling in Mechanical Domain, Electrostatic Domain, Magnetic Domain, Thermal Domain, Diffusion Domain, Fluid Domain, Optical Domain, and Biochemical Phenomenon.

Text Book:

G.K. Ananthasuresh, K.J. Vinoy, S. Gopalakrishnan, K.N. Bhat, V.K. Aatre , "Micro and Smart Systems, " Wiley India Publication, First Edition, 2010.

Resources:

1. "Between Technology &Science : Exploring an emerging field knowledge flows & networking on the nanoscale ", Martin S. Meyer,1st Edition, Universal Publisher ,2005
2. "Nanoscience& Technology: Novel structure and phenomea" Ping Sheng ,CRC Press, 2003
3. " Nano Engineering in Science & Technology : An introduction to the world of nano design ", Michael Rieth, CRC Press,
4. "Enabling Technology for MEMS and nano devices ", Balles, Brand, Fedder, Hierold.
5. "Optimal Synthesis Methods for MEMS", G. K. Ananthasuresh, Kluwer Academic Publishers, 2003
6. "MEMS & MOEMS Technology and Applications" P. RaiChoudhury, SPIE Press, 2000

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III Semester

EE1984	VLSI for Wireless Communication	L= 3	T = 0	P = 0	Credits = 3

Evaluation Scheme	MSE-I	MSE-II	TA	ESE	Total	ESE Duration
	15	15	10	60	100	3 Hrs

Objective	Outcomes
• To study the design concepts of low noise amplifiers. • To study the various types of mixers designed for wireless communication. • To study and design PLL and VCO. • To understand the concepts of CDMA in wireless communication.	1. Graduates will able to apply knowledge from basic engineering and other disciplines to identify, formulate and present solutions to technical problems in a variety of specialty areas related to telecommunications engineering technology. 2. Graduates will able to learn new related technologies in the fields of telecommunication and wireless networks along with the concepts of that require advanced knowledge within the field. 3. Graduates will able to apply advanced technical knowledge in multiple contexts.
Mapped Program Outcomes:	

SN	Course Outcomes	Mapped PO						
		a	b	c	d	e	f	g
1	Graduates will able to apply knowledge from basic engineering and other disciplines to identify, formulate and present solutions to technical problems in a variety of specialty areas related to telecommunications engineering technology.	H	H	M	L	M	M	L
2	Graduates will able to learn new related technologies in the fields of telecommunication and wireless networks along with the concepts of that require advanced knowledge within the field.	H	H	L	L	L	M	L
3	Graduates will able to apply advanced technical knowledge in multiple contexts.	H	H	H	M	M	L	L

Unit I : Communication Concepts
Overview of wired Systems, Standards, Access methods, Modulation Schemes, Classical channels, wireless channel , Multipath fading.,

Unit II:Receiver Architecture
Receiver frond end, Filter design, nonidealities and design parameters, deviation of Noise Figures.

Unit III:Low Noise Amplifiers (LNA)
Matching networks, Wideband LNA Design, Narrowband LNA Design, Narrowband LNA Core Amplifiers.

Unit IV:Active & Passive Mixers
Balancing, Qualitative description of Gilbert Mixer, Conversion gain, noise, switching mixer, Distortions in Mixers.

Unit V:Analog to Digital Converters
Demodulators, A/D conversion in Receiver, Implementation of Sigma Delta Modulators.

Unit VI:Frequency Synthesizers
PLL Based Frequency Synthesizer, Phase detector and charge pump, Loop Filters, Dividers, VCOs

Resources:
Bosco Leung, "VLSI For Wireless Communication, " Springer Publication, Second Edition,

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III Semester

EE1985	ASIC Design	L= 3	T = 0	P = 0	Credits = 3

Evaluation Scheme	MSE-I	MSE-II	TA	ESE	Total	ESE Duration
	15	15	10	60	100	3 Hrs

Objective	Outcomes
• The course is designed to teach students about Higher Methodology for ASICI design and includes various testing techniques, fault models, algorithms.	1. Graduates will able to eexplain types of ASICs, technology involved for sequential, combinational 2. Graduates will able to eexplain Programmable ASICs and its Logic cells and I/O cells of different vendors. 3. Graduate will be able to explain partitioning methods. 4. Graduate will be able to floor planning and placement 5. Graduates will able to eexplain ASIC construction and routing 6. Graduates will able to explain issues in chip design
Mapped Program Outcomes: a,c,d	

SN	Course Outcomes	Mapped PO						
		a	b	c	d	e	f	g
1	Graduates will able to explain types of ASICs, technology involved for sequential, combinational	H		M	H			
2	Graduates will able to explain Programmable ASICs and its Logic cells and I/O cells of different vendors.	H		H	H			
3	Graduate will be able to explain partitioning methods.	L		H	H			
4	Graduate will be able to floor planning and placement	L		H	H			
5	Graduates will able to explain ASIC construction and routing	L		H	H			
6	Graduates will able to explain issues in chip design	M		H	H			

Unit - I

Introduction to ASICs, Types of Asics, Design Flow, Economics of Asics, ASIC Cell Libraries, ASIC library design

Unit – II

Programmable ASICs: Antifuse, SRAM, EPROM, EEPROM, Shannons expansion theorem, multiplexer logic as function generator.

Unit – III

Physical design flow, System Partition, FPGA Partitioning, Partitioning Methods.

Unit – IV

Floor planning: Goals & Objectives, Measurement of Delay, Channel Definition, I/O & power planning. Placement: Goals & objective, placement algorithms.

Unit - V

Routing: Goals & objectives of global & detailed routing, measurement of channel density, Routing algorithms, special routing, circuit extraction & DRC.

Unit – VI

Issues in chip Design: Requirements of successful design, Soc, Power consumption issues, Power network, power optimization, chip power usage analysis, clock distribution, chip reliability, Analog integration in digital environment, crosstalk delay.

Resources:

1. "Application - Specific Integrated Circuits", M.J.S .Smith, 1st Edition, Addison -Wesley Longman Inc., 1997.
2. "VLSI Design", K.LalKishor,V.S.V.Prabhakar.
3. VLSI Circuits and Systems in Silicon", Andrew Brown, McGraw Hill, 1991.
4. Field Programmable Gate Arrays" S.D. Brown, R.J. Francis, J. Rox, Z.G. Uranesic-Kluever Academic Publishers, 1992.

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III Semester

EE1986	**Semiconductor Memory Design**	L= 3	T = 0	P = 0	Credits = 3

Evaluation Scheme	MSE-I	MSE-II	TA	ESE	Total	ESE Duration
	15	15	10	60	100	3 Hrs

Objective	**Outcomes**
• Memory is an important part in many digital circuits and microcontrollers. This course discusses implementation methods and problems in designing and making semiconductor memories.	1. Graduates will be able to apply knowledge from undergraduate engineering and other disciplines to identify, formulate, solve novel advanced electronics engineering along with design coding that require advanced knowledge within the field. 2. Graduates will be able to apply advanced technical knowledge in multiple contexts 3. Graduates will be able to understand and design advanced memory systems
Mapped Program Outcomes: a,b,e	

SN	**Course Outcomes**	**Mapped PO**						
		a	**b**	**c**	**d**	**e**	**f**	**g**
1	Graduates will be able to apply knowledge from undergraduate engineering and other disciplines to identify, formulate, solve novel advanced electronics engineering along with design coding that require advanced knowledge within the field.	H						
2	Graduates will be able to apply advanced technical knowledge in multiple contexts	H						
3	Graduates will be able to understand and design advanced memory systems	H	M		H			

Unit I

Study of semiconductor devices such as BJT and MOSFET etc. as a memory element. Masked Read-Only Memories (ROMs)-High Density ROMs-Programmable Read-Only Memories (PROMs)-Bipolar PROMs-CMOS PROMs-Erasable (UV) - Programmable Road-Only Memories (EPROMs)-Floating-Gate EPROM Cell-One-Time Programmable (OTP) Eproms-Electrically Erasable PROMs (EEPROMs)- EEPROM Technology And Architecture-Nonvolatile SRAM-Flash Memories (EPROMs or EEPROM)- Advanced Flash Memory Architecture.

Unit II

SRAM Cell Structures-MOS SRAM Architecture-MOS SRAM Cell and Peripheral Circuit Operation-Bipolar SRAM Technologies-Silicon On Insulator (SOI) Technology-Advanced SRAM Architectures and Technologies- Application Specific SRAMs.

DRAM Technology Development-CMOS DRAMs - DRAMs Cell Theory and Advanced Cell Strucutures - BiCMOS, DRAMs - Soft Error Failures in DRAMs - Advanced DRAM Designs and Architecture-Application Specific DRAMs.

Unit III

Masked Read-Only Memories (ROMs)-High Density ROMs-Programmable Read-Only Memories (PROMs)-Bipolar PROMs-CMOS PROMs-Erasable (UV) - Programmable Road-Only Memories (EPROMs)-Floating-Gate EPROM Cell-One-Time Programmable (OTP) Eproms-Electrically Erasable PROMs (EEPROMs)-EEPROM Technology And Architecture-Nonvolatile SRAM-Flash Memories (EPROMs or EEPROM)-Advanced Flash Memory Architecture.

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III Semester

EE1986	**Semiconductor Memory Design**	L= 3	T = 0	P = 0	Credits = 3

Evaluation Scheme	MSE-I	MSE-II	TA	ESE	Total	ESE Duration
	15	15	10	60	100	3 Hrs

Unit IV

RAM FaultModelling, Electrical Testing, Peusdo Random Testing-Megabit DRAM Testing-Non-volatile, Memory Modelling and Testing-IDDQ Fault Modelling and Testing-Application Specific Memory Testing

Unit V

General Reliability Issues-RAM Failure Modes and Mechanism-Non-volatile Memory Reliability-Reliability Modelling and Failure Rate Prediction-Design for Reliability-Reliability Test Structures-Reliability Screening and Qualification. RAM Fault Modelling, Electrical Testing, Pseudo Random Testing-Megabit DRAM Testing- Non-volatile Memory Modelling and Testing-IDDQ Fault Modelling and Testing-Application Specific Memory Testing.

Unit VI

Radiation Effects-Single Event Phenomenon (SEP)-Radiation Hardening Techniques-Radiation Hardening Process and Design Issues-Radiation Hardened Memory Characteristics-Radiation Hardness Assurance and Testing - Radiation Dosimetry-Water Level Radiation Testing and Test Structures. Ferroelectric Random Access Memories (FRAMs)-Gallium Arsenide (GaAs) FRAMs - Analog Memories-Magneto-resistive Random Access Memories (MRAMs)-Experimental Memory Devices. Memory Hybrids and MCMs (2D)-Memory Stacks and MCMs (3D)-Memory MCM Testing and Reliability Issues-Memory Cards-High Density Memory Packaging Future Directions.

Resources:

1. "Semiconductor Memories", Ashok K. Sharma, Two-Volume Set, Wiley-IEEE Press, 2003
2. "DRAM Circuit Design: A Tutorial", Brent Keeth, R. Jacob Baker Wiley-IEEE Press, 2000
3. "High Performance Memories: New Architecture DRAMs and SRAMs - Evolution and Function", Betty Prince, Wiley, 1999
4. Nonvolatile Memory Technologies with Emphasis on Flash, IEEE Press series on Microelectronics by Joe E Brewer and Manzur Gill 2008.

III Semester

EE1987/EE1938	Advanced Computer Architecture	L= 3	T = 0	P = 0	Credits = 3

Evaluation Scheme	MSE-I	MSE-II	TA	ESE	Total	ESE Duration
	15	15	10	60	100	3 Hrs

Objective	Outcomes
• The objective of this course is to introduce the fundamental techniques on which high-performance computing is based, to develop the foundations for analyzing the benefits of design options in computer architecture, and to give some experience of the application of these techniques.	1. Understand and evaluate the hardware components of advanced architectures Understand and analyze architectures performance and select among different ones for particular use scenarios 2. Understand and analyze the most important parallel architectures in order to distinguish their main difference. 3. Understand the levels of software and hardware comprising the Instruction Set Architecture (ISA) of a computer 4. Make design decisions based on performance data.
Mapped Program Outcomes: a, c,d	

SN	Course Outcomes	Mapped PO						
		a	b	c	d	e	f	g
1	Understand and evaluate the hardware components of advanced architectures Understand and analyze architectures performance and select among different ones for particular use scenarios	M						
2	Understand and analyze the most important parallel architectures in order to distinguish their main difference.	M			M			
3	Understand the levels of software and hardware comprising the Instruction Set Architecture (ISA) of a computer	M		M	M			
4	Make design decisions based on performance data				M			

Unit I

The state of computing, Classification of parallel computers, Multiprocessors and multicomputers, Multivector and SIMD computers. Conditions of parallelism, Data and resource Dependences, Hardware and software parallelism, Program partitioning and scheduling, Grain Size and latency, Program flow mechanisms, Control flow versus data flow, Data flow Architecture, Demand driven mechanisms, Comparisons of flow mechanisms

Unit II

Network properties and routing, Static interconnection Networks, Dynamic interconnection Networks, Multiprocessor system Interconnects, Hierarchical bus systems, Crossbar switch and multiport memory, Multistage and combining network.

Unit III

Advanced processor technology, Instruction-set Architectures, CISC Scalar Processors, RISC Scalar Processors, Superscalar Processors, VLIW Architectures, Vector and Symbolic processors

Unit IV

Linear pipeline processor, nonlinear pipeline processor, Mechanisms for instruction pipelining, Dynamic instruction scheduling, Branch Handling techniques, branch prediction, Arithmetic Pipeline Design, Computer arithmetic principles, Static Arithmetic pipeline, Multifunctional arithmetic pipelines

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III Semester

EE1987/EE1938	**Advanced Computer Architecture**	L= 3	T = 0	P = 0	Credits = 3

Evaluation Scheme	MSE-I	MSE-II	TA	ESE	Total	ESE Duration
	15	15	10	60	100	3 Hrs

Unit V

Cache basics & cache performance, reducing miss rate and miss penalty, multilevel cache hierarchies, main memory organizations, design of memory hierarchies.

Unit VI

Symmetric shared memory architectures, distributed shared memory architectures, models of memory consistency, cache coherence protocols (MSI, MESI, MOESI), scalable cache coherence, overview of directory based approaches, design challenges of directory protocols, memory based directory protocols, cache based directory protocols, protocol design tradeoffs, synchronization,

Resources:

1. "Advanced computer architecture", Kai Hwang, Tata McGraw Hill,1993
2. "Computer organization and design" ,D. A. Patterson and J. L. Hennessey, 2nd Edition, Morgan Kaufmann,
3. "Computer Architecture and organization", J.P.Hayes, 3rd Edition, McGraw Hill,1998
4. "Memory System and Pipelined processors" Harvey G.Cragon , NarosaPublication,1998
5. "Parallel computer";V.Rajaranam&C.S.R.Murthy, Printice Hall of India,2002
6. "Foundation of Parallel Processing", K.Ghose, RajanMoona&Phalguni Gupta, Narosa Publications,2002

III Semester

EE1981	**Project Phase – I**	L= 0	T = 0	P = 16	Credits = 8

Evaluation Scheme	Continuous Evaluation	ESE	Total	ESE Duration
	100		100	

Objective	**Outcome**
	1. Students will be able to identify and formulate problem effectively through literature survey and analysis. 2. Students will be able present the idea effectively with good presentation and communication skill 3. Students will be able to use related EDA tools and related software. 4. Students will be able to understand project management and the importance of social and research ethics.
Mapped PO:a,b,c,d,e,f,g	

IV Semester

EE1991	Project Phase - II	L= 0	T = 0	P = 24	Credits = 12

Evaluation Scheme	Continuous Evaluation	ESE	Total	ESE Duration
	40	60	100	

Objective	Outcome
	1. Students will be able to identify and formulate problem effectively through literature survey and analysis. 2. Students will be able present the idea effectively with good presentation and communication skill 3. Students will be able to use related EDA tools and related software. 4. Students will be able to understand project management and the importance of social and research ethics.
Mapped PO:a,b,c,d,e,f,g	